A Wide-Tuning Range Transformer-Based RF CMOS Oscillator

by

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Abstract

In this thesis a method of producing a VCO with a wide enough tuning range, such that the correct centre frequency can be ensured, is presented. This is achieved without compromising the power consumption of the circuit. The work is novel in that a transformer is preferred to an inductor to help maximize this tuning range. The design was fabricated in a CMOS 0.18μm technology, and has a frequency tuning range lying between approximately 2.0 and 2.8 GHz, drawing 20mA from a 1.8V supply. A staggered-tuning range was employed to minimize the effect of noise on the analog control voltage, so the control process is a dual one, with both analog and digital controls.The oscillator produces quadrature outputs which are essential for many transceiver systems. Two chips have been submitted for fabrication. The second design will be tested in November 2001.

Acknowledgments

I would like to start by thanking Ken Martin for having given me the wonderful opportunity to come work in such a positive environment. Thanks so much for all your help and consideration!

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To my father Robin, and sisters Sophie and Emily.

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Chapter 1

Introduction

The growth in telecommunication systems enforces the need for low-power, high-quality, fully-integrated transceivers. The digital baseband signal processing that is required in portable mobile systems, such as mobile phones, is implemented in sub-micron CMOS. With the existing standards that dictate high transceiver performance, such as *GSM*, *DECT*, *IEEE 802.11b*, *HomeRF* and *Bluetooth*, the RF blocks within the transceiver have typically been implemented in bipolar or GaAs processes. With decreasing gate widths in CMOS technology as well as significant research, many of the RF components implemented in alternate technologies are now being implemented in CMOS [Gramega, '01; Craninckx, '97]. Design of a frequency synthesizer in sub-micron CMOS, is still one of the greatest challenges. The selectivity requirements for the standards introduced are severely restrictive and with them come other constraints, such as power minimization, and tuning range. To achieve these requirements LC-oscillators which have high Q-factor off-chip resonators (used within a phase locked loop, PLL) are preferred. Recently there has been a push to also integrate the oscillator's resonator [Hajimiri, '99; Tiebout, '01]. Unfortunately for a digital CMOS process the Q-factor of these inductors tends to be poor (Q<10), thereby hampering the selectivity of the transceiver. Frequency synthesis is made possible by a PLL within the transceiver, a general block diagram is shown in Figure 1.1.

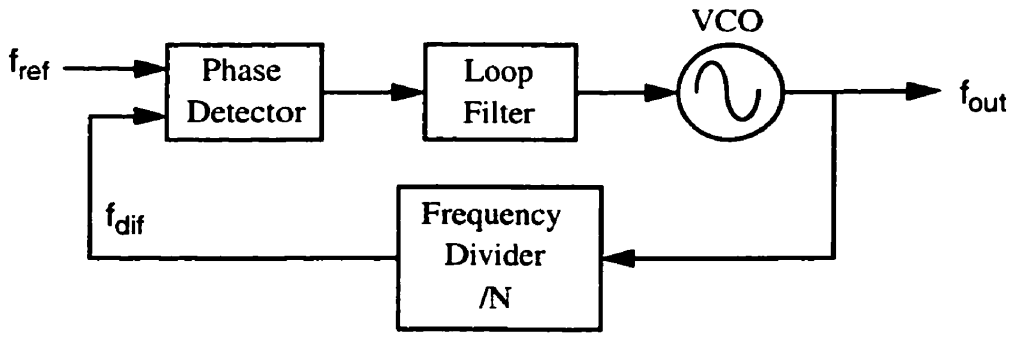

FIGURE 1.1 PLL Frequency Synthesizer

The feedback action within the loop causes the output frequency to be N times greater than the reference frequency. This reference signal is usually taken from a stable, low-frequency crystal oscillator. The spectral purity of the synthesized signal will largely depend on the quality of the VCO.

1.1 The *Bluetooth* Standard

The two oscillators presented in this work have centre frequencies of 2.5GHz and 2.35GHz. There are a number of standards for which the design would be suitable, such as *HomeRF* (2.404->2.478GHz), *Bluetooth* (2.402->2.48) GHz and the *IEEE* standard *802.11b* (2.40->2.4835GHz). Due to the large tuning range of both designs presented, it may not be necessary to alter the centre frequency of the oscillators, while still allowing for full coverage of temperature and process variations. This section will present the reader with a brief description of *Bluetooth*, a technology named after Harald Blatand (Bluetooth), a tenth-century Danish king who conquered much of Scandinavia. The reasons for this choice will become evident.

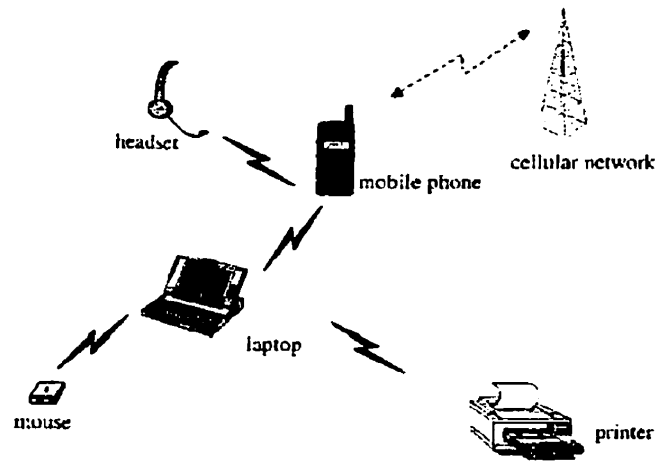

FIGURE 1.2 *Bluetooth* Applications

A possible *Bluetooth* application is shown above [*Economist*, '00]. A typical technophile on a train will carry a personal digital assistant (PDA), a lap-top computer, and possibly a small printer. She can then connect her PDA or computer to her mobile phone via an infra red connection or cable and then connect to the Internet over the cellular network. *Bluetooth* is a wireless based system, such that no cables are required to connect the devices of

this 'personal-area network' (PAN). Infra red links could also be used but they have a limited range, require direct line-of-sight, are sensitive to device orientation, and in principle can only be used between two devices with in the PAN. In addition, radios have greater range, can propagate around and through materials and connect to many devices simultaneously. Using *Bluetooth* in conjunction with a replacement of the existing 'circuit-switched' telephone networks to 'packet-switched' networks would facilitate high rates of data transfer between the PAN and the rest of the digital world. Packet-switched networks, in contrast to circuit-switched networks, are constantly on, so that data can be sent or received with no pause to establish a connection. A number of packet-switched networks are in existence, including Japan's *i-mode* phones and the interactive paging networks used by *Research in Motion*'s hand-held devices. *Bluetooth* aims to replace cables, docking cradles and incompatible standards with a tiny chip and antenna in each device, enabling wireless communication within the PAN, which in turn could communicate with other devices outside of this network using the local cellular network.

In February 1998, five major companies, led by *Ericsson*, formed a special interest group to create a standard radio interface to allow for wireless connectivity between electronic devices. A single standard ensures inter-operability between devices, regardless of their manufacturer, thus breaking the previous competitive (incompatibility) philosophy that had restricted the growth of consumer-electronics. *Microsoft*, *3Com*, *Lucent* and *Motorola* also joined the fray in 1999, and now hundreds of companies are also adopting this standard. Eighteen months after its foundation, the first version of the *Bluetooth* specification was published, outlining both control software and radio protocols, thus enabling companies to begin designing radio-equipment and applications.

As a technology there is nothing radically new about *Bluetooth*. As a standard it is just a modification of standards used in products like cordless digital phones and wireless LANs. Like them it uses a 'spread-spectrum' technique, finding all the unused frequencies within its frequency band. It then 'spreads' its signal power over these available frequencies, hopping from frequency-frequency more than a thousand times a second. It constantly adjusts to changing interference conditions, making the best use of the frequencies available.

Depending on the location of the receiver, *Bluetooth* modifies the transmitted signal power in a manner similar to cordless digital phones and wireless LANs. It utilizes signal encryption as well as an encrypted frequency mapping scheme, so that its signal cannot be easily intercepted or understood. And like many commercially available wireless consumer products, it operates in the unlicensed 2.4GHz frequency band.

What makes *Bluetooth* unique is that it scans its environment, looking for compatible devices that are in range and that have the appropriate identification. Once one or more devices have been identified, an ad-hoc network is established known as a 'piconet' [Haarsten, '00]. Several piconets can communicate with each other forming a 'scatternet'. *Bluetooth* supports point-multipoint transmission.

This could also be achieved using a wireless LAN with the standard *IEEE 802.11b* [*Economist*, '01], which offers greater range, higher bandwidth (11MB/s compared to *Bluetooth*'s 1MB/s) and a greater compatibility with wired LANs. The plug-in circuit cards used for this standard are physically large, expensive and consume a great deal of power. Because of these constraints, these cards are aimed at the corporate market. *Bluetooth* has been designed explicitly for the consumer market in three important ways:

1) *Bluetooth* has been designed to be cheap, the transceiver unit should sell for no more than $5.

2) *Bluetooth* is a passive technology, no effort is required from the user to establish connections between the devices of a piconet.

3) It should be designed to have superior performance to other existing wireless products.

Transceiver power constraints for *Bluetooth* are more restrictive than *IEEE 802.11b* or *HomeRF* [Lansford, 00], but the phase-noise requirement is not as severe: $L_{\geq 3MHz} \leq -124\frac{dBc}{Hz}$, so it is possible for a oscillator to meet these requirements with a integrated inductor [Klepser, 00].

1.2 Thesis Outline

Chapter 2 gives some background to RF oscillator design. It reviews some fundamental oscillator theory, some published topologies and methods for implementation of a CMOS LC oscillator, and finally a discussion of oscillator phase noise is presented. This discussion outlines some of the mechanisms which lead to the non-ideal frequency-spectrum that is observed for any real oscillator, as well as the detrimental impact it has on transceiver operation. Chapter 3 describes the design of the oscillator, and includes both transient oscillator simulations as well as s-parameter plots of the tank transformer. Chapter 4 outlines the test method and results. Chapter 5 concludes the work with an outline of the second design submitted to *CMC (Canadian Microelectronics Corporation)*, future work that is considered, and finally a discussion as to why a transformer-based oscillator may be preferred over a LC oscillator.

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Chapter 2

RF LC Oscillators: A Background

This chapter is dedicated to reviewing CMOS LC oscillator topologies. A General Phase-Noise Theory is also described that assumes a Linear Time-Variant (LTV) methodology.

2.1 Basic Oscillator Theory

An oscillator is an amplifier included in a positive feedback loop (with a frequency-selective feedback block) so as to produce an unstable system. The resulting instability is controlled by introducing some form of non-linearity to the structure so that the resulting signal amplitude is 'limited'. A necessary condition for oscillation, known as the Barkhausen criterion, is expressed in terms of the feedforward and feedback blocks that are integral parts of the oscillator structure. The Barkhausen criterion dictates that a self-sustained oscillation will occur in a feedback system at a frequency at which the phase shift around the loop is zero and the loop gain equals unity, i.e.:

$$|G(j\omega_o)| = 1 \tag{1}$$

and

$$\angle G(j\omega_o) = 0. \tag{2}$$

An alternative approach to examining the behavior of the oscillator is to examine the poles of the system. For any filter structure or stable analog amplifier, it is necessary to ensure that the poles remain in the left half of the s-plane. In contrast to a stable linear circuit, an oscillator is inherently unstable; we therefore desire to place the poles of such a circuit on the $j\omega$ axis, i.e. $s = \pm j\omega_o$. In practice the loop gain is designed to be greater than unity, which will ensure proper start up of the oscillator and will provide continued oscillation. To prevent the exponential growth of the signal, some form of non-linear amplitude control is included to force the poles back from the right half plane on to, or close to the $j\omega$ axis. This may manifest as a separate circuit, often labelled Automatic Level Control

(ALC), which fixes the output amplitude of the oscillator. ALC circuits add to the complexity of the design and also add to the power consumption and chip area. With ever increasing integrability and longer unit life being essential for economic competitiveness, both of these disadvantages are important considerations in mobile communications. An alternative way of limiting the output amplitude of the oscillator is to employ the already existing non-linearity of the transistors, thereby forcing the amplifier in to saturation for part of the cycle, i.e. using the transistors as switches.

It is important to mention that the Barkhausen criteria is necessary but not always sufficient; for a phase shift of 180 degrees around the loop the circuit will latch-up as opposed to oscillate.

2.1.1 Negative Resistance Analysis

This work has been concerned with the implementation of a negative-G_m oscillator. This type of oscillator is in common use for RF applications, in many different technologies. The basic concept is that if a negative admittance is placed in parallel with a lossy LC tank, an oscillation will be initiated, whose amplitude will grow until inherent amplitude limiting reduces the net resistance of the circuit to zero. A differential negative admittance was implemented, but for illustrative purposes it is shown below how a FET with its gate tied to a small signal ground by an inductance can be used to implement a negative resistance (Figure 2.1).

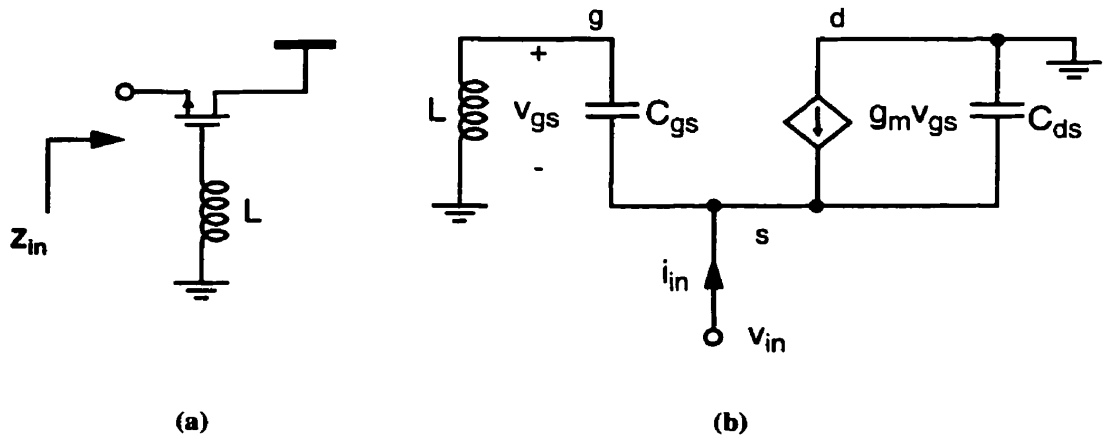

FIGURE 2.1 Implementation of negative-R using a transistor with an 'inductive' gate.

If C_{gd} is neglected and performing KCL at the source (in this case the input), results in the following equation:

$$i_{in} + g_m v_{gs} = \frac{v_{in}}{\frac{1}{j\omega C_{gs}} + j\omega L} + v_{in}(j\omega C_{ds}) . \tag{3}$$

If we note that (using voltage division):

$$v_{gs} = -v_{in}\left(\frac{\frac{1}{j\omega C_{gs}}}{\frac{1}{j\omega C_{gs}} + j\omega L}\right) \tag{4}$$

and we only consider the real part of the impedance, then we find that:

$$Re(Z_{in}) = Re\left(\frac{v_{in}}{i_{in}}\right) = \frac{1 - \omega^2 L C_{gs}}{g_m} . \tag{5}$$

For frequencies much larger than the resonant frequency of LC_{gs} and lower than ω_T (the angular frequency at which the current gain of the transistor is unity), R_{in} is found to be approximately:

$$R_{in} \approx \frac{-\omega^2 L}{\omega_T} . \tag{6}$$

It has been assumed here that $\omega_T = \frac{g_m}{C_{gs}}$.

In this work two cross-coupled transistors, as shown in Figure 2.2, are used to synthesize a negative resistance. It is more intuitive to consider this configuration to be acting as a negative admittance, as will be discussed later in this thesis. This circuit can be shown to have a negative resistance of:

$$R_{in} \approx \frac{-2}{g_m} . \tag{7}$$

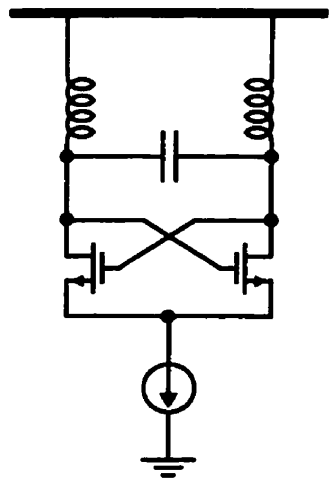

FIGURE 2.2 Differential Implementation of negative-g_m. oscillator.

2.2 Voltage Controlled Oscillators

The frequency of RF oscillators must be adjustable. This is in order to account for process sensitivities and perhaps to allow for transceiver channel selection. An ideal Voltage Controlled Oscillator (VCO) may be defined to be a circuit whose output is a sinusoid with a frequency that varies linearly with respect to a control voltage:

$$\omega_{OSC} = \omega_{FR} + K_{OSC} V_{cont} \quad . \tag{8}$$

To allow generation of the carrier signal in most transceiver structures, a VCO will be placed in a phase locked loop, with the necessary frequency dividers (multipliers). Implementation of a linearly-controlled LC oscillator is not a straight forward task due to the relationship that the oscillator's output frequency has with respect to any variation in tank capacitance, i.e. $\omega_{OSC} \propto \frac{1}{\sqrt{C_{tank}}}$. Some methods have been developed to ensure reasonable linearity, one of which will be discussed in Section 2.1.3.

2.2.1 Varactor Diodes

Varactor diode structures are p+/n- structures placed in a N-Well. Their capacitance can be varied by modifying the reverse bias across the diode, or modulating the well's potential.

The structure is shown in Figure 2.3 with two possible tank configurations shown in Figure 2.4.

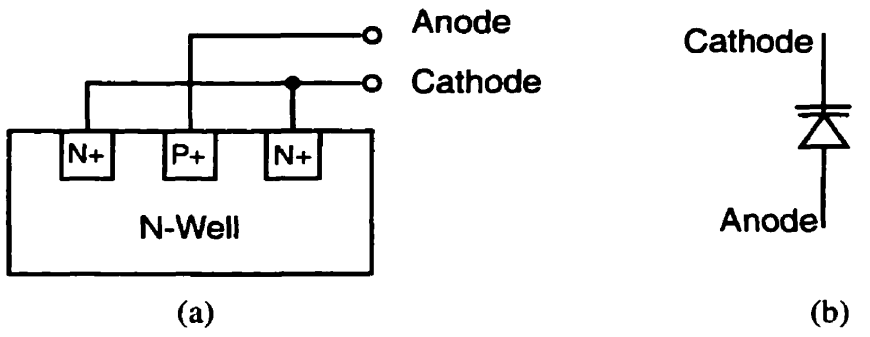

FIGURE 2.3 a) Physical Structure of diode, b) Schematic representation.

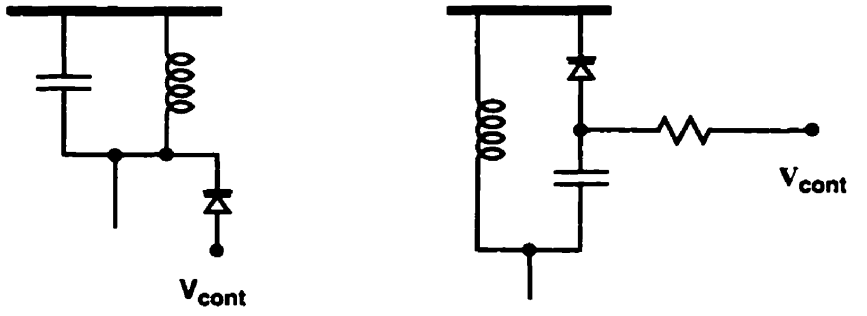

FIGURE 2.4 Varactor Diodes added to a Tank.

This type of varactor structure suffers from two inhibitors: the Q of these structures is often poor, and the tuning range is limited. Oscillator tuning range is an important transceiver specification, because the centre frequency and tuning range of the oscillator will be affected by process variations. The inductance value of on-chip planar inductors will map the designed inductance well (+/- 5%), and can be firmly evaluated by laying out inductor structures for test. Capacitance values however may deviate by as much as 20% from designed values. Designs that utilize bond wire inductance will also suffer greatly from process variation. Therefore, it is necessary to design a resonant tank that will be able to compensate for process variations, i.e. maximize tuning range without compromising the phase noise performance of the circuit. There has been recent research into improving the Q and tuning range of varactor structures by improved layout techniques and utilizing the differential nature of the output of many oscillators [Porret, 2000].

2.2.2 MOS Varactors

There are two types of MOS capacitors that can be exploited to implement a varactor: they are the more common inversion FET and the accumulation mode FET. The inversion device has been exploited between strong inversion and depletion [Kral, 98; Hung, 98; Castello, 98; Andreanai, 98]. This structure suffers from some limitations in spite of its ease of manufacture:

1) The quality factor of the varactor in its weak and moderate inversion regions is reduced by the series resistance of its channel.

2) The effective tunability is limited by the overlap capacitance between the lightly doped diffusions (LDD) and the gate of the device. Therefore the tunable capacitance is limited to a narrow range of the channel.

Accumulation mode FETs are relatively uncommon although they can exhibit excellent performance characteristics. One stark difference is the threshold voltage of the latter device; the controlling voltage must swing in a bipolar fashion to ensure maximum variations in the capacitance of the structure. Below we can inspect the structures of the devices as well as their performance characteristics with regard to tuning range and Q-factor.

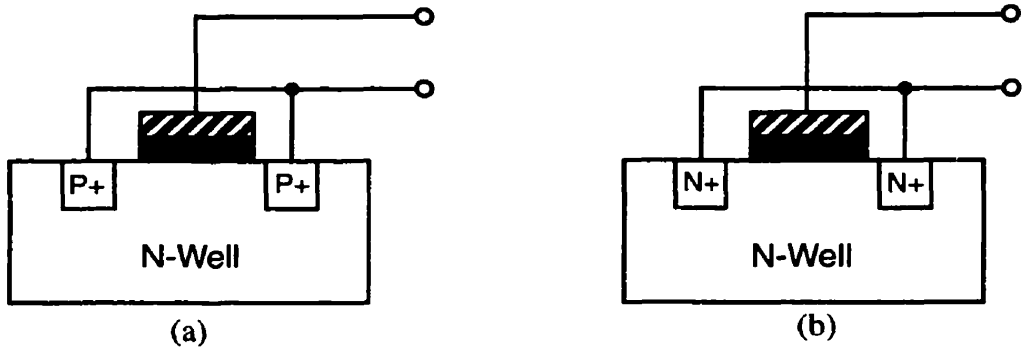

FIGURE 2.5 a) PMOS Capacitor Varactor, b) NMOS Accumulation Varactor.

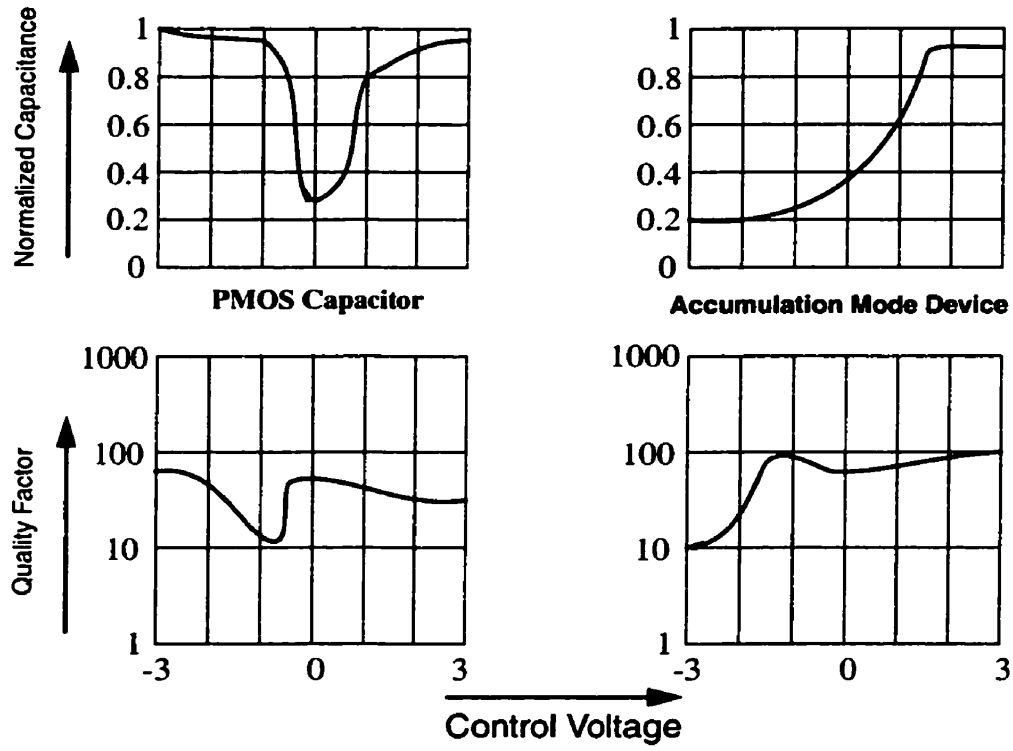

FIGURE 2.6 Capacitance & Q-Factor for MOS Capacitors versus Control Voltage [Porret, 2000]

2.2.3 A Novel Varactor Structure

A novel varactor structure has been proposed recently [Wong, '00], with the intention of increasing the tunability of an LC CMOS tank beyond what was previously possible using the conventional structures such as the reverse-biased pn junction diode, and the MOS capacitors previously discussed. A cross section of this device is shown in Figure 2.7. This device can be considered an amalgamation of the structures shown in Figures 2.5 a) and b). The structure is similar to a PMOS device except that one of the p+ diffusions is replaced by a n-diffusion. In this work [Wong, '00], the authors suggest that the device can be used as a three terminal device, i.e. its capacitance may be varied by altering the gate voltage or modulating the drain-source potential difference. It may also be possible to utilize the well of the device to enlarge its tuning range, or to add an extra level of controllability. However this technique is not explored in the paper.

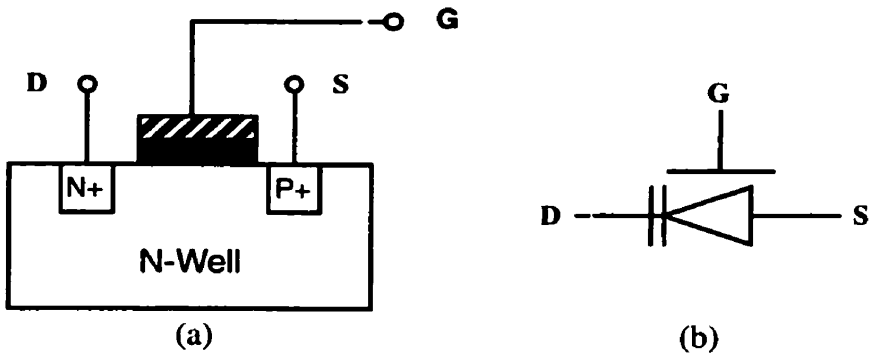

FIGURE 2.7 Novel Varactor Structure: a) Cross Section, b) Circuit Symbol.

An application of this device is also presented, as shown in Figure 2.8. This topology ensures a linear relationship between the controlling voltage and the frequency of the oscillator's output; this is due to the introduced non-linearity of the source follower device, which cancels the existing non-linear characteristic of the varactor device. A detailed physical explanation as to the operation of the device is presented in [Wong, '00]. This may be summarized by concluding that because of the presence of the gate capacitance, the junction capacitance, as well as the parasitics, the device yields a higher capacitance per unit area than conventional structures.

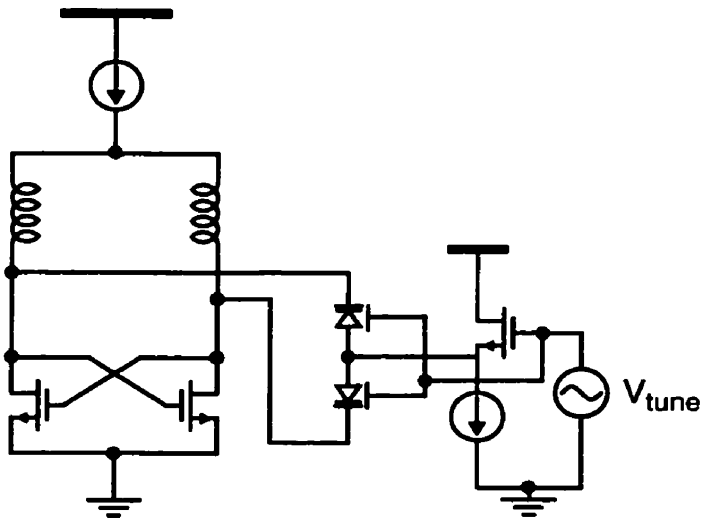

FIGURE 2.8 VCO Schematic taking advantage of the Novel Varactor Design.

2.2.4 Switched Reactor Structures

In 1998, a paper was presented by researchers from the University of California, L.A. at the Custom Integrated Circuits Conference (CICC) [Kral, '98]. This paper described new oscillator topologies, aspiring to solve the problem of the limited tuning range of existing oscillator topologies in CMOS technology. The paper introduces two topologies: a resonant tank using a switched (fixed) capacitor to modify the centre frequency of oscillation, and an alternate tank that switches different inductors to modify resonances. The two schematics are presented here, as designed by the authors of [Kral, '98]. Both designs were laid out in a 0.6μm CMOS process. The 'RF Switch' (in the switched-capacitor design) is a low resistance, large transistor with an asymmetrical layout so as to minimize the parasitic drain capacitance and thus reduce the loading effect of the switch while in its 'off' state. The source capacitance of the transistor is increased, but this proves unimportant as the source is connected to ground.

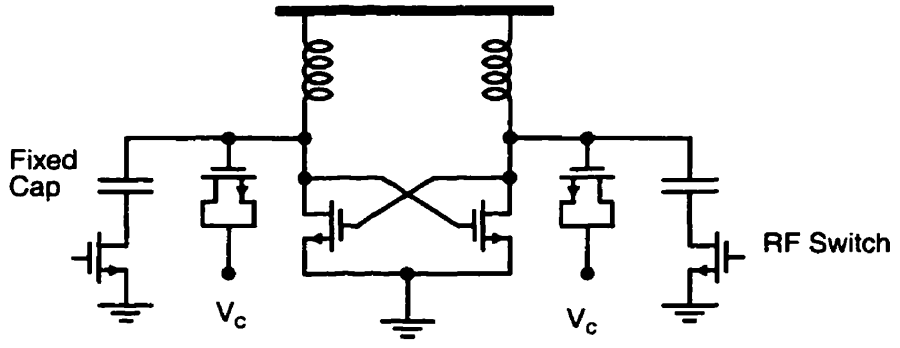

FIGURE 2.9 Oscillator that utilizes Fixed Capacitor for Coarse Frequency Adjustment.

Note that in the second topology (Figure 2.10) instead of switching inductors directly, the technique used switches in one of four oscillators each having a different tank inductance. This method is preferred, as switching inductors directly in the oscillator structure would degrade the Q factor of the on-chip inductor (which is already limited to Q<10), because of the finite on-resistance of the switches available.

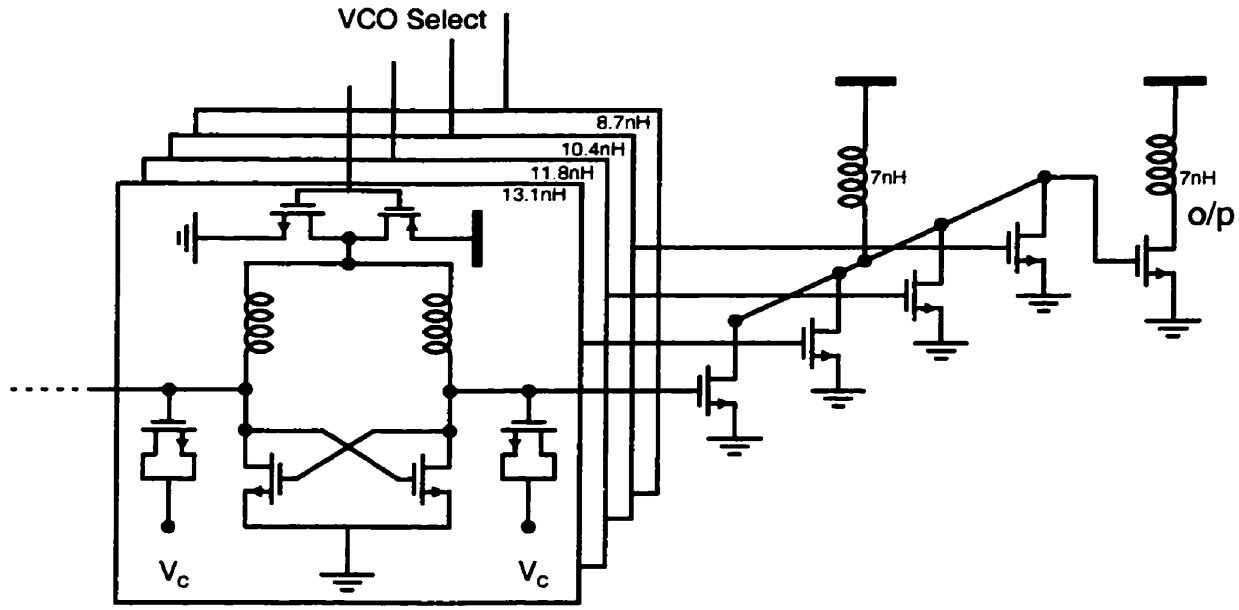

FIGURE 2.10 Switched Array of Oscillators using a Common Output.

The above structure, while displaying a large tuning range (26%), suffers from the fact that the chip area of the core oscillator structure is four times larger than a single oscillator structure. While it may be possible to justify this increase with a ring oscillator, LC oscillators require large areas of silicon due to the sizeable dimensions of on-chip inductors. From a cruder perspective, one may conclude that the above design is not actually one oscillator but four oscillators combined, so the initial problem of increasing oscillator tuning range has not been solved. The switched capacitor design exhibits a tuning range of 12%. This switched capacitor topology was also utilized by Level One Communications, Incorporated, [Cho '99]; no oscillator specifications were presented in this paper. The approach used in this thesis is a modification of the switched capacitor design.

2.2.5 Bondwire Inductors

Until now the design emphasis on inductors for RF applications has been in trying to improve planar, on-chip inductors by utilizing standard processing steps, or by introducing extra processing steps such as selectively etching the substrate out from under the inductor structure. There has also been investigation into the properties and applications of bondwire inductors. Bondwires have a very low series resistance and therefore have a higher

quality factor than their on-chip counterparts (even though this resistance will be degraded at higher frequencies due to the skin effect). An approximate rule of thumb for the design of LC tanks using bondwire inductors is that the inductance is approximately 1nH/mm. Jan Craninckx and Michel Steyaert, from the Katholieke Universiteit of Leuven, pioneered the use of bondwire inductors as tank elements in CMOS oscillators [Craninckx, '95]. Analog Designers have been incorporating bondwire inductances into the end design of many RF circuits, such as input matching of low noise amplifiers [Meyer, '94] or extra inductance in oscillator design (for example, providing a path to an off-chip tank) [Margarit, '99]. The Belgian researchers extensively simulated the behavior of bondwire structures, in order to determine how their reactance varied with length, height and separation from other bondwires. These simulations were run using a finite-element simulator and the first order equations presented in [Craninckx, '95] were confirmed (to a reasonable level of accuracy):

$$L = \frac{l}{5}\left[\ln\left(\left(\frac{2l}{r}\right) - 0.75 + \frac{r}{l}\right)\right] \tag{9}$$

$$M = \frac{l}{5}\left[\ln\left(\frac{l}{d} + \sqrt{1 + \left(\frac{l}{d}\right)^2}\right) - \sqrt{1 + \left(\frac{d}{l}\right)^2} + \frac{d}{l}\right] , \tag{10}$$

where l is the wire length, r is the wire radius, and d is the distance between inductors. An 'enhanced' differential tank was incorporated to improve the SNR of the oscillator over an equivalent LC tank by 6dB, but with the downside of reducing the tuning range of the oscillator by 50%, as only 'half' of the tank capacitance is adjustable. The differential structure also infers that only the external bondpad (at the end of the bondwire) will load the tank because the internal pad will be a common mode node and so its parasitics will not be important.

Using a differential tank with bondwire inductors was the design initially considered in this research. The reference paper discussed above is highly detailed and excellent phase noise results were achieved with reasonable power consumption. There are, however, a number of disadvantages to using bondwire inductors:

1) The bondwires are bonded across the length of the silicon area, which means that the length of the chip would need to be significant in order to attain sufficiently large inductance values. The authors used two bondwires, each of length 1.5mm, to achieve a tank inductance of approximately 3nH. Thus, the overall chip length was greater than 1.5mm. In terms of mass production this may not matter as the vacant area underneath the bondwires can be used for other transceiver components, but it becomes a factor when submitting a single design to CMC.

2) The tuning range reported was 4.5% for a 3V controlling voltage and 7% for 10V. This tuning range may have been improved by using alternative varactors to those used by the designers, but would still be limited due to the low-voltage operation required.

3) The semiconductor industry is reluctant to incorporate bondwire analog techniques as yield or reproducibility of the bonding process cannot be guaranteed.

2.2.6 Frequency Control Utilizing a Varied Coupling Structure

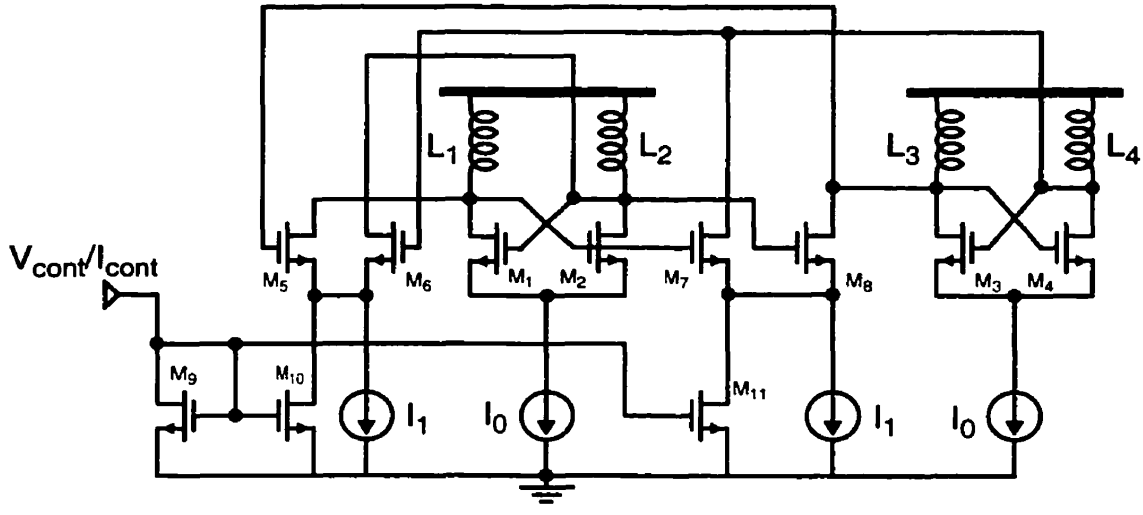

FIGURE 2.11 VCO utilizing varied coupling to achieve frequency tunability

The VCO shown in Figure 2.11 incorporates two fixed-frequency LC oscillators to generate a variable-frequency output through modulation of the coupling between the structures [Liu, '99]. To understand the operation of this design a signal flow graph can be constructed as shown in Figure 2.12. Each oscillator is modeled by a positive feedback loop, G_i where i=1,2.

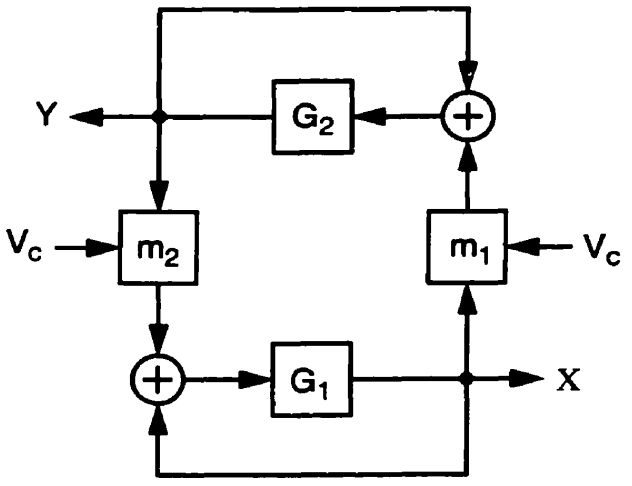

FIGURE 2.12 Signal Flow Diagram of Coupled Oscillators (G_1 and G_2)

In steady state operation and for both oscillators to lock to the same frequency, the following must hold:

$$(X + m_2 Y)G_1(j\omega) = X \tag{11}$$

$$(Y + m_1 X)G_2(j\omega) = Y\ , \tag{12}$$

where m_1 and m_2 are scalars and X and Y are the output phasors of the two oscillators. Assuming identical oscillators implies that G_1=G_2=G and m_1=-m_2=m, resulting in $X^2 + Y^2 = 0$, or $X = \pm jY$ (if m>0 and transistors are used to implement m_1 and m_2 => X = jY). This ensures that the coupled oscillator generates quadrature outputs, a property that is used in the work of this thesis. The oscillation frequency of the system can be determined by using these facts and either of the above equations:

$$(1 + jm)G(j\omega) = 1 \tag{13}$$

leading to two solutions:

$$\phi(Z(j\omega_1)) = -\text{atan}\, m \tag{14}$$

and

$$\phi(Z(j\omega_2)) = \text{atan}\, m \tag{15}$$

where $Z(j\omega)$ represents the tank impedance and the gain $G(j\omega)$ is proportional to this quantity. For a typical resonator, the magnitude of impedance peaks at a frequency higher than the resonant frequency:

$$f_o = \frac{1}{2\pi\sqrt{LC}}\sqrt{1 - \frac{CR_s^2}{L}}, \tag{16}$$

where R_s is the series, parasitic resistance of the tank inductor.

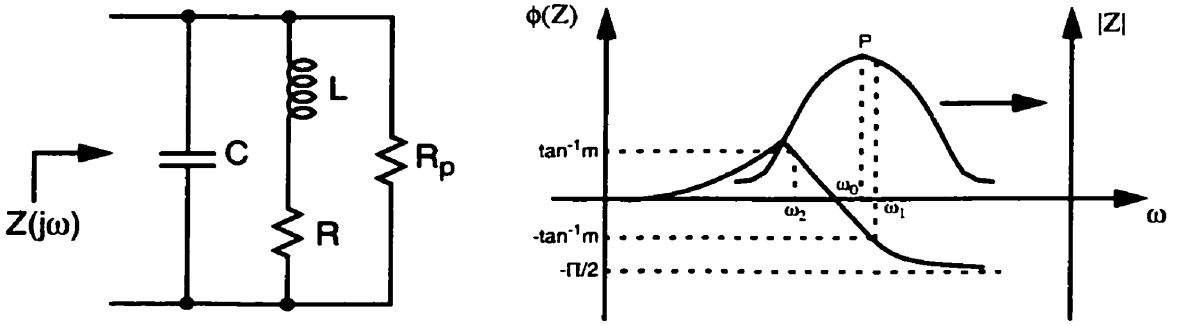

FIGURE 2.13 a) Resonator Impedance. b) Magnitude and Phase Response.

Only ω_1 is a valid solution (of (13)) as the loop gain is less than 1 for $\omega = \omega_2$ and therefore oscillation is not sustainable. By varying the coupling (m=0->1) between the oscillators it is possible to vary the output frequency from ω_o to ω_1. The upper bound of m is determined by the phase noise requirement for the oscillator application, whereas the lower bound of m is a function of the disparity between the two oscillator cores. The two oscillators will not be perfectly matched so if the coupling is not strong enough the output will be multi-toned. The coupling coefficient is the ratio of the differential transconductances, i.e. $\frac{G_{m_{5-6}}}{G_{m_{1-2}}}$ or $\frac{G_{m_{7-8}}}{G_{m_{3-4}}}$. With a constant current I_0 the coupling coefficient can be varied by altering the source current flowing in M_5 and M_6 as well as M_7 and M_8. This is achieved by including a control voltage and the transistors M_{10} and M_{11}. For a current controlled implementation an additional transistor M_9 is also included.

Conclusions:

1) The paper reviewed presents a method of varying oscillator frequency without utilizing varactors.

2) The design has lower power consumption (18mW), but the phase noise performance of the design is inferior to other designs that operate at similar or higher frequencies [Wang, '99], and the tuning range is not large enough to ensure that process variations are accounted for (16%). The design was fabricated in 0.35μm CMOS.

2.2.7 LC Ring Oscillator

The final topology considered is an experimental ring structure designed to improve phase noise performance [Kim, '00]. The basic concept of this design is to use a cascaded structure so as to implement a biquadratic bandpass filter structure. The authors claim that as the number of cascaded biquadfilters increases, the noise performance of the circuit will improve. This is due to the improved selectivity accorded to the increased order of the filter transfer function. If N identical oscillators are properly cascaded, the effect of noise filtering is realized and the output noise power will be reduced by a factor of N^2. However the number of noise sources will also be increased by a factor of N, leading to an increase by N of the output power noise density. The carrier signal at the resonant frequency is also amplified by a factor N, thereby increasing the signal power by N^2. Since the phase noise is defined as the ratio of noise per unit bandwidth to carrier power, the phase noise decreases by $10\log N^3$dBc/Hz.

There are numerous down sides to this approach:

1) The power consumption and chip area will also increase by a factor of N.

2) Despite the claims of improved phase noise performance, the results although impressive for a 0.6um design, are not vastly superior to those alternate approaches (by other researchers) presented in [Kim, '00].

3) The layout of such a structure is cumbersome as the inductors must be separated from each other by significant distances to prevent magnetic coupling of the signals of interest.

2.3 Phase Noise

Oscillators, like other analog circuits, are susceptible to noise. This noise may be from oscillator sources such as transistor noise and noise contribution from a lossy inductor, or it may be external, coming from voltage buffers or other external sources. Both the phase and the amplitude of the output waveform will be modulated detrimentally by this noise. In many cases the effect of amplitude noise is not as important; this is because the non-linear amplitude limiting mechanism will limit the amplitude variations. The focus in this section will be on phase noise, which manifests itself as a deviation of the zero crossing of the output waveform. Many designers refer to this phenomenon as oscillator 'jitter'.

Consider a periodic output $v(t) = A\cos(\omega_c t + \phi_n(t))$, where ϕ_n represents the random excess phase noise, which effects the zero crossings of the generated waveform. For $|\phi_n(t)| \ll 1\,rad$ we can rewrite v(t) as $v(t) \approx A\cos(\omega_c t) - A\phi_n(t)\sin(\omega_c t)$, that is, the spectrum of ϕ_n is translated to $\pm\omega_c$. Phase noise in RF applications is usually considered across the frequency spectrum of interest. For an ideal oscillator the spectrum will appear as in Figure 2.14 a), whereas for the real case the phase noise will manifest itself as a 'skirt' surrounding the desired carrier frequency, as in Figure 2.14 b).

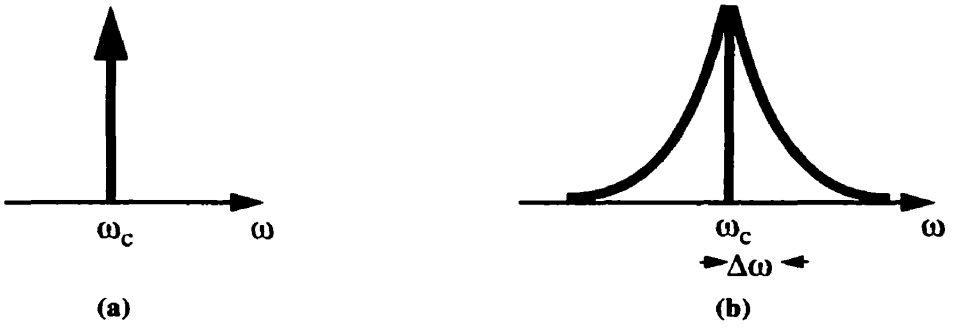

FIGURE 2.14 a) Output Spectrum of Ideal Oscillator. b) Spectrum of Actual Oscillator.

The standard way of quantifying the phase noise of an oscillator is to measure the noise power in a unit bandwidth at a distance $\Delta\omega$ from the carrier frequency and divide by the signal power of the carrier. The unit most commonly used is dBc/Hz.

2.3.1 Effect of Oscillator Phase Noise in Transceivers

To understand the effect that phase noise may have, we can consider the transceiver structure below. If the Local Oscillator contains phase noise, both the upconverted and down-converted signals will be corrupted.

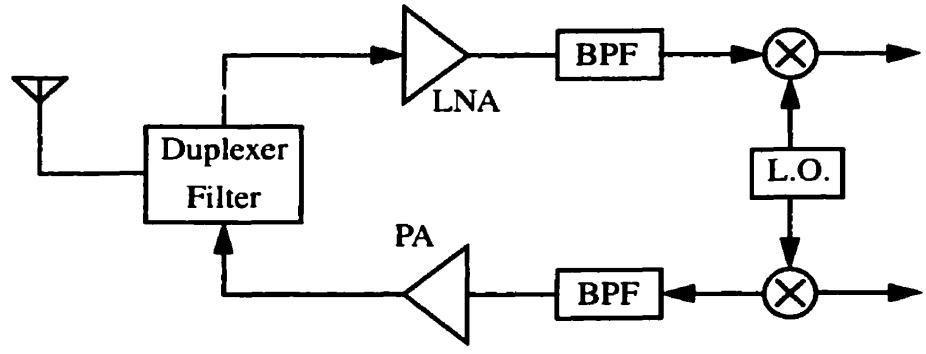

FIGURE 2.15 Generic Transceiver Front End.

In the ideal transceiver system, the oscillator translates the incoming signal to a different frequency with no loss of information or corruption of the incoming signal. In the non-ideal case, we can consider the impact of the phase noise skirt of the oscillator signal on the conversion of received signals. We can look at specific case, where both a wanted signal and an interfering signal are present at the antenna of the system. The spectra of the signals, as well as the spectra after conversion are shown in Figure 2.16. In this case the wanted signal has a smaller amplitude than the interferer. This may often be the case; for example, if the system in use is at the 'edge' of a wireless communications cell (with an interfering signal also present). If the phase noise is too large the mixed interfering signal could possibly swamp out the wanted signal and no useful information will be decoded by the system.

In order to retrieve a reasonable signal at the receiver, the LO must be extremely sharp. In IS-54, for example, the phase noise must be less than -115dBc/Hz at a 60kHz offset [Razavi, '98].

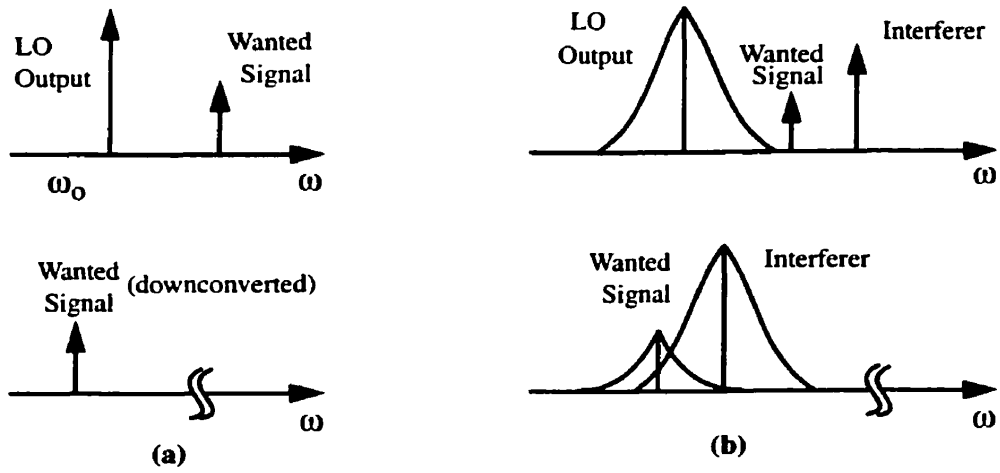

FIGURE 2.16 Downconversion by a) Ideal and b) Real Oscillators.

2.3.2 A General Phase Noise Theory

In this section some basic theory, developed by Thomas Lee and Ali Hajimiri, is presented for a LC oscillator [Lee, '00, Hajimiri '99, Hajimiri '98]. In particular there is a strong correlation between oscillator noise and power dissipation, the Q-factor of the tank, and noise sources within the circuit. First, a theory for an ideal oscillator (Figure 2.17) is developed, then the non-ideal case is considered where the energy restorer contains noise sources. The theory for the non-ideal case is thorough and exact, yet developing a practical design methodology based on it, as will be shown, is non-trivial.

Studying oscillators we will see that although the assumption of linearity may be defended, the noise analysis must be done under time-varying conditions. This contrasts with previously published theory that assumes a non-linear, time-invariant system. It may seem counter-intuitive to apply a linear analysis to an inherently non-linear system. It can, however, be easily shown that by applying a noise impulse to this system and measuring the output noise, that this output will be linearly related to the input (given the correct timing). Studying the impulse response of the system reveals that periodic time variations lead to frequency translation of device noise to produce the observed frequency response of LC oscillators. This developed theory is able to incorporate the noise sources in the circuit that have cyclostationary properties, i.e. their moments vary in time and are periodic.

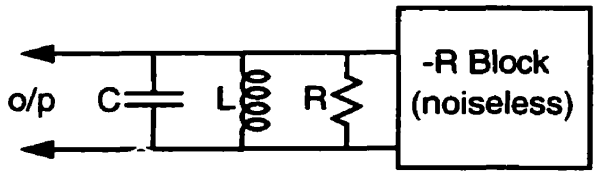

FIGURE 2.17 Quasi-Ideal Oscillator Implementation.

The circuit shown above models a lossy tank in parallel with an 'energy restorer', which is used to cancel the losses of the tank and ensure proper start up of the circuit. The only noisy circuit element is the tank loss modeled by a parallel resistance R. We desire a relationship between the noise generated by this element and the signal power of the circuit [Lee, '00]. The energy stored in the tank is:

$$E_{stored} = C\overline{V_{sig}^2} \quad , \tag{17}$$

where $\overline{V_{sig}^2}$ is the mean-square signal voltage and a sinusoidal waveform has been assumed. The total mean square noise voltage is found by integrating the resistor's thermal noise density over the noise bandwidth of the RLC resonator:

$$\overline{V_n^2} = 4kTR\int_0^\infty \left|\frac{Z(f)}{R}\right|^2 df = 4kTR\frac{1}{4RC} = \frac{kT}{C} \quad . \tag{18}$$

Combining equations we obtain a signal to noise ratio:

$$\frac{S}{N} = \frac{\overline{V_{sig}^2}}{\overline{V_n^2}} = \frac{E_{stored}}{kT} \quad . \tag{19}$$

It is now possible to incorporate power dissipation and resonator Q, by noting that Q is defined as the ratio of stored power to power dissipated by lossy elements of the tank;

$$Q = \frac{\omega E_{stored}}{P_{diss}} \quad , \tag{20}$$

implying

$$\frac{S}{N} = \frac{QP_{diss}}{\omega kT} . \tag{21}$$

We observe that the signal to noise ratio is proportional to tank quality as well as to the power consumed by the circuit. This gives an insight as to why RF designers remain focused on improving tank Q, and hence why there has been so much research into maximizing the quality of on-chip reactive elements [Long, '97; Niknejad, '98].

Phase Noise of an Ideal Oscillator.

Examining the tank in Figure 2.17, we note that the only source of noise in the oscillator is the tank conductance. This is because the realization of the energy restorer is assumed to be noiseless. This noise source can be modeled as a current source with mean squared noise current spectral density, $\frac{\overline{i_n^2}}{\Delta f} = 4kTG$.

This current noise can be converted to a voltage by multiplying this quantity by an equivalent tank impedance. Because the function of the energy restorer is to cancel the tank's conductance, the equivalent tank impedance at a frequency offset $\Delta\omega$, from resonance ω_O, is given by:

$$Z(\omega_O + \Delta\omega) \approx j\frac{\omega_O L}{2\frac{\Delta\omega}{\omega_O}} , \tag{22}$$

and utilizing the fact that $Q = \frac{1}{\omega_O GL}$ we modify equation 22:

$$|Z(\omega_O + \Delta\omega)| = \frac{1}{G}\frac{\omega_O}{2Q\Delta\omega} . \tag{23}$$

Thus, the spectral density of the mean-squared noise voltage (across the tank) is given by:

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f}|Z|^2 = 4kTR\left(\frac{\omega_O}{2Q\Delta\omega}\right)^2 . \tag{24}$$

This power density is dependent on frequency as the tank acts as a filter, the voltage response of such a tank falls of at a rate of 1/f, so therefore the power density will fall off with $1/f^2$ as displayed in equation 24. This (thermal) noise will affect both the phase and amplitude of the oscillator's output, but due to the inherent amplitude limiting of an LC oscillator any amplitude variations are considered to be insignificant and so are ignored. By the equipartition theorem of thermodynamics [Waterston-Maxwell], it is evident that both the phase and amplitude will be equally affected. This means that we can divide the result found above by two and, normalizing with respect to the mean-square carrier voltage, we arrive at:

$$L\{\Delta\omega\} = 10\log\left[\frac{2kT}{P_{sig}}\left(\frac{\omega_O}{2Q\Delta\omega}\right)^2\right] \quad , \tag{25}$$

known as the normalized single sideband noise spectral density. This phase noise will decrease with increasing signal power, as well as increasing Q. This intuitively makes sense as the thermal noise generated in the circuit is fixed and maximizing the Q narrows the bandwidth of the LC-tank.

There are many discrepancies between what is observed for a real oscillator and what is given by equation 25. Although any oscillator will possess a region where the observed noise density is proportional to $1/(\Delta\omega)^2$, the magnitude of the noise will be considerably greater. This is because any practical implementation of an energy restorer will introduce additional noise sources to the oscillator.

A real phase noise plot will eventually reach a 'noise floor', this may be because of the presence of external components, such as buffers, but may also be due to test equipment limitations. Finally, studying the noise plot for the real case, we will see that the noise initially falls at a rate proportional to $1/(\Delta\omega)^3$. These characteristics are shown in Figure 2.18.

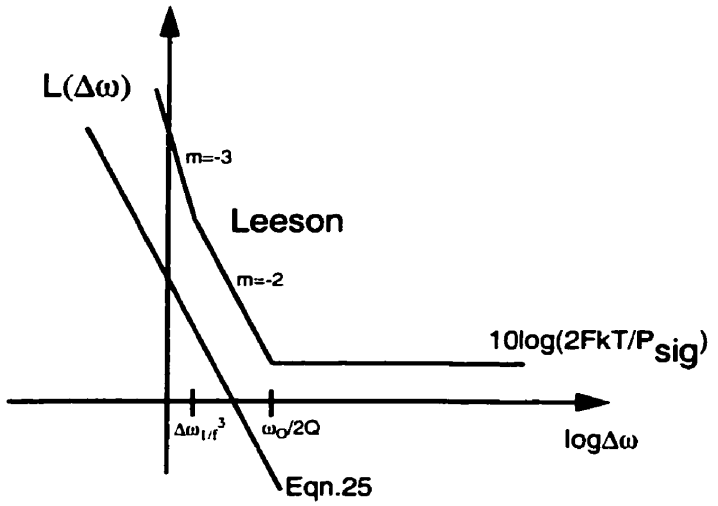

FIGURE 2.18 Phase Noise: Leeson's Formula verses that presented in equation 25.

A modification to equation 25 incorporates these discrepancies:

$$L\{\omega\} = 10\log\left[\frac{2FkT}{P_{sig}}\left\{1+\left(\frac{\omega_O}{2Q\Delta\omega}\right)^2\right\}\left(1+\frac{\Delta\omega_{\frac{1}{f^3}}}{|\Delta\omega|}\right)\right] \quad . \tag{26}$$

This alteration due to Leeson includes a factor F to account for the increased noise in the $1/\Delta\omega^2$ region, an additional factor of unity to incorporate the observed noise floor, and finally a term in the second set of parentheses to provide a $1/\Delta\omega^3$ at small offsets from the carrier frequency. Both the Leeson factor F and $\Delta\omega_{1/f}{}^3$ are empirically determined quantities. The downside to this theory is that designers without any knowledge of where F comes from, may try to increase oscillator Q by the use of an active circuit. This approach would not work, as F will be altered and the phase noise performance may degrade. So Leeson's approach although accurate does not give the phase-noise insight that we desire.

A Linear, Time Varying Phase-Noise Theory.

The theory presented so far assumes a linear, time-invariant relationship between the input noise injected into the oscillator and the resulting output phase noise. Although the linearity can be defended both theoretically and by experiment, the same is not true for time-invariance. This is because linear time-invariant systems can not perform frequency translations. Many publications have tried to present a non-linear, time-invariant mixing theory to explain the noise behaviors of oscillators. This approach is problematic, as the amplitude of the sidebands generated would depend non-linearly on the input signal, and this is not what is observed. This section will show that it is necessary to assume a linear, time-variant system. Although the active devices in any oscillator behave in a non-linear fashion, we are not linearizing their operation, but rather we are linearizing around a steady state solution of the system. In other words, we do not assume that all the variables that describe the operation of such a circuit are linearly related, but we will assume that the resulting output noise is linearly related to any injected device noise.

To show that time-invariance does not hold, it is possible to consider the response of a lossless LC tank to an injected current pulse. The system is oscillating at a given frequency and a pulse is injected at time τ, as shown in Figure 2.19.

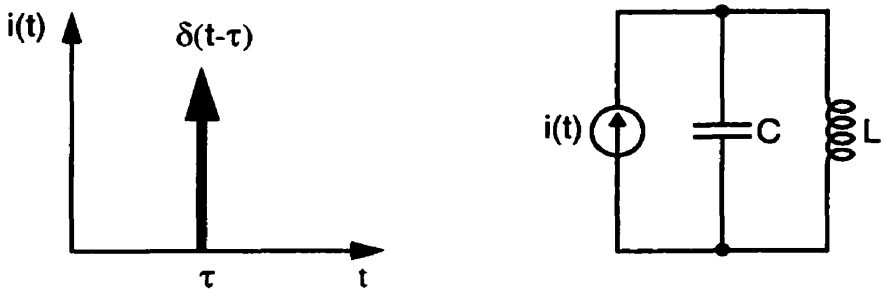

FIGURE 2.19 LC Tank excited by a pulse.

If the impulse occurs when the output of the tank is at its maximum, the amplitude increases but the phase will be unaltered. If the pulse is injected at any other time, both the amplitude and phase of the output will be changed. Both instances are shown in Figure 2.20.

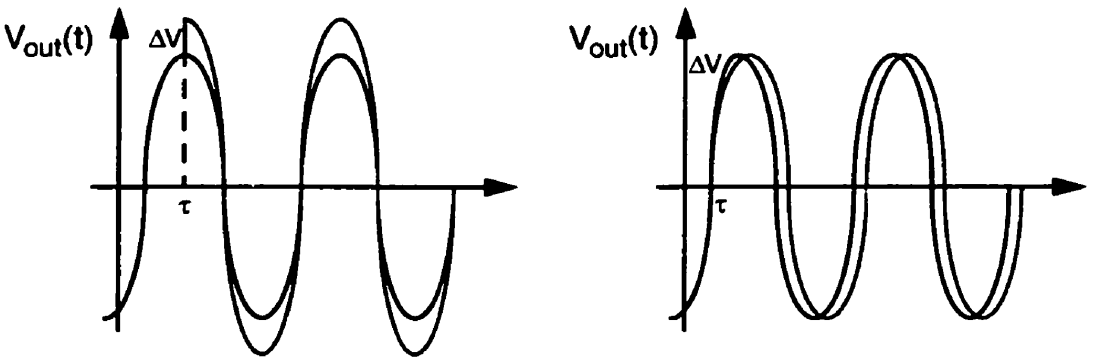

FIGURE 2.20 Impulse Responses of a LC Tank.

Therefore, an impulsive input produces a step change in phase:

$$h_{\phi}(t,\tau) = \frac{\Gamma(\omega_O \tau)}{q_{max}} u(t-\tau) \ , \tag{27}$$

where u(t) is the unit step function. Γ(x) is called the impulse sensitivity function (ISF) and is a dimensionless frequency and amplitude independent function periodic in 2π. Dividing by q_{max}, the maximum charge displacement across the capacitor, makes the function Γ(x) independent of signal amplitude. Figure 2.21 shows that this function is a time-varying measure of the sensitivity of the oscillator to an input impulse.

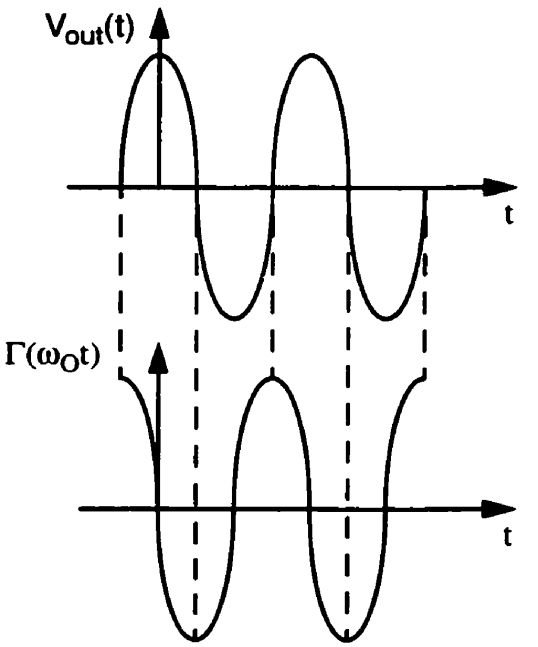

FIGURE 2.21 ISF for an LC Oscillator.

$\Gamma(x)$ has its maximum value at the zero crossings of the output. $\Gamma(x)$ can be found analytically, but it is generally easier to find this useful function by simulation. Once the ISF has been determined, it is possible to calculate the excess phase:

$$\phi(t) = \int_{-\infty}^{\infty} h_{\phi}(t,\tau) i(\tau) d\tau = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\omega_O \tau) i(\tau) d\tau \quad . \tag{28}$$

where $i(\tau)$ is the normalized noise current. Because the ISF is periodic, it can be expressed as a Fourier Series:

$$\Gamma(\omega_O t) = \frac{c_O}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_O t + \theta_n) , \tag{29}$$

where the coefficients c_n are real and θ_n is the phase of the nth harmonic of the ISF. If we assume that the noise components are uncorrelated, we can neglect the effect of θ_n. The series typically converges rapidly, so that only the first terms of the series become relevant and the phase is given by:

$$\phi(t) = \frac{1}{q_{max}} \left[\frac{c_O}{2} \int_{-\infty}^{t} i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau) \cos(n\omega_O \tau) d\tau \right] . \tag{30}$$

This equation allows for the calculation of the excess phase of the output, once the Fourier coefficients of the ISF have been computed. The normalized noise current is an RF signal, whose various components across the frequency spectrum undergo up and downconversions resulting in the observed noise skirt. It is clear that minimizing the coefficients c_n will minimize the phase noise, this can be illustrated further by considering Parseval's Theorem:

$$\sum_{n=0}^{\infty} c_n^2 = \frac{1}{\pi} \int_0^{2\pi} |\Gamma(x)|^2 dx \quad . \tag{31}$$

The ISF is a function of the oscillator waveform, and hence potentially under the control of the designer.

Another powerful property of the LTV theory presented is that it is able to accommodate cyclostationary noise sources. This is of great importance, as the current noise from any active device in an oscillator will be a cyclostationary process. This is hardly surprising as the noise current of an active device is a function of its biasing, and in this case the bias current is varying periodically.

2.3.3 Conclusions

Having reviewed some fundamental (albeit recent) phase noise theory [Lee, '00; Hajimiri, '99; Hajimiri, '98], it is possible to identify some key design criteria for an LC oscillator. The LTI model illustrates the importance of tank quality and signal power; both need to be maximized to improve oscillator performance. Deeper insights are provided by the LTV theory and these illuminate the most effective operation of the energy restorer, in order to minimize the phase noise: an active device(s) must be present in order to implement the energy restorer required. This transistor will inject noise into the circuit. In order to minimize this effect, it is necessary to determine the ISF of the circuit. The ISF illustrates the sensitive and insensitive points in the oscillator's cycle. There are many ways that the active device can deliver energy to the tank, but it is preferable to design the circuit such that this power is delivered at an 'insensitive' part of the cycle and preferably all at once. For an ideal oscillator the transistors would remain off most of the time, only delivering energy, in the form of a current pulse, at the signal peak(s) of each cycle. A way to develop a design methodology to ensure this for a real oscillator is not obvious. Thomas Lee and Ali Hajimiri have managed to demonstrate, through both simulation and fabrication, that by implementing a symmetrical negative resistance oscillator with appropriate transistor sizing, as shown in Figure 2.22, that the dc value of the ISF (Γ_{DC}) can be minimized. This procedure minimizes the upconversion of 1/f noise. By exploiting this symmetry, they have managed to reduce the $1/f^3$ corner to its minimum value for this architecture. The phase noise results presented are impressive: -121dBc/Hz at a frequency offset of 600kHz from the main carrier frequency (1.8GHz).

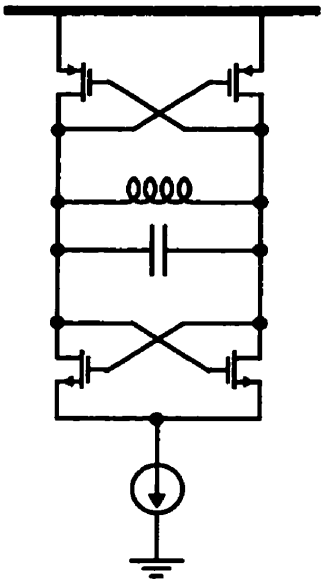

FIGURE 2.22 Differential, 'Symmetric' LC Oscillator.

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Chapter 3

Circuit Design

As discussed in Chapters 1 and 2, it is imperative for a LC oscillator to have a wide enough tuning range to ensure that any process variations can be tuned out as well as in certain cases to facilitate channel selection. The work of this thesis is focused on the implementation of an LC oscillator with a wide tuning range. Ring oscillators can be designed with large tuning ranges and low power dissipation, but they suffer from poor phase noise performance. LC oscillators have better phase noise properties, but historically there has been a problem with implementing a wide tuning range CMOS LC oscillator. The reasons for this will be discussed in this chapter, as well as a way of circumventing this issue.

3.1 Hybrid Tuning with Hysteresis

We are aware that a large tuning range is an essential oscillator design requirement. There is a dichotomy in this: if the VCO has a large tuning range, any random fluctuations on its control terminal will result in large modulations of the output frequency. This induced phase noise can be reduced by decreasing the VCO modulation index, K_v (Hz/V). One method of achieving this, without losing the tuning range needed, is to employ a hybrid analog-digital tuning scheme [Kral, '98]. There are a number of methods that could be used to implement this staggering, such as using a varactor with dual control. In this work it is achieved by switching one of a number of capacitors into or out of a reactive tank, with a varactor being continuously tuned by an analog voltage. The resulting tuning characteristic is illustrated in Figure 3.1, with overlapping staggered VCO characteristics. This staggering technique is employed to minimize the switching of the capacitors and the jitter that may result as a consequence of this switching. The example shown in Figure 3.1 utilizes three switched capacitors, where as the final design uses six.

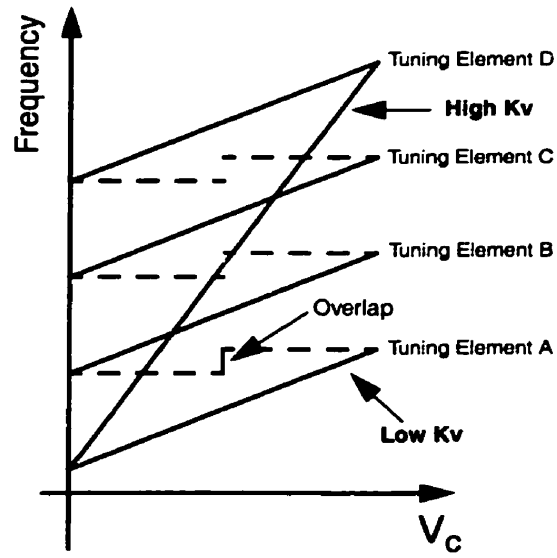

FIGURE 3.1 Hybrid Analog-Digital Tuning Characteristic (with Hysteresis).

3.2 Tank Losses

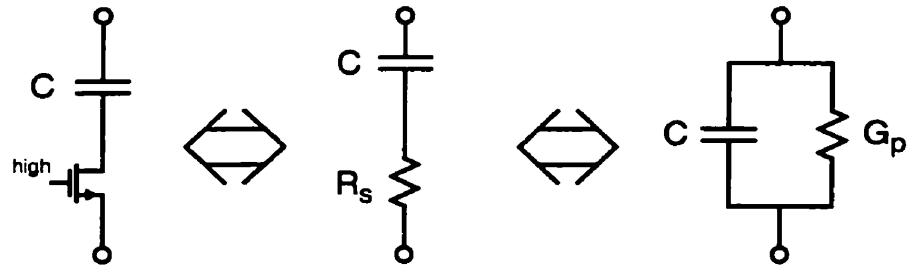

FIGURE 3.2 Losses incurred by using MOS Switch.

In order for oscillations to be sustained, it is essential that the negative admittance, generated by the cross-coupled pair, exceeds the total loss within the circuit. The main source of loss in a switched tuning scheme oscillator are the losses associated with the inductor, varactor losses, as well as the loss due to the finite on-resistance of the switches used to help implement a coarse tuning scheme. Figure 3.2 displays one way in which we can consider the parallel loss incurred by using a switch, where:

$$G_p = R_s(\omega_O C)^2, \tag{32}$$

and R_S is the series resistance of the switch.

One method of minimizing the switch resistance is to use large switching transistors. The downside to this approach is that the parasitic switch capacitance will increase, and the tuning scheme often becomes more difficult to implement.

3.3 Passive Boosting of $-G_m$

In order to ensure a wide tuning range, we could increase the $-G_m$ of the circuit by boosting the sizes of the transistors, or increasing their bias currents. The first technique will increase the capacitive loading on the tank, and therefore reduce the oscillation frequency. The latter must be avoided as low power consumption is of great importance. The novel idea implemented in this work is to use an on-chip transformer for the specific purpose of maximizing the tuning range.

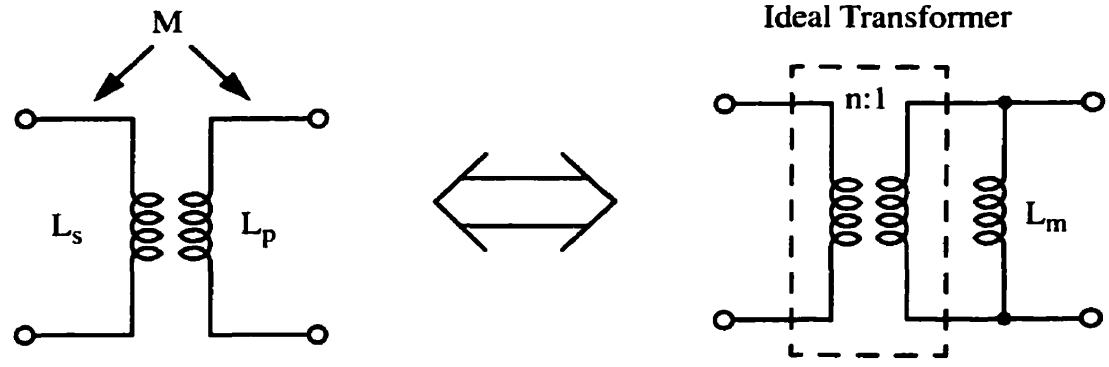

FIGURE 3.3 Equivalence of Mutually Coupled Coils to Transformer and Magnetizing Inductance.

Two mutually coupled coils are equivalent to an ideal transformer in parallel with an inductance (Figure 3.3), this inductance is often referred to as the magnetizing inductance. The magnetizing inductance is given by: $L_m=L_p$, and the transformer turns ratio is given by: $n=M/L_p$ or $n^2=L_s/L_p$ $(n>1)$. Thus the transformer can be used as an admittance booster, with $-G_m$ across the secondary getting boosted to $-n^2G_m$, on the primary. L_m provides the inductance needed to resonate with the selected tank capacitance. This means we have managed to increase the negative admittance required without compromising power or transistor sizes. The full benefits of using a transformer instead of an inductor, specifically an inductor of value L_s, are laid out in detail in Chapter 5.

3.4 Quadrature Signal Generation

There are three popular methods of producing quadrature signals, which are essential for many telecommunication transceivers. They are: RC poly-phase filtering, frequency division-by-2, and direct quadrature oscillation.

RC polyphase filters can be used to generate I and Q signals from a single phase input [Galal,'00]. They generate accurate quadrature signals over a given band, but for a multi-band transceiver, multiple, or cascaded, filters would be required. They require large areas of silicon to implement, add to the tank capacitance, and contribute circuit noise due to the resistors used to implement the filter.

Frequency divide-by-2 circuits use less area than their RC polyphase filters counterparts, and can be used to generate reasonably accurate I and Q signals ($<1^{o}$) over their entire operating range [Maligeorgos,'01]. In order to generate quadrature signals at f_O, it would be necessary to design an oscillator, with a centre frequency of $2f_O$. Equation 21 in chapter 2 illustrates that the S/N performance of an LC oscillator is inversely proportional to f, so that an alternative technique is preferred.

This work implements direct quadrature oscillation by cross-coupling two identical LC oscillators in the appropriate fashion [Millar, '34; Rofougaran,'96]. If we examine Figure 3.4, we notice that we have two identical oscillators: assuming the drain of M_1 is at 0^{o} and the drain of M_2 is at -180^{o}, transistors M_5-M_8 act as inverters forcing 90 degree phase shifts between their inputs (gate) and outputs (drain). Hence this circuit produces two differential outputs, one being phase shifted from the other by 90^{o}. In other words, the oscillator is a type of ring oscillator -- the oscillation frequency is determined by the resonant frequency of the tank as well as the level of coupling that exists between the oscillator cores.

M_1-M_4 are sized at 60/0.18 μm. M_5-M_8 have W/L of 30/0.18 μm, this ensures that the coupling between the two negative Gm cells is strong enough to prevent the outputs from being multi-toned. The tank circuit is shown in Figure 3.5.

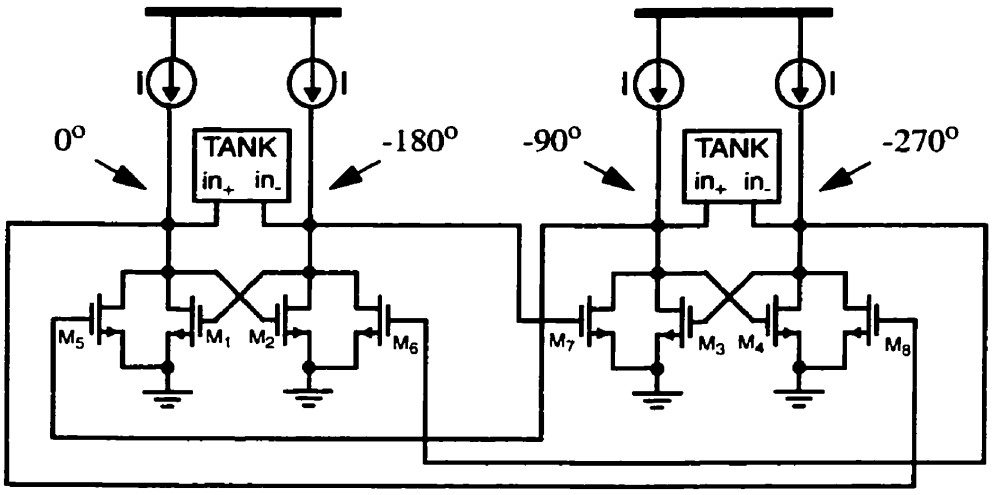

FIGURE 3.4 Coupled Quadrature Oscillator.

3.5 Tank Design

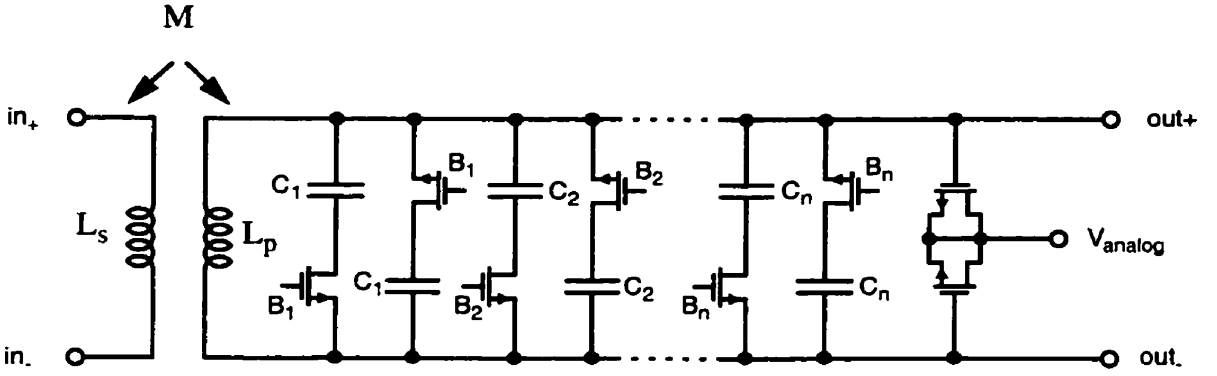

FIGURE 3.5 Tank Circuit containing Switchable Fixed Capacitors and Varactor.

For the above tank, n was chosen to be 6. In other words there are 12 capacitors, switched by a six bit digital word. The analog tuning is made possible by two NMOS varactors, sized at 12μm*12μm. The transistors used to implement the switches are sized at 40/0.18, they have a nominal on-resistance of 15Ω and a nominal drain-source capacitance of 42fF when switched off.

3.5.1 Capacitor Selection

The tank elements of the first design submitted for fabrication were chosen so as to achieve a staggered tuning range from 2GHz to 3GHz. The capacitors for the first design were weighted as follows: $C_6=C_5=2C_4=4C_3=8C_2=16C_1$, where C_1=50fF.

3.5.2 Varactor Design

For minimizing substrate noise injected into the circuit it is preferable to use PMOS varactors. This is because the 'channel' is isolated from the substrate, and is therefore less prone to interference due to substrate noise. The reasons for choosing NMOS over PMOS, in spite of the latter's superior noise performance, are explained in this section.

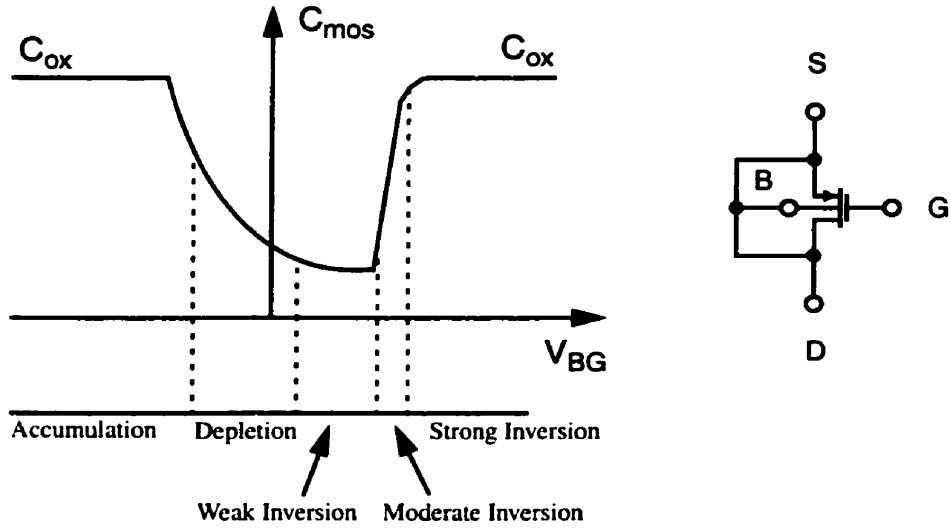

FIGURE 3.6 Tuning Characteristics of a PMOS capacitor with Bulk shorted to Drain and Source.

Above is the tuning characteristic of a PMOS capacitor [Andreani, '00]; this illustration is very useful when designing for a variable capacitance such that the bulk-gate voltage is a small-signal. It is then possible to bias the transistor such that maximum varied capacitance is ensured (i.e. by biasing the device such that its operating point is at the centre of the 'moderate inversion' operating range).

If the signal is 'large', as is the case for a VCO, the tuning capability is restricted due to the non-monotonic nature of the device's tuning characteristic. Reconnecting the device such that the bulk is connected to V_{DD}, with the drain and source remaining shorted, ensures that the device does not enter the accumulation mode for any value of V_{sg}. Although the resulting characteristic, Figure 3.7, is not monotonic, it is closer than the previous structure, thus making it easier to account for analog tuning.

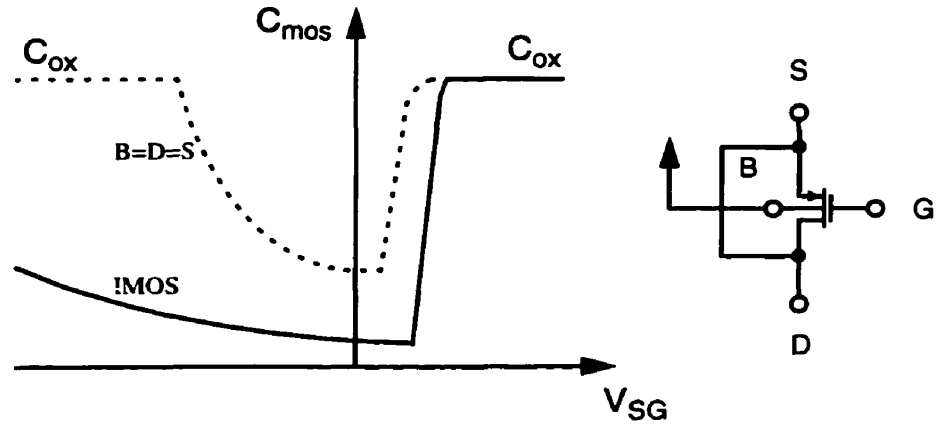

FIGURE 3.7 Tuning Characteristic for the inversion mode capacitor (IMOS) [Andreani, '00].

The final VCO design utilizes this IMOS tuning characteristic, although a NMOS varactor has been used instead. There are two reasons for this choice. First of all, a NMOS implementation has a lower parasitic channel resistance than the PMOS transistor. Additionally, if the PMOS varactor had been chosen, maximum varied capacitance and proper buffer operation could not have been ensured.

It would have been possible for the circuit topology chosen to use an accumulation mode MOS varactor. This device, as its name would suggest, is restricted to operation in the accumulation-mode, and has the added benefit of having a lower series resistance than its inversion-mode counterpart. This mode of operation is ensured by replacing the p+ source and drain diffusions with n+ 'Bulk' diffusions, as shown in the diagram below [Andreani, '00].

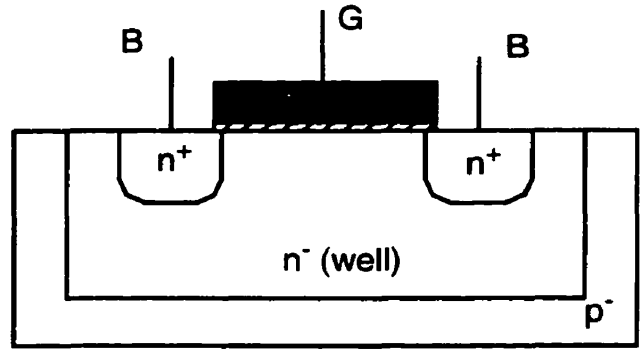

FIGURE 3.8 Accumulation-Mode MOS Varactor.

Although this device exhibits superior performance to conventional NMOS or PMOS varactors, it is not characterized or supported by silicon foundries, therefore proving very difficult to simulate. In order to model this device properly it would have been necessary to lay out numerous test structures; the time constraints of this work did not allow for this approach.

3.5.3 Transformer Selection

Monolithic transformers have received increasing attention in recent years. They can be effectively used in RF circuits to achieve feedback, matching, and inter-stage coupling. In this work we are interested in coupling a negative G_m cell to a resonant tank.

There are some downsides to implementing a transformer on silicon. The Q-factor of each of the coils used to make up the structure is lower than off-chip inductive structures. This problem is two-fold, the top metal-layer in any CMOS structure has a low conductivity and the resistivity of the substrate is low. GaAs which remains a popular technology for RF circuits has many more options available to the designer. It is quite common to have a top metal layer with superior conductivity, such as gold or copper. It also has a semi-insulating or insulating substrate, which lends itself to the implementation of higher quality resonant structures, as the current losses due to the substrate are lower than in the Si case.

Parasitic capacitance of such a structure must also be taken into account by the designer. As well as accurately modeling the losses of the structure and its deviation from maximized coupling, the parasitic capacitance associated with the transformer dictates the maximum frequency at which the transformer is useful.

There are a number of ways in which an on-chip transformer can be laid out. Four common structures will be discussed: the Shibata (parallel conductor) winding [Shibata, '81], the Frlan (interwound) winding [Frlan, '89], the Finlay (overlay) winding [Finlay, '85] and the concentric spiral winding [Mohan, '98]. All four structures are displayed in Figure 9, note that the case of a 1:1 turns ratio is considered.

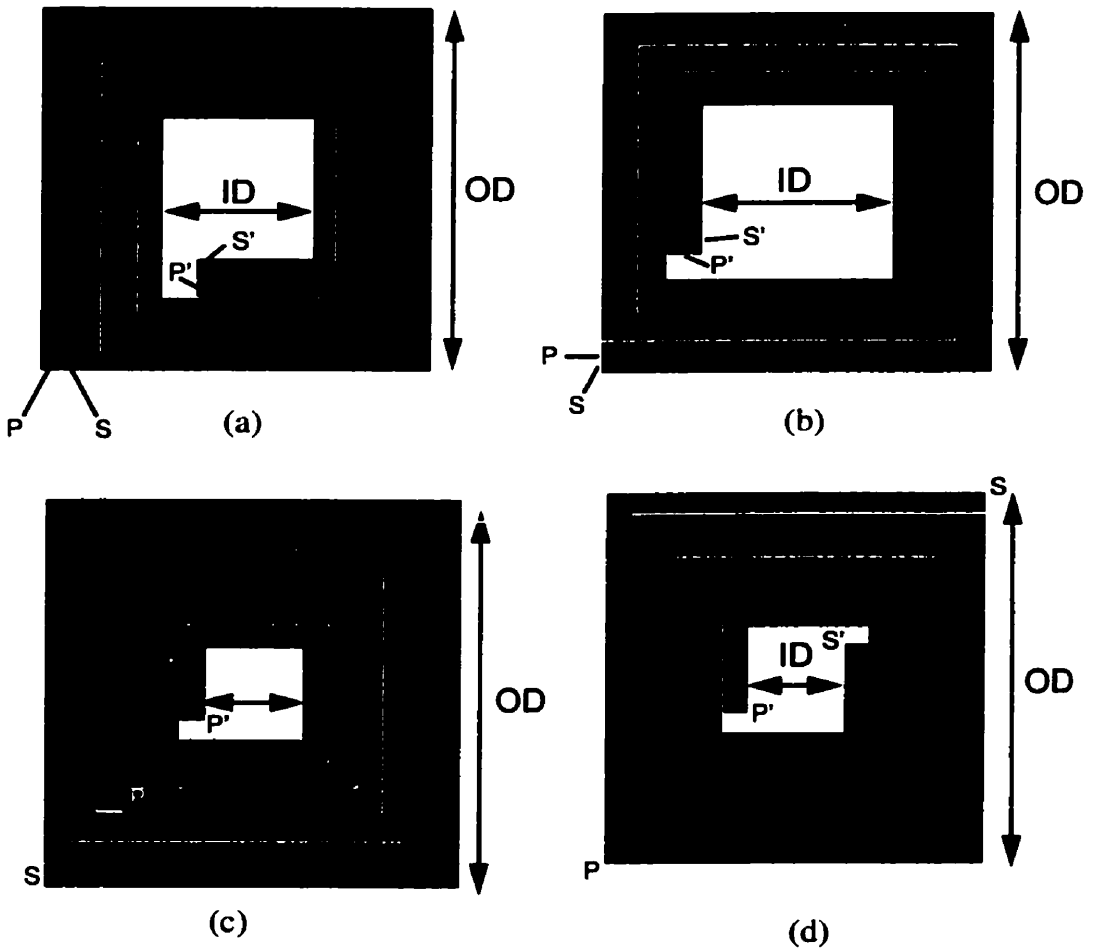

FIGURE 3.9 Transformer Winding Configurations [Long, '00], (a) Shibata Winding, (b) Finlay Winding, (c) Concentric Spiral Winding, (d) Frlan Winding.

As discussed in **3.3:** $M = \sqrt{L_p L_s}$, for the case of an ideal transformer. For a real transformer the coupling between the coils is non-ideal. The measure of coupling-imperfection is known as the k-factor: $k_m = \frac{M}{\sqrt{L_p L_s}}$. So for an ideal transformer k_m is unity and for two uncoupled coils k_m=0. As the magnetic properties of the materials used to make a Si chip are similar to those of air, the confinement of the magnetic field is weak. But it is still possible to realize k-factors as high as 0.9 for on-chip implementations [Long, '00].

The Shibata coupler shown in Figure 9(a) consists of two (top-metal) inductors that are interwound to promote magnetic coupling. As far as the designers are concerned, the dis-

advantages of this coupler are two-fold: although both coils have the same number of turns (N_t=3), they are of different lengths and therefore have different inductances, implying that the turns ratio is not 1:1 as desired. The primary and secondary terminals are in the same location, which may make connecting other circuitry complex.

The Finlay or overlay winding is, as its name suggests, two overlaid identical coils. This reduces the area required by the structure, even though the conductivity of the lower metal will typically be lower than the top metal. This is not the only asymmetry associated with this coupler as the top metal layer is insulated from the substrate because of the underlying metal. This means that the metal-substrate capacitances differ for each coil; therefore the designer must ensure that this configuration is appropriate for their application. The parasitic reactances associated with this transformer are higher than the others considered, implying that the maximum useful frequency is lower. This structure does, however, exhibit a very high k-factor of about 0.9.

A concentric spiral winding transformer as shown in Figure 9(c) has a common periphery that is limited to a single turn, this means that the k-factor is low (~ 0.6). Additionally, the primary inductance and secondary inductance differ greatly in size due to their mismatch in length.

Finally, we will consider the Frlan winding, which has two identical interwound coils. This aspect ensures that the electrical characteristics of both primary and secondary are also identical when they have the same number of turns. Another advantage is that the primary and secondary connections are located on opposite sides of the transformer, facilitating connection to circuitry. The Frlan transformer was used in this work.

There are additional transformer designs that were considered [Cheung, '98], that have not been discussed in this thesis.

3.5.4 Transformer Design and Simulation

Hewlett Packard's Advanced Design System was used to both simulate and help model the transformer used in this work. Various transformer designs were laid out and simulated in Momentum, with process parameters for TSMC's (Taiwan Semiconductor Manufacturing Corporation) 0.18um CMOS process being utilized. The final transformer design is shown in Figure 3.10. It has a 1:2 step up ratio between primary and secondary (n=2), which was realized by partitioning the primary into two separate turns rather than one continuous winding. The separate windings were then connected in parallel to implement the 1:2 transformer. The outer dimension of this final design is 300um, the line spacing was chosen to be 1um, the metal width is 10um and the inner dimension works out to be 126um which allows ample space to allow the magnetic flux to pass through the centre of the coils.

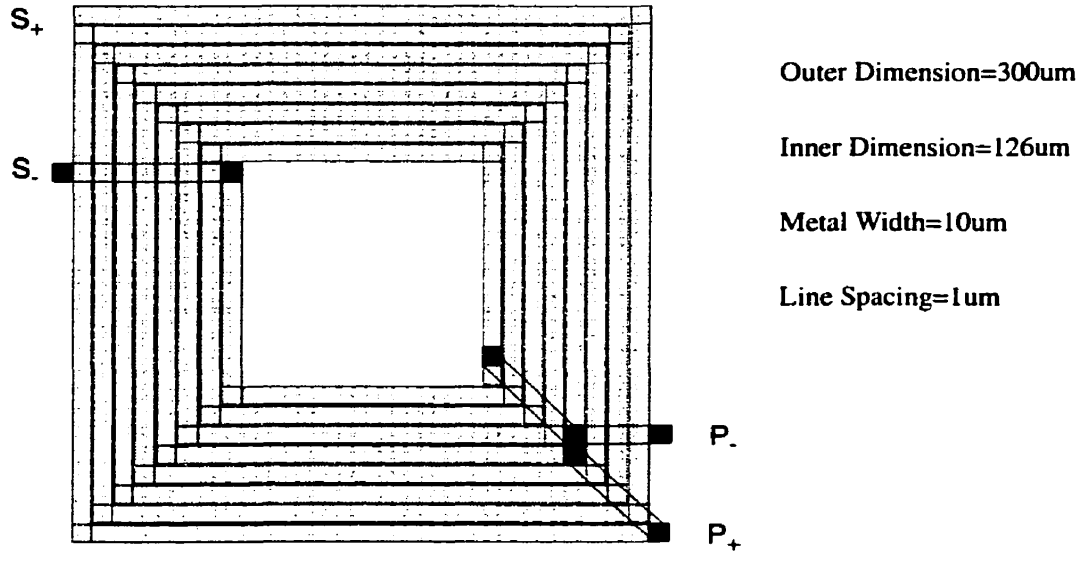

FIGURE 3.10 Transformer used in Oscillator Tank.

There are two popular methods of modeling an on-chip transformer. The first is to model each conducting length separately and then combine all these models together. If we consider two strips of metal in the transformer as shown in Figure 3.11, i.e. a simple two conductor transformer, each strip of metal has an associated series inductance (with finite Q), a parasitic impedance to ground (which models parasitic capacitances and substrate losses). The mutual coupling that occurs between the conductors, on both a magnetic (M)

and electrical (C_m) level, must also be incorporated. Each strip within the designed transformer can be modeled separately, taking into account the coupling between it and its adjacent conductors. Once all the models are complete, they can be combined to produce a comprehensive transformer model.

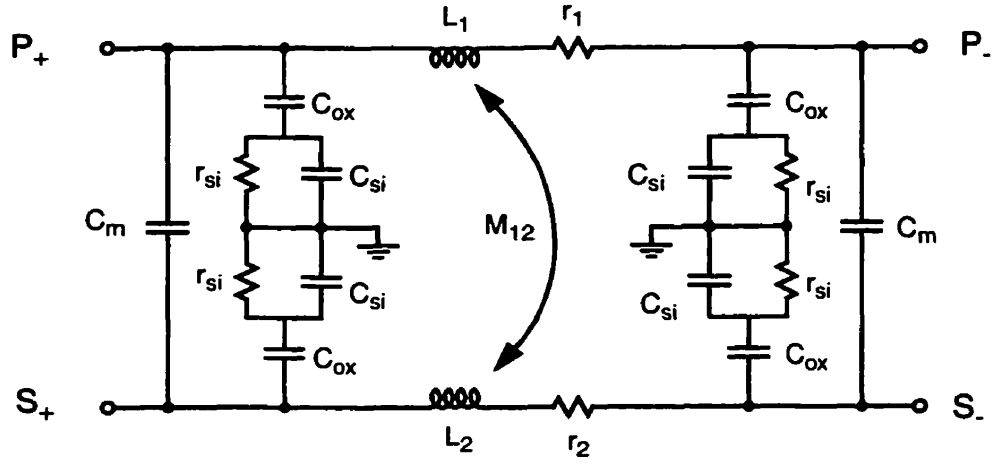

FIGURE 3.11 Model for Simple Two-Conductor Transformer.

As any real transformer is by its nature a distributed structure, this procedure is very accurate. It is, however, an involved process to determine all of the electrical parameters within this structure.

The second approach is to produce a compact model for the entire structure, as shown in Figure 3.12.

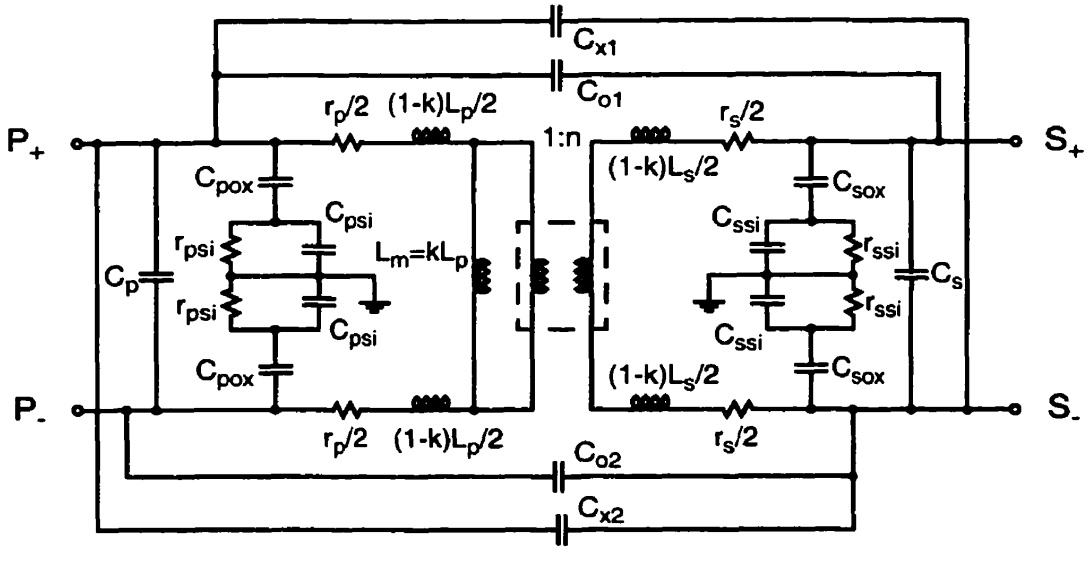

FIGURE 3.12 1:n transformer compact model.

Although this approach is less exacting, it allows for easier hand calculations, and is a more intuitive way of understanding the operation of an on-chip transformer.

As illustrated in Figure 3.3, two mutually coupled coils are equivalent to a 'magnetizing' inductance in parallel with either the primary or secondary of an ideal transformer. The compact model assumes two ideally mutually-coupled coils at the centre of the model; the model is then completed by factoring in transformer parasitics and non-idealities. The 'parasitic' primary and secondary inductances ($(1-k)L_p$ and $(1-k)L_s$) are used to model the imperfections in the magnetic coupling of the coils -- they account for the fact that k is not equal to one. In this example, the magnetizing inductance L_m is modeled as k times the inductance of the primary coil. The parasitic capacitances that occur between each of the four transformer terminals are modeled by C_x, C_o, C_s and C_p. The parasitic capacitances due to the oxide dielectric and the low resistivity substrate are approximated by C_{ox} and C_{si}.

Finally, r_p, r_s, and r_{si} are included to model losses that occur in a real transformer. All three of these parameters are frequency dependent. The first two are so because they model the losses generated by the skin effect, as well as those due to the DC resistance of the coils. r_{si} models the loss currents that are generated in the low-resistivity substrate, which become more pronounced with increasing frequency.

Each element value of the compact model for the transformer used in this work is listed in the table below (using Figure 3.12, note that n=0.5), this model is valid over the range 2-3GHz:

TABLE 3.1. Element Values for Compact Model (Valid from 2-3GHz)

	(fF)		(fF)		(nH)		(Ω)
C_p	4.4	C_{x1}	70.5	L_m	3.94	r_p	14.9
C_{pox}	110.5	C_{x2}	70.5	L_p	1.16	r_{psi}	440
C_{psi}	388.5	C_{o1}	100	L_s	0.28	r_s	3.2
C_s	0.6	C_{o2}	100			r_{si}	754.1
C_{sox}	182.9						
C_{ssi}	306.6						

3.5.5 Differential Verses Single-Ended

The final design uses the tank in a differential fashion (Figure 3.4). It can be shown that driving an on-chip inductor differentially results in a higher Q-factor and broader bandwidth than the single-ended case [Danesh, '98]. If we consider a possible microstrip model, where the parasitics to ground (as shown in Figure 3.11) are simplified from three elements C_{ox}, C_{si} and r_{si} to two elements, C_p and r_p, then the resulting model used is shown in Fig. 13 a), with the single-ended excitation case being shown in 13 b), and the differential case in 13 c).

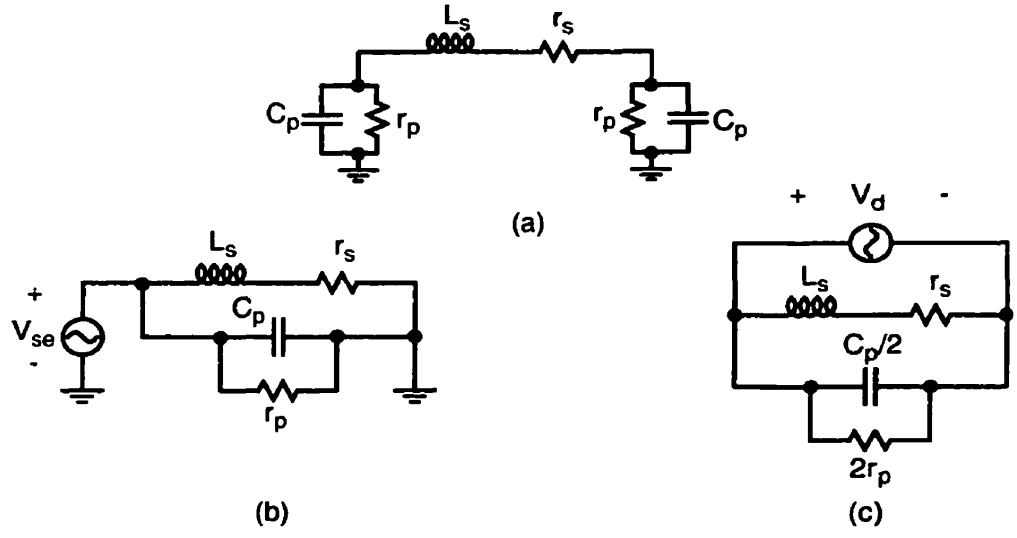

FIGURE 3.13 a) Model for Microstrip line, b) Single-Ended Model, and c) Differential Model [Long,'00].

Figure 3.13 illustrates that the impedance across the inductor in the differential case is twice that of the single-ended case. Both impedances are approximately the same at low frequencies. However with increasing frequencies, the ratio of the reactive part of this impedance to its real part is greater for the differential case. This implies that a higher Q-factor results from driving an inductive element differentially. A wider operating bandwidth is another plus side to the differential approach.

3.5.6 High Frequency Response & Transformer Tuning

The upper frequency limit of a transformer may be defined by the self-resonant frequency; this is the frequency at which the parasitic capacitances of both transformer coils resonate

with their associated inductances. The reactance looking into either the primary or the secondary beyond this frequency limit is capacitive.

The term 'Transformer Tuning' is normally associated with modifying the impedances of both primary and secondary coils, in a parallel fashion, in order to reduce the losses between input and output ports [Long, '00; Cheung, '98]. This is achieved by adding capacitance to the primary or secondary, i.e. by increasing C_p and/or C_s (Figure 3.12). The two ports become matched when the total admittance, shunted with the internal transformer, becomes resonant with L_m, the magnetizing inductance. This tuning, as we would expect, decreases the operating range of the transformer.

The tuning that takes place in this work is different than that described in other research publications [Long, '00; Cheung, '98]. This work intentionally modifies the resonant frequency of the transformer, by either modifying the gate-source voltage of a varactor or by switching in one of six fixed capacitors. The highest oscillation frequency of the oscillator is set by the magnetizing inductance, L_m, in conjunction with the parasitics of both the transformer and the oscillator's transistors. The lowest frequency is set when all switches are on and the varactor is tuned such that its gate-channel capacitance is at its maximum.

Some simulated plots are included for the transformer with reference to 50Ω ports. Although the transformer is a differential device, a simple testbench was utilized to simulate in a single-ended fashion. This allows for generation of easily understandable transformer scattering-parameters. The reflection coefficients for both ports are shown over the range DC to 10GHz (S_{11} and S_{22}). From these two plots it is observed that the primary coil has the larger inductance. The forward transmission of power from port 1 to port 2 (S_{21}) is also shown over the same frequency range. We note that S_{21} reaches its optimum value of approximately -5dB over the transformer passband, but this is for the single-ended case. As was discussed in **3.5.5**, driving the device differentially, as was done in this work, will improve tank performance.

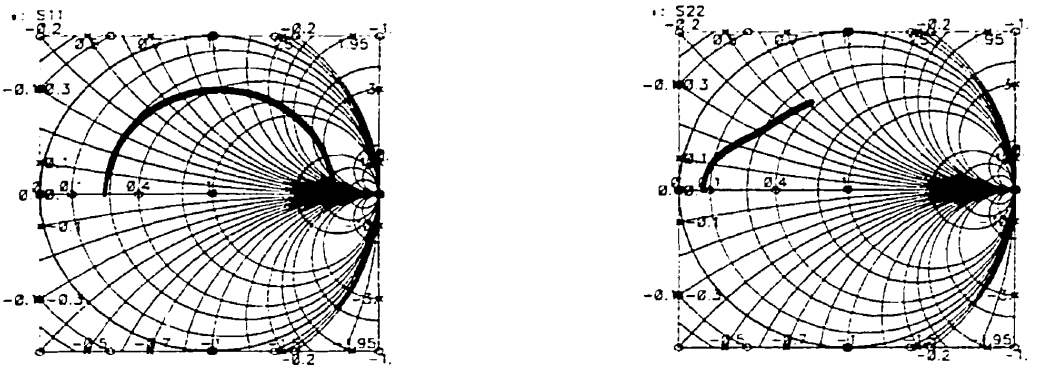

FIGURE 3.14 Reflection Coefficients of Primary and Secondary Coils (f:100kHz->10GHz).

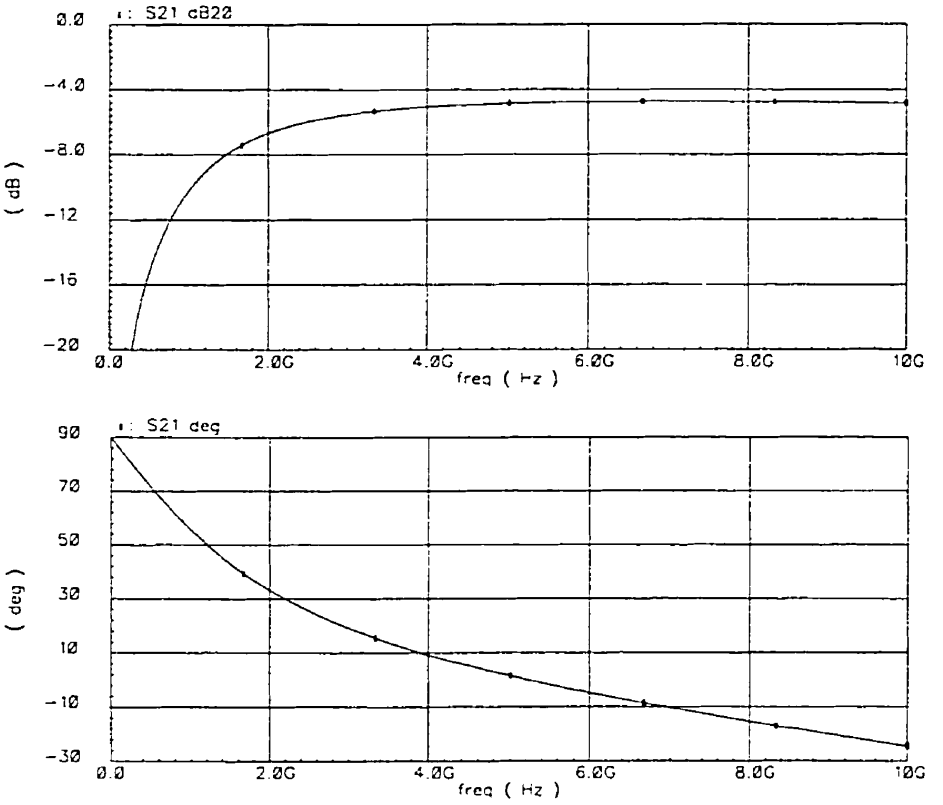

FIGURE 3.15 Measure of Transformer Transmission Efficiency(f:100kHz->10GHz)

3.6 Buffer Design and Circuit Biasing

The buffer used was a simple open-drain differential pair, as shown in Figure 3.16. The DC voltage at the buffer gates was set using a resistor divider (see Figure 3.19). The transistor drains are externally connected to 50Ω terminations using bias-Ts. The differential pairs are biased at 5mA, using a wide-swing cascode NMOS current mirror [Johns, '97]. The negative G_m cells are biased using the same mirror architecture, but in PMOS. Both designs are shown in Figure 3.17. Note that the negative G_m cells are both biased at 10mA.

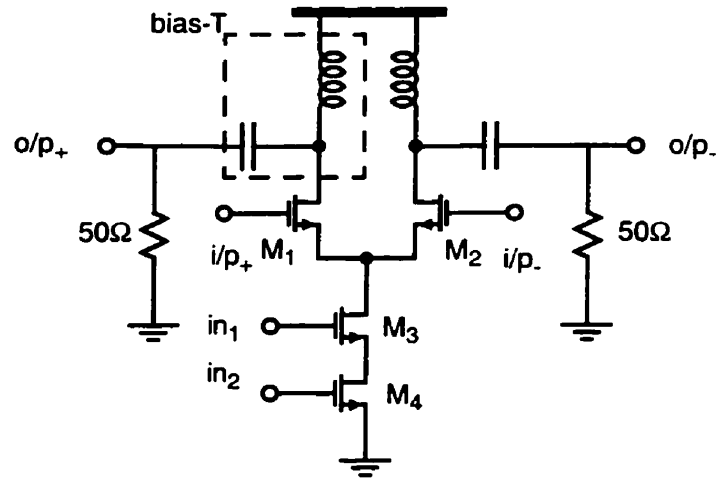

FIGURE 3.16 Open Drain Buffer

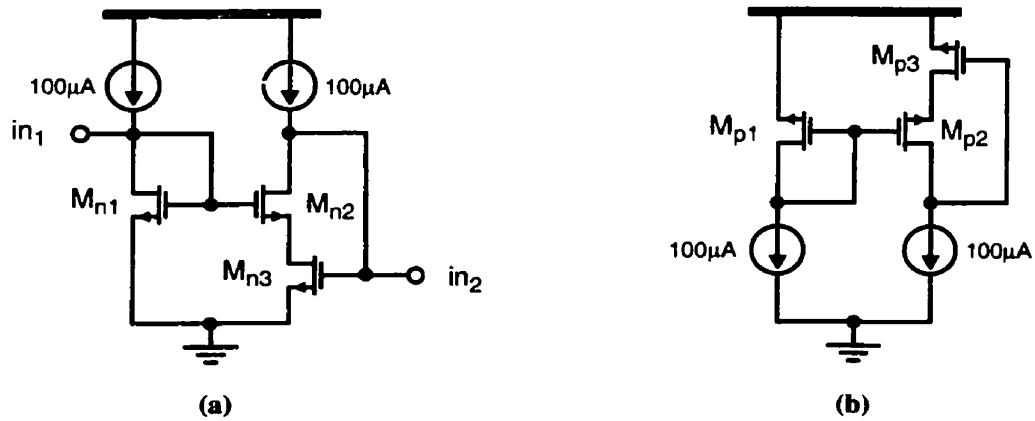

FIGURE 3.17 a) NMOS & b) PMOS Wide-Swing Cascode Current Mirrors

The design values for all the transistors in the figures above are listed in Table 3.2.

TABLE 3.2. Transistor Sizes (μm/μm)

M_1,M_2	100/0.18
M_3,M_4	400/0.5
M_{n1}	3/1
M_{n2},M_{n3}	8/0.5
M_{p1}	6/0.48
M_{p2},M_{p3}	12/0.24

3.7 Simulation Plots

The simulation results shown here were generated by simulating the final, extracted lay-out. The plots in Figure 3.18 are the differential outputs, at the 50Ω termination, of each oscillator core. These outputs are displaced from each other by 90 degrees, i.e. quadrature outputs have been generated. The magnitude of the lower frequency oscillation is smaller, as the tank impedance is inversely proportional to increasing tank capacitance. At the maximum oscillation frequency of 2.851GHz, the outputs are not perfectly sinusoidal. This occurs due to the large differential signal present between the buffers inputs, which forces M_1 and M_2 into triode operation for part of the oscillation cycle.

Figure 3.19 demonstrates that the transformer is operating as expected over its 'passband'. The voltage conversion is 1:2.3 from the primary to the secondary. The result is not equal to 2 as the inductors laid out to implement the secondary of the transformer are not all equal in length. This property is inherent to the Frlan transformer (Figure 3.9 d).

The power supply rejection of the oscillator was investigated. The low frequency or DC rejection is detailed in Chapter 4. The high-frequency rejection performance was established by simulation. A sine wave is placed on V_{dd} of amplitude 180mV, i.e. 10% of nominal V_{dd}, the frequency was varied and for this system the worst case jitter occurs for a modulation frequency of 1.5GHz. The oscillation frequency was set to the centre frequency and the sampling rate is 5ps. Figure 3.20 displays the normalized jitter of the system with respect to time (n*5ps), the modulation on V_{dd} is not activated until half way through the simulation, from this point on we can see that the jitter deteriorates.

Finally the tuning range of the design is presented. The frequency of oscillation can be adjusted from a minimum of 2.158GHz to a maximum of 2.882GHz. This amounts to a tuning range of +/- 13.5% when the centre frequency is assumed to be 2.52GHz.

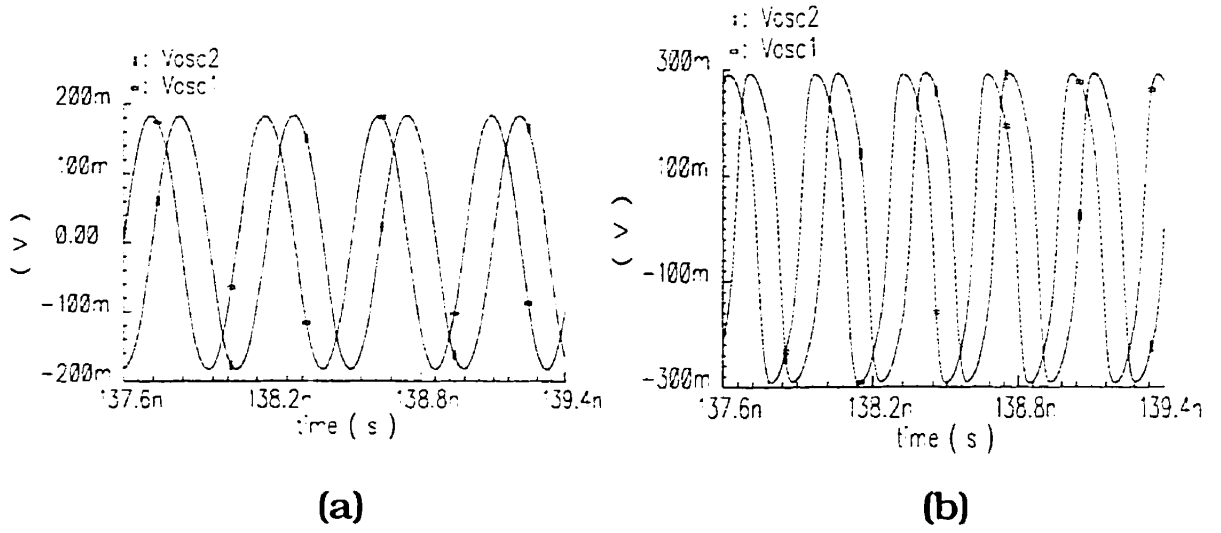

FIGURE 3.18 a) Oscillation at 2.158GHz (minimum), b) Oscillation at 2.882GHz (maximum).

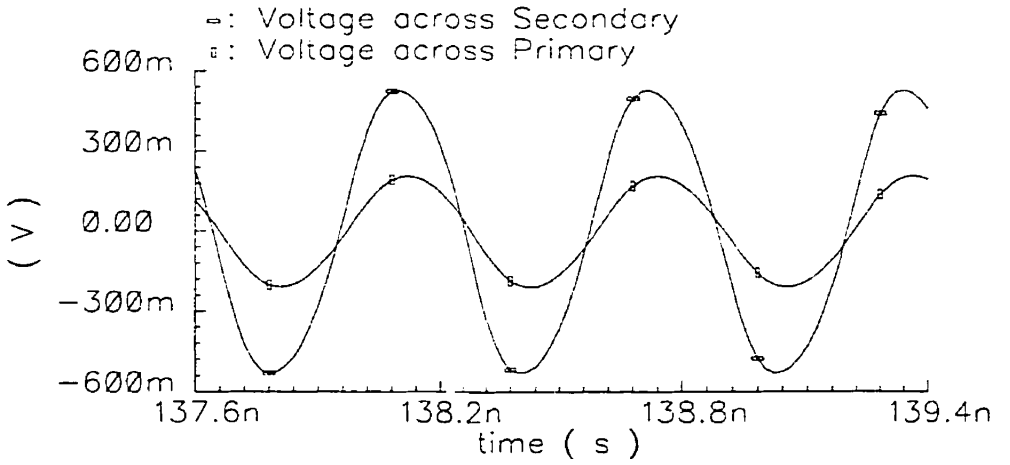

FIGURE 3.19 Transformer Simulation (voltage ratios at both extremities are equal to 2.3V/V).

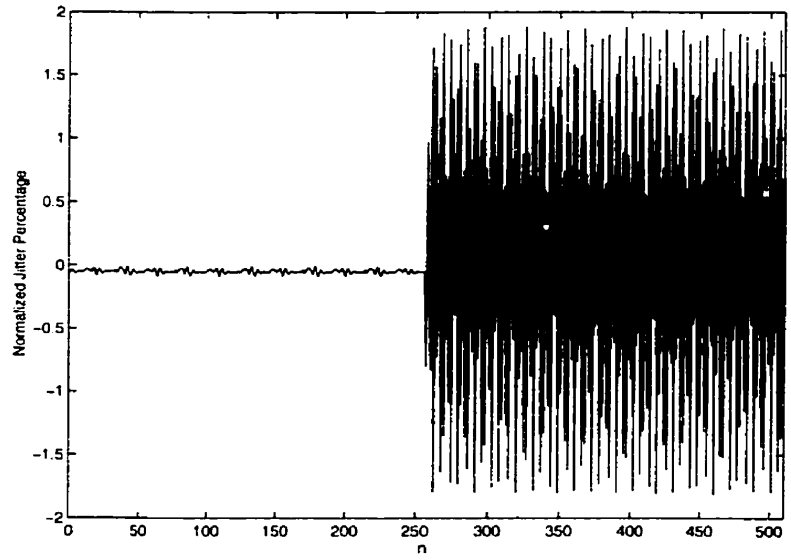

FIGURE 3.20 Oscillator Jitter Plot.

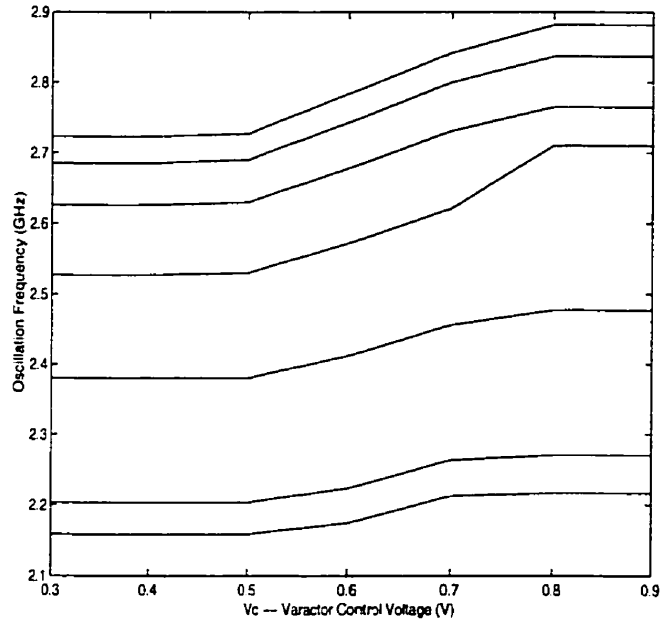

FIGURE 3.21 Tuning Characteristic.

3.8 Circuit Layout

In the circuit layout shown below, metal fill has been deleted to make the diagram easier to inspect. The chip measures 1500μm x 1500μm. One notable aspect of the layout is that wide metal strips (10μm) needed to be used to connect the switches and fixed capacitors to

the transformer secondary. This is because the current levels are approximately doubled from the primary to the secondary. These lines have parasitic capacitance and inductance. The inductance of these lines was minimized by using two metal6 strips in parallel as shown below. The capacitors were constructed using metal6 and metal5 plates, further details are given in the next chapter. The pad structure used was designed by Dickson Cheung. The signal pads are 50μm x 50μm, where as DC or gnd pads are 100 x 100. The distance between pad centres is 150μm. This pad structure is used in conjunction with custom made RF probes.

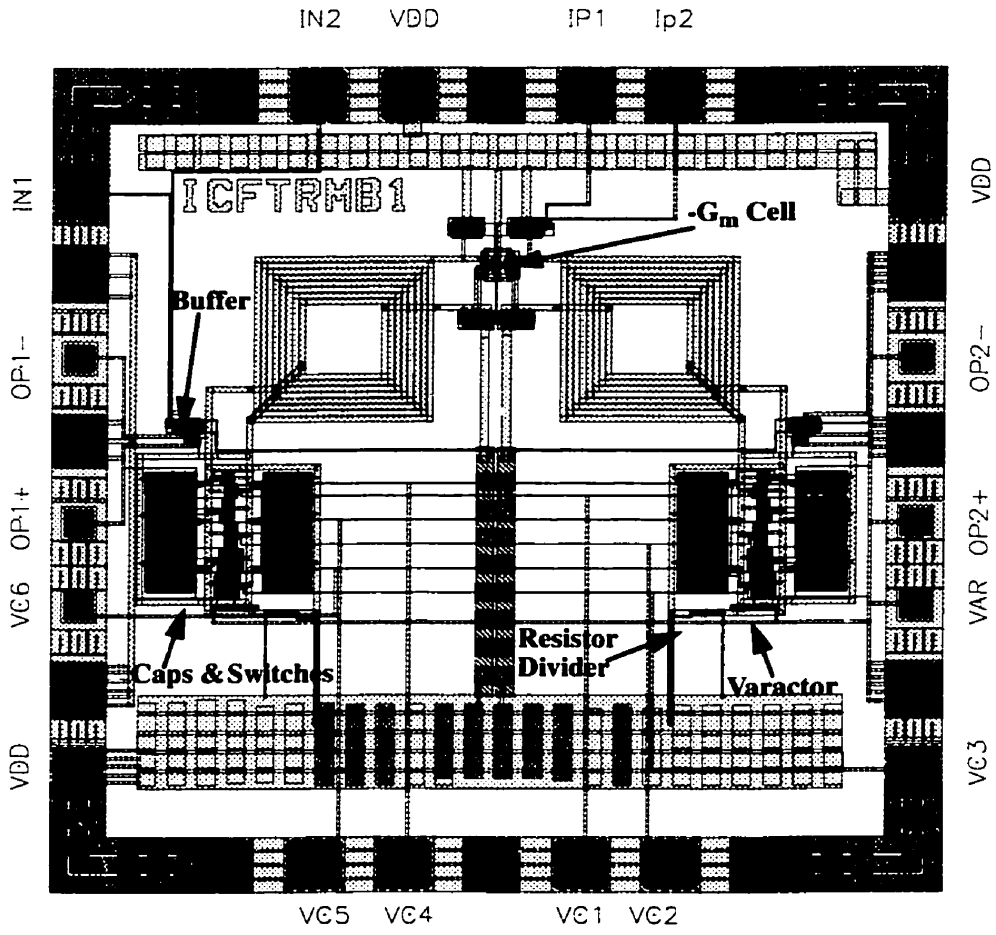

FIGURE 3.22 Chip Layout.

3.9 Conclusion

In this chapter some of the problems associated with designing a wide tuning range LC oscillator have been addressed. The final design has a staggered tuning range characteris-

tic, with hybrid analog/digital voltage control. Two cross-coupled negative G_m cells are used to produce quadrature outputs, which are needed in many transceiver systems to facilitate image rejection. The two oscillator cores draw 20mA from a 1.8V supply. An additional 10mA is used for biasing the open drain buffers. The simulated tuning range is from 2.158GHz->2.882GHz, which is a tuning range of 27% around a center frequency of 2.52 GHz. The tuning range was increased for the second design submission to 33%, this design is presented in Chapter 5.

3.10 References

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Chapter 4

Measurements for Fabricated VCO

The following chapter presents some illustrative test results for the fabricated oscillator. The oscillator was tested using a *Cascade* probe bench, in conjunction with *GGB* custom-made RF-probes (up to 40GHz). The output of the circuit was inspected using a *HP8563* spectrum analyzer (up to 26.5GHz).

4.1 Tuning Range

The main design consideration for this work was the tuning range. As we will see from the frequency spectrum plots presented in this chapter the tuning range does not match the simulated tuning range. The average tuning range (averaged over test-die) was found to be 14%, from 2.54GHz to 2.93 GHz. This tuning range is approximately half of what was observed in simulation (27%). Although the top frequency is similar to that observed in simulation (2.85GHz -- see Figure 3.18), the lowest frequency is approximately 500MHz above the simulated result. This occurred as the tank capacitor values were incorrect. This is discussed in greater detail in Chapter 5. A second design will be tested in November of this year.

4.2 Phase Noise

Two spectra are are presented in Figures 4.1 and 4.2. As one would expect, the phase noise performance at the higher frequency is superior. There are higher losses present in the circuit at the lowest frequency, because all the capacitors are switched into the oscillator tank. The phase noise for both cases is measured at a 2MHz offset: for a carrier frequency of 2.892GHz the phase noise performance was found to be -101dBc/Hz, at the lowest frequency of 2.559GHz the phase noise was -85dBc/Hz.

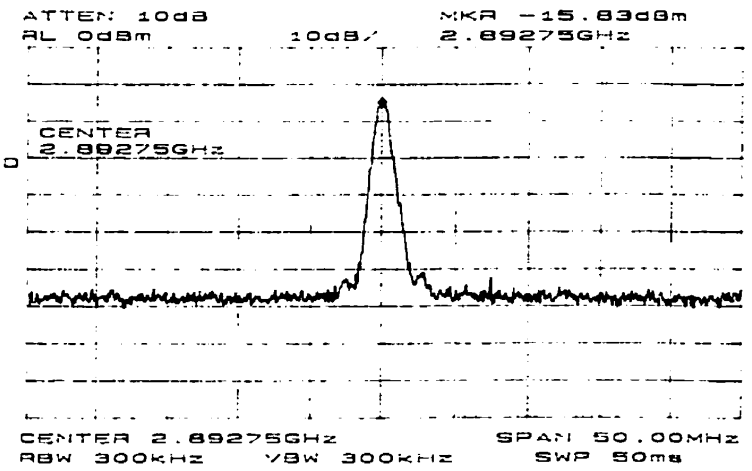

FIGURE 4.1 Frequency Spectrum (Maximum Oscillation Frequency)

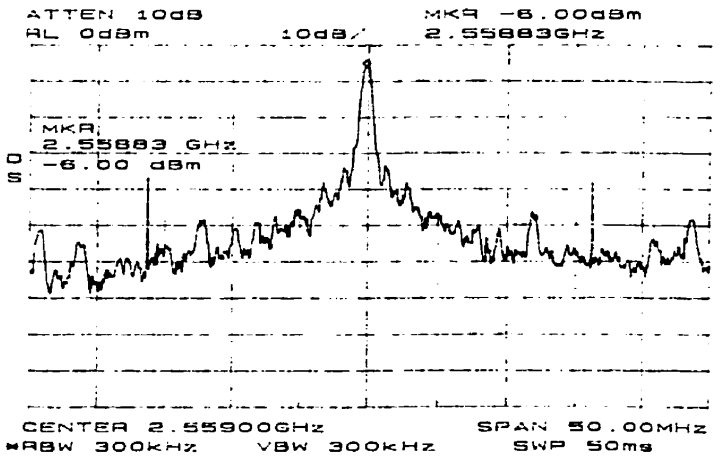

FIGURE 4.2 Frequency Spectrum (Minimum Oscillation Frequency)

It should be noted that the noise measurement was made by taking a single-ended output of one of the oscillators. This infers an inferior phase-noise measurement, as the amplitude of the test-signal will be half that of the differential signal, and common-mode noise will not be eliminated. A balun or hybrid should be used to combine both signals, so as to eliminate this source of noise and improve the phase-noise measurement.

The performance of simple spectrum-analyzer measurements is limited. A typical spectrum-analyzer is not adequate to measure noise at large offset frequencies. The quality of the phase noise-measurement taken by the spectrum analyzer is limited by the analyzer's synthesizers (used to convert the input frequency to the measurement frequency) and the relatively poor noise-figure of the analyzer's front end.

The noise testing can be made more accurate by using the delay line method [Andreani, '98], usually incorporated into a dedicated phase-noise system [RDL,'01]. A block diagram of a typical system is shown in Figure 4.3. There are a number of other measurement techniques such as the Quadrature Technique or the FM Discriminator Method [Owen]. The delay line method is introduced as it is in common use for the testing of RF oscillators [De Muer, '00, Tiebout, '01]. The advantages of this test-method are that it can be used to measure the phase noise of unlocked or drifting RF oscillators, and it does not require an additional RF source. The oscillator signal is split into two separate paths, one path is fed directly to a mixer, the other passes through a delay line. This delay line is necessary to ensure that the noise at each of the mixer's inputs is uncorrelated. The delay line includes a variable phase-shifter so that the phase of the two input signals to the phase-detector can be set for phase quadrature. This implies that if the phase detector has inputs $\sin(\omega t+\phi_{n1})$ and $\cos(\omega t+\phi_{n2})$ then its output will have two components, i.e. $\sin(2\omega t+\phi_{n1}+\phi_{n2})$ and $\sin(\phi_{n1}-\phi_{n2})$. The latter is a signal whose amplitude is proportional to the phase noise of the oscillator. This signal can be viewed using a spectrum analyzer, or, as with most dedicated systems, it will be digitized and the resulting signal will be manipulated by a FFT digital signal processor.

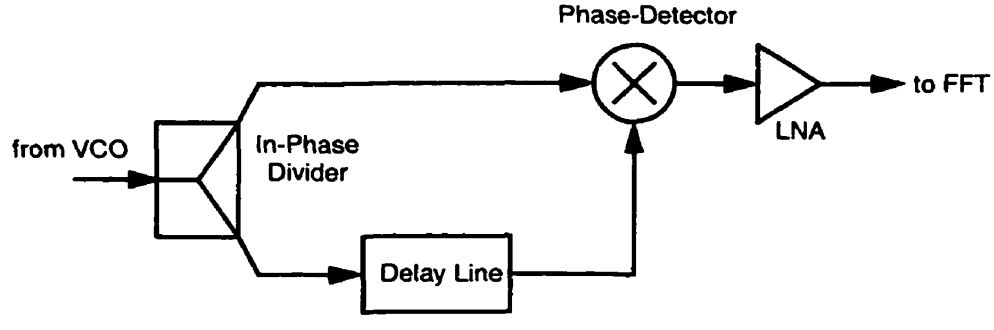

FIGURE 4.3 Delay Line Discriminator

4.3 Test Conclusions

The power supply rejection of the design seems to be excellent. With a fixed current being drawn by the oscillator, V_{DD} was varied between 1.5 and 1.85V. The frequency of oscillation varied from 2.82GHz (1.5V) to 2.89GHz (1.85V).

More time and consideration will be given to the testing of the second design. As well as improving the phase noise 'testbench', the oscillator will be tested for quadrature-phase mismatch. Below is a table, which illustrates the merits of this work in comparison to previously published oscillator designs, LC oscillators are displayed above the design with ring oscillators at the bottom.

TABLE 4.1 Recently Published RF Oscillators with Specifications.

Reference.	Technology	Power [mW]	Freq. [GHz]	Tuning [%]	Phase Noise [dBc/Hz]	FOM [dBc/Hz]
[Tiebout, '01]	0.25μm CMOS	20 (Quad)	1.8	16	-143 @ 3MHz	-185
[Andreani, '00]	0.6 μm CMOS	4.46	1.8	11	-132 @ 3MHz	-181
[Svelto, '00]**	0.35 μm CMOS	12	1.3	27	-119 @ 600kHz	-175
[Wang, '99]	0.35 μm CMOS	11.6	9.8	3	-115 @ 1MHz	-184
[Wong, '00]	0.35 μm CMOS	22.5	1.9	17	-105 @ 1MHz	-157
[Kral, '98]	0.6 μm CMOS	25	1.35	12	-104 @ 100kHz	-172
[Rofougaran, '96]	1 μm CMOS	30	0.9	17	-85 @ 100kHz	-149
[Kim, '00]	0.6 μm CMOS	20	0.9	10	-132 @ 300kHz	-154
[Lam, '99]	0.35 μm CMOS	26 (Quad)	2.6	13	-110 @ 5MHz	-150
[Razavi, '97]	0.6 μm CMOS	15 (Quad)	1.8	7	-100 @ 500kHz	-159
[Lee, '00]	0.25μm CMOS	6	1.8	not-stated	-121 @ 600kHz	-183
[Liu, '99]	0.35 μm CMOS	18 (Quad)	6.5	16	-98.4 @ 1MHz	-162
[Bury, 01] (simulated)	**0.18μm CMOS**	**36 (Quad)**	**2.5**	**27**	---------- ----------	---------- ----------
Second Design (simulated)	**0.18μm CMOS**	**36 (Quad)**	**2.35**	**33**	---------- ----------	---------- ----------
Tested Oscillator	**0.18μm CMOS**	**36 (Quad)**	**2.74**	**14**	**-101 @ 2 MHz** **-85 @ 2 MHz**	**-149** **-131**
[Razavi, 01]	0.4μm CMOS	33.5	2.5	29	-80 @ 5MHz	-119
[Hajimiri, '99]	0.25μm CMOS	10	2.8	34	-95 @ 1MHz	-154

A normalized phase noise is defined as a figure of merit (FOM) for oscillators:

$$FOM = S_{SSB}\left(\frac{\Delta f}{f_o}\right)^2 \frac{P_{VCO}}{mW} \tag{34}$$

where P_{VCO} is the total VCO power consumption and S_{SSB} is the single sideband noise power [Tiebout, '01]. 'Quad' implies that two VCO cores are required. Two phase noise measurements are shown here, one at each of the tuning range extremities (Figure 4.1 and 4.2). One important variable that is not used in the FOM is the modulation index of the oscillator which has been minimized in this design while maintaining a wide tuning range.

Note **: This work has the largest tuning range of all the LC oscillators listed in Table 1, with the exception of the design reported by Svelto ['00]. It should be mentioned that the authors of this paper used a control voltage between 0 and 5V, which is larger than the V_{dd} used to power the oscillator (2V). Staggered-tuning is not utilized in their work, its absence will mean that any noise coupled to the varactor control electrode translates into a large phase noise at the oscillator output. The phase noise performance of this work is impressive, yet bond-wire inductors were used in the tank, which, as discussed previously, are not easily reproducable in a manufacturing environment.

4.4 References

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Chapter 5

Conclusion

As was discussed in the previous chapter, the tested oscillator exhibited a narrower tuning range than expected, so another design was submitted for the June 2001 submission date. The following pages describe modifications made to the design, reasons as to why this new topology may be preferred to the classical LC oscillator for on-chip implementations, and finally a review of the work presented in this thesis as well as future work that will be carried out.

5.1 Circuit Redesign.

The oscillator did not work as simulated. It was necessary to identify the design error and then submit a modified version of the original design for fabrication. It became obvious that the capacitors that were laid out were approximately one third their extracted values. This occurred as the technique used by *Cadence* to extract the capacitors in question was highly inaccurate. The capacitors used for the second design iteration were kept simple to ensure proper extraction. Four metal layers were used in their construction. A representation of the structure is shown in Figure 5.1. Metals 1 and 2 were omitted to minimize any parasitic capacitance to ground.

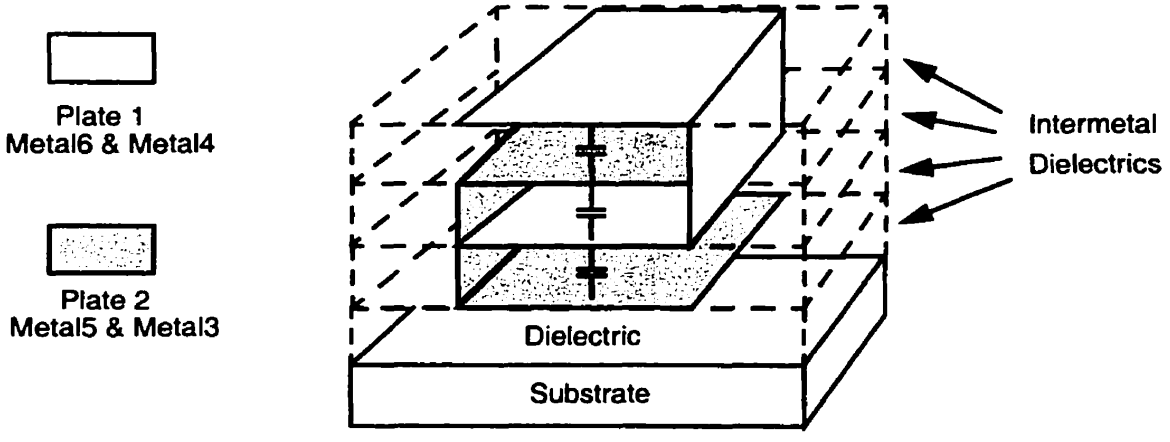

FIGURE 5.1 Representation of four-metal capacitor

The resulting structure has three desired metal-metal capacitances, given by $C = \frac{\varepsilon A}{d}$, as well as four plate to ground parasitic capacitances.

A number of other modifications were made to the design. The varactor was moved from the primary, where it was in parallel with the switched capacitors, to the secondary. As was discussed in **3.5.2,** it is necessary to minimize varactor channel resistance so as to improve the phase noise performance of the oscillator. The initial design used a 12μmx12μm transistor, which has a relatively high channel resistance. The varactor in the second design is 100μmx0.5μm.

The tuning scheme is also somewhat simplified from the first case, such that there are only five tuning characteristics associated with this design. 250fF, 500fF, 500fF and 600fF were the design values chosen. The simulated staggered characteristic is shown below. The overall tuning range is from 1.999GHz to 2.766GHz, which is equivalent to a tuning range of 33% (i.e. +/- 16.5%) about a centre frequency of 2.35GHz. This is an improvement of 6% over the previous design discussed in Chapter 3.

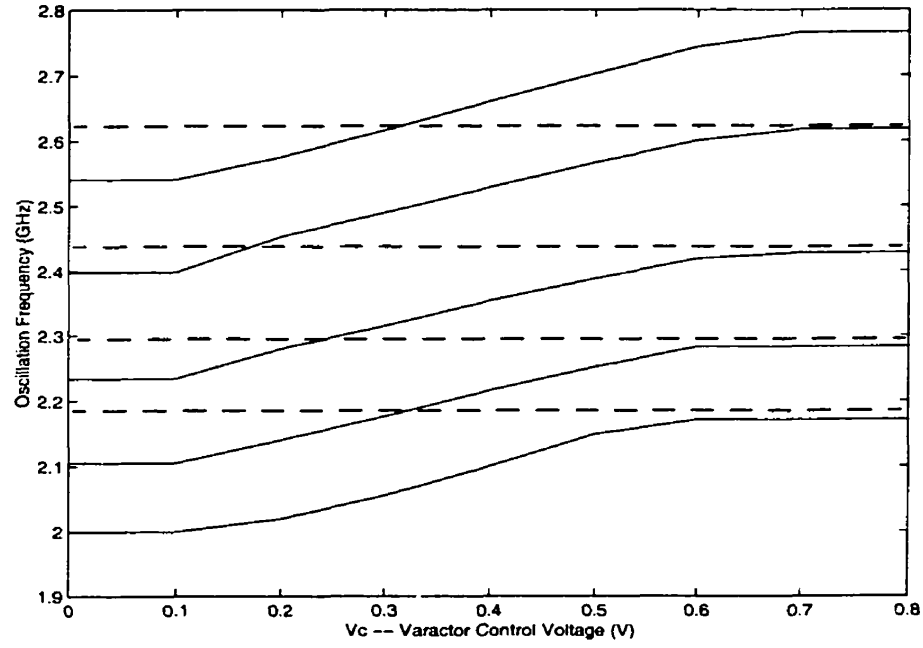

FIGURE 5.2 Tuning Characteristic of Second Design

The rest of the circuit was left unaltered, such that the power consumption of both designs is equivalent.

5.2 Benefits of a TC Oscillator

In order to understand some of the advantages and disadvantages of a transformer-coupled implementation, the final design is compared to a LC oscillator that uses a tank inductance of 5.0nH. This inductance is approximately equivalent to the inductance of the secondary coil in the transformer-based design (i.e. 5.1nH).

To allow for a reasonable comparison, it was required that the on-resistance of the switches used in the inductor case be four times greater than those used in the transformer case. This is because an impedance is reflected from being in parallel with the low-impedance coil to the high-impedance side, and therefore appears to be four times greater. As the varactor appeared across the primary in the transformer case, its size was not changed. The tuning characteristic for the inductor case is shown below (simulations run for Vc=0 and Vc=0.8V).

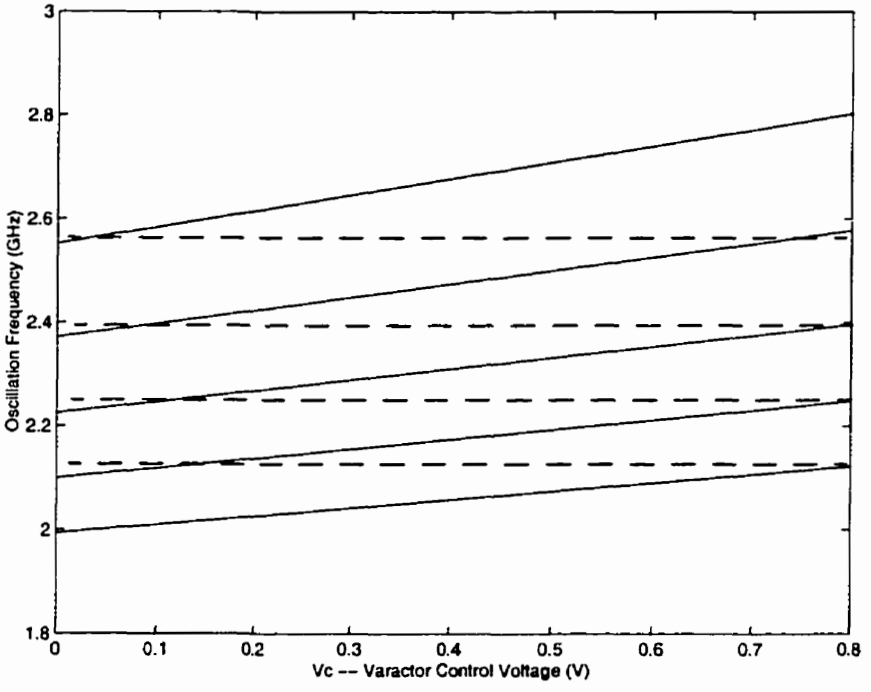

FIGURE 5.3 Tuning Characteristic of Inductor Based Design

The first obvious benefit of the single coil design is that less chip area will be used. Other advantages are that it may be easier to accurately model the inductors, as opposed to the transformer, and simulation times are less for the inductor case.

There are a number of advantages to using a transformer over an inductor:

For increased system integration and portability it is becoming necessary for many telecommunications systems to operate from a single battery. This means that today's analog designers are having to design circuits that operate at low supply voltages. The amplitude of the oscillation across the negative-admittance cell can be controlled by the designer [Anand, '01; Margarit, '99], but many methods of achieving this level control will add to circuit complexity, and therefore add to contributed device noise. This is undesirable, as it is vital to minimize oscillator phase noise. In the case where a inductor was used in the tank, the tuning range is approximately the same as for the transformer case. These simulations were, however, run without a buffer. When the same open-drain buffer was included in the design, the top frequency fell from 2.802GHz to 2.678GHz (124MHz), with the lower frequency falling from 1.994GHz to 1.945GHz (49MHz). In comparison when the same test was done on the 'TC' oscillator, the differences were 36MHz and 6MHz, respectively. So for a transformer based design the loading effect of the buffer on the oscillator is not as dramatic.

The buffer transistors are voltage controlled. In order to ensure, a 'clean' sinusoidal signal at the buffer output, it is necessary for these transistors to remain active throughout the oscillator cycle. This is not ensured for the inductor-based oscillator. At the high frequency extremity, the V_{gs} across the buffer transistors varies from -0.11V to 0.9V; for the other extremity, the range is -0.12V to 0.85V, so that the buffer's output deviates substantially from the required sinusoid. This distorted output is shown below.

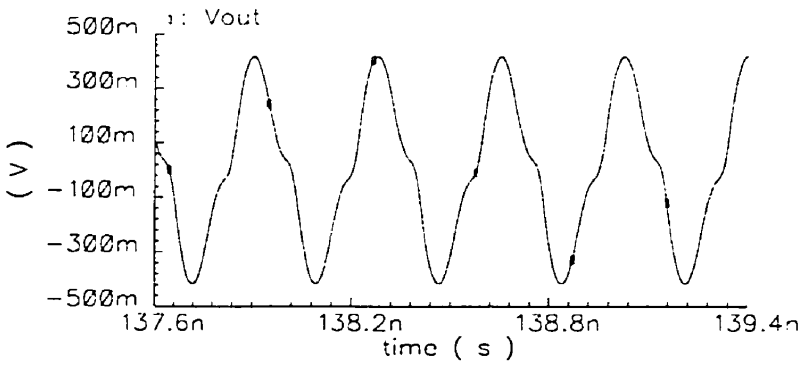

FIGURE 5.4 Buffer Output for Inductor-Based Oscillator

The designer has more biasing control of the buffer in the 'TC' case. Firstly the DC voltage at the buffer gates can be set at any level between 0 and 1.8V. For this reason, and the fact that the voltage has been stepped down by a factor of approximately 2 by the transformer, the drive signals for the buffer are reasonable.

One final point worth noting is of a practical nature. As was discussed, the capacitor values for the second submitted design were 250fF, 500fF, 500fF, and 600fF. To achieve a similar tuning range for the inductor-based design, the four values were all set to 60fF. It is the designer's opinion that the transformer based design would be easier to implement. For the CMOS process in question there will be a discrepancy in capacitor values due to process variations. This is true for both cases, but it is important for many circuit designs to maximize the ratio of desired to parasitic capacitance values. In the inductor-only case, the staggered-tuning characteristic is more difficult to implement due to the small sizes of the capacitors required. The benefits of this novel oscillator topology over a LC oscillator with the same inductance as that of the large coil of the transformer, are summarized as follows:

Benefits of a Transformer Based Oscillator

1) The element sizes used in the transformer oscillator are more practical and lead to a more implementable circuit.

2) The capacitive loading introduced by a buffer is not as dramatic as the LC case.

3) The inclusion of a transformer in the design allows the buffer's gates, or any other additional circuitry, to be biased at the designer's discretion. The amplitude of the oscillation may also be reduced so that the transistors of any following circuitry operate in the correct mode.

5.3 Future Work

The second design will return from fabrication in October of 2001. The testing of this second circuit will be more comprehensive than the first. A test will be performed to measure the phase error between the two quadrature outputs. More phase noise tests will be carried out as well as more power supply rejection ratio (PSRR) tests, and the effect of varying chip biasing conditions will be investigated.

The designer's goal for this work was to validate a novel design idea. There are many ways in which this design could be optimized in the future. For any oscillator design there are many considerations: phase noise, power, and amplitude control. The main goal of this work has been to maximize the tuning range of the oscillator, with other considerations being secondary.

In terms of future work, more time needs to be spent in developing a passive circuit model for the transformer, whether it be compact or distributed. For respectable phase-noise simulation results, it would also be necessary to compare and contrast alternative MOS models (to those used by *CMC*) such as *Philip's MOS9*. The science of transistor modeling at RF frequencies is on-going [Chen '01], but there are a number of methods of improving phase-noise simulations that are available to the designer.

There are many new methods that are being explored to implement novel tuning schemes, in some cases new varactor structures are used [Wong, '00, Porret, '00], in others the circuit biasing is modulated [Liu, '99; Anand, '01]. It would be interesting to investigate alternative implementations of hybrid-tuning utilizing some of the novel ideas published recently. It also would be interesting to incorporate this design into a Phase-Locked Loop to further investigate its operation [McLaren, '00]

5.4 Conclusion

For a RF oscillator operating within a transceiver, it is necessary that the tuning range is large enough to ensure that the correct oscillation frequency can be set. This frequency is subject to change, due to temperature and process variations. Ring oscillators are able to guarantee a wide-tuning range, but they suffer from a poor phase-noise performance. LC oscillators have better phase-noise performance due to the filtering action of the LC tank used, but historically it has been difficult to design for a wide-tuning range. This problem is exacerbated by reduced voltage supplies. This has been addressed in this thesis, with a compromise between phase-noise performance and tuning range. The final design has a (simulated) tuning range of 33% (around a centre frequency of 2.35GHz), quadrature outputs and draws 20mA from a 1.8V supply.

5.5 References

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