High Speed Submicron CMOS Oscillators and PLL Clock Generators

by

Lizhong Sun, M. Eng.

A thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of
Doctor of Philosophy

Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Carleton University
Ottawa, Ontario
Canada

April 1999

© Copyright 1999, Lizhong Sun

National Library of Canada
Acquisitions and Bibliographic Services
395 Wellington Street
Ottawa ON K1A 0N4
Canada

Bibliothèque nationale du Canada
Acquisitions et services bibliographiques
395, rue Wellington
Ottawa ON K1A 0N4
Canada

Your file Votre référence

Our file Notre référence

The author has granted a non-exclusive licence allowing the National Library of Canada to reproduce, loan, distribute or sell copies of this thesis in microform, paper or electronic formats.

L'auteur a accordé une licence non exclusive permettant à la Bibliothèque nationale du Canada de reproduire, prêter, distribuer ou vendre des copies de cette thèse sous la forme de microfiche/film, de reproduction sur papier ou sur format électronique.

The author retains ownership of the copyright in this thesis. Neither the thesis nor substantial extracts from it may be printed or otherwise reproduced without the author's permission.

L'auteur conserve la propriété du droit d'auteur qui protège cette thèse. Ni la thèse ni des extraits substantiels de celle-ci ne doivent être imprimés ou autrement reproduits sans son autorisation.

0-612-48337-1

Canada

Abstract

This thesis presents the design, analysis and implementation of monolithic GHz range voltage/current controlled ring oscillators and a monolithic phase-locked loop (PLL) clock generator in submicron CMOS technology. A general ring oscillator topology capable of achieving high speed operation, multiphase output and wide tuning range is proposed. The topology uses sub-feedback inverters to construct fast loops enabling a long chain ring oscillator to achieve increased operating frequency and higher equivalent quality factor. The operating frequency of the ring oscillator is directly proportional to the transconductance (G_m) of sub-feedback inverters which can be controlled with an external voltage to achieve linear tuning. Detailed implementation of the topology for both single-ended and differential circuits is also proposed. Extensive theoretical analysis yielded insight into the sub-feedback loop ring oscillators and allowed formulation of design guidelines. Simulations and measurement results (0.5 μm CMOS process) support the analytical findings. A fully integrated 1.25 GHz 0.35 μm CMOS PLL clock generator that included the proposed VCO topology and a frequency control and stabilizing bias circuit was designed, implemented and tested. Measurement results confirm the suitability of the VCO and the PLL for applications such as clock generation/recovery systems, high speed multiphase data sampling and microprocessor clock synchronization.

Acknowledgments

This thesis would not have been possible without the encouragement, support and contributions of many people. In particular, I am very much in debt to my supervisor Professor Tad Kwasniewski, for motivation when I needed it most, and many hours of interesting discussions. Without his guidance and helpful suggestions, working on this thesis would have been much more difficult.

I would like to thank Kris Iniewski and Brian Gerson from PMC-Sierra, Inc, Burnaby, BC., for the offer of a co-op term for me to work there and giving me enough freedom to try out new ideas in new project. Special thanks to Victor Lee for his contribution to 1.25 GHz CSU project. I would also like to thank Dragos Cartina, Yin Xu, Marcial Chua, Rod Zavari, Justin Taylor, Joseph Yuen and Bernard Guay in analog department, their help and discussion have made my stay at PMC-Sierra a rich and rewarding experience.

During at Carleton, I was able to benefit from the knowledge of many Professors, staff, former graduate students, research engineers. I would like to thank all of them, especially Prof. Calvin Plett, Prof. Ralph Mason, Nagui Mikhail, Jacques Lemieux, Fangxing Wei, Kashif Sheikh, Sergie Uhanoy, Bill Toole, Roni Khazaka for their help and discussion.

The financial support from Motorola Semiconductor, PMC-Sierra, Inc and infrastructure support from Communications and Information Technology Ontario (CITO), Canadian Microelectronics Corporation (CMC) and National Science and Research Council of Canada (NSERC) are gratefully acknowledged.

Last but not least, I would like to provide my gratitude to my parents, my parents-in-law and my wife for their love, understanding, patient and support.

The information used in this thesis comes in part from the research program of Dr. T.A. Kwasniewski and his associates in the VLSI in Communications Group. The research results appearing in this thesis represents an integral part of the ongoing research program. All research results in this thesis including tables, graphs and figures but excluding the narrative portions of the thesis are effectively incorporated into the research program and can be used by Dr. Kwasniewski and his associates for education and research purposes, including publication in the open literature with the appropriate credits. Matters of intellectual property may be pursued collaboratively with Carleton University and Dr. Kwasniewski where and as appropriate.

To
my parents
and my wife

Contents

List of Figures

List of Tables

Abbreviations

ADC	Analog-to-Digital Converter or Conversion
ASIC	Application Specific Integration Circuit
BER	Bit-Error Rate
BiCMOS	Bipolar-CMOS
BW	Bandwidth
BPF	Band-Pass Filter
CDMA	Code-Division Multiple Access
CML	Current Mirror Logic
CMOS	Complementary Metal-Oxide Semiconductor
C^2MOS	Clocked CMOS
CMRR	Common Mode Rejection Ratio
CRC	Clock Recovery Circuit
DAC	Digital-to-Analog Convertor
DC	Direct Current
DDS	Direct Digital Synthesis
DECT	Digital European Cordless Telephone System
DLL	Delay Locked Loop
DPA	Digital Phase Accumulator
DSP	Digital Signal Processing
DUT	Device Under Test

ECL	Emitter Coupled Logic
FET	Field Effect Transistor
FF	Flip-Flop
FFT	Fast Fourier Transformer
FPGA	Field Programmable Gate Array
f_T	Transistor Unity-Gain Frequency
GaAs	Gallium-Arsenide
g_m / G_m	Transconductance
GMSK	Gaussian Minimum Shift Keying
GSM	Global System Mobile
HSPICE	High Speed Simulation Programming with IC Emphasis
IC	Integrated Circuit
ICO	Current Controlled Oscillator
IEEE	Institute of Electrical and Electronics Engineers
ISSCC	International Solid State Circuits Conference
JSSCC	Journal of Solid State Circuits
LF	Loop Filter
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
MASH	Multi-Stage Noise Shaping
MESFET	Metal Semiconductor Field Effect Transistor
MOS	Metal Oxide Semiconductor
NRZ	Non-Return-to-Zero
PA	Power Amplifier
PD	Phase Detector
PLL	Phase-Locked Loop
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuits

ROM	Read Only Memory
RZ	Return-to-Zero
SAW	Surface Acoustic Wave Devices
SONET	Synchronous Optical Network
SNR	Signal-to-Noise Ratio
TDMA	Time-Division Multiple Access
TSPC	True Single Phase Clock
VCO	Voltage-Controlled Oscillator
V_{DD}	Positive Power Supply
VHDL	Very High-Speed Integrated Circuits Hardware Definition Language
VLSI	Very Large Scale Integrated Circuits
V_{SS}	Ground Power Supply
XOR	eXclusive OR gate

CHAPTER 1

Introduction

1.1 Motivation

The rapid growth in the use of wireless communication devices and demand for higher local area networks (LANs) data rate provides both opportunities and challenges for VLSI and RFIC technology development. The demanding performances these systems require has resulted in tremendous academic and industrial effort to design larger scale integrated circuits (IC's) and proposals for new high speed and low power circuit structures in a cost effective technology.

Current IC's for the GHz frequency range are mostly implemented in either a GaAs MESFET or Si bipolar process. However, submicron CMOS technology is considered the most attractive technology in the long run due to the capability CMOS offers for large-scale integration and low cost [GrMe95][Abi97]. The modern deep submicron CMOS process provides for high f_T transistors [Wan98], allowing CMOS RF IC's to compete with GaAs IC's and Si bipolar IC's in the important low GHz frequency ranges.

Phase-locked loops (PLL) are widely used in various communications and control system applications. In mobile cellular systems, for example, PLLs are incorporated into frequency synthesizers to generate high frequency, tunable carrier signals. In data communications, PLLs are used in timing recovery circuits to extract the clock from the received signal to restore the distorted data and synchronize the post-stage digital signal processing (DSP). The commercial success of LANs and the demand for higher data rates have recently increased the need for inexpensive high speed PLLs. Other applications of PLL include tracking filter, modulation and demodulation of signals. As systems applications approach higher frequency/speed and incorporate higher level integration, PLL design continues to be a challenge. PLL must deal with requirements such as monolithic implementation, low cost, minimal number of external components, low power dissipation and low phase noise.

The voltage controlled oscillator (VCO) is an integral part of phase-locked loops (PLL), frequency synthesizers and clock recovery circuits. Most current commercial wireless transceivers utilize external varactor-tuned resonators to implement low phase noise VCOs in frequency synthesizers, which function as local oscillators. Incorporation of these oscillators on chip is an important goal in increasing receiver integration level and thereby reducing power and cost. In high speed data sampling, clock recovery and synchronization systems, ring oscillators are particularly attractive for multiphase and quadrature clock signal generation. They are easy to implement monolithically and take only a small amount of chip size. Although a free running ring oscillator tends to have poor noise performance, the close-in VCO phase noise can be minimized if PLL loop bandwidth and loop order can be kept high. Since the volume of data traffic in LANs is expanding almost exponentially from one year to the next, high speed operation has become a critical requirement in many modern data communication transceivers, where the maximum VCO oscillating frequency often limits the maximum obtainable data rate, especially when mul-

tiphase or quadrature outputs with large and linear tuning range are required. Hence, VCO structures that can satisfy these requirements and work in a GHz range with the CMOS process pose an important design challenge. Furthermore, guidelines leading to an optimum VCO design need to be developed within the limitations of the available technology.

1.2 Contributions

The major contributions made in this thesis are the following:

(1) A general ring oscillator circuit topology capable of achieving high speed operation and multiple phase output is proposed [SKI99]. The topology uses sub-feedback inverters to construct fast loops enabling a long chain, multiphase output ring oscillator to achieve increased operating frequency and higher equivalent quality factor. It is found that for a long chain ring oscillator, there exists an optimum feedback index i which results in the highest operating frequency.

The operating frequency of the sub-feedback loop based ring oscillator increases linearly with the transconductance (G_m) of sub-feedback inverters which can be controlled with an external voltage (or current). The frequency control can also be understood as changing the effective number of delay stages (N_{eff}) within the range of $(i+1)$ and N, where i and N are the feedback index and the stage number of ring, respectively. Thus the sub-feedback loop based topology also provides an alternative way to conventional capacitive or resistive tuning.

(2) A linearized model in frequency domain is developed and leads to the disclosure of the relationship between speed (increment/decrement) and feedback index i. This speed-feedback index relation is important for optimum speed improvement and is confirmed by

time domain simulations and measurement results. Phase noise in the proposed sub-feedback loop based ring oscillators is analyzed. Noise sources are classified into three groups according to their contribution to the total output phase noise. The analysis discloses the relationship between time-domain output signal waveform shaping and feedback index i. It is found that the sub-feedback loop architecture introduces noise filtering (improved effective quality factor Q) in the signal path. The analysis is confirmed by the simulations and measurement results.

(3) Detailed implementation of the proposed topology for both single-ended and differential circuits is proposed and analyzed. The design was implemented and fabricated in a 0.5 μm CMOS technology. Measurement results confirm the topology's suitability for applications such as high speed multiphase data sampling, clock generation, data recovery systems and microprocessor clock synchronization. A GHz range monolithic CMOS PLL clock generator unit is designed for data communications [SuKw992]. The VCO incorporates the proposed sub-feedback loop based ring oscillator and a frequency control and stabilizing bias circuit to achieve not only a large and linear tuning range but also improved temperature and supply voltage sensitivity. The PLL was fabricated in a 0.35 μm CMOS process, occupies an active area of 1 mm^2, and consumes approximately 100 mW when operating at 1.25 GHz from a 3.3 V power supply.

1.3 Organization of the Thesis

This thesis is organized in six chapters. Chapter 2 reviews VCO principle, design consideration and architectures for high frequency and RF frequency range operation. In order to develop a viable design for VCO circuits and explore the capabilities offered by CMOS technology, system architecture, such as PLL clock generators, clock recovery systems and frequency synthesizers are also discussed.

In Chapter 3, the high-speed capabilities of CMOS ring oscillator are explored. A general ring oscillator circuit topology capable of achieving high speed operation, multiple phase output and wide tuning range is proposed for both single-ended and differential circuit implementations. Speed improvements are analyzed in both frequency and time domain. The circuit design, implementation issues and measurement results (0.5 μm CMOS process) are also presented.

In Chapter 4, the phase noise in single-ended CMOS ring oscillators and the proposed sub-feedback loop based CMOS ring oscillators are analyzed in the time domain and frequency domain. The analysis leads to intuitive guidelines for designing low noise sub-feedback loop ring oscillators. The comparison between theoretical results derived from analytical formulae and experimental results is also presented.

Chapter 5 presents the design and analysis of a GHz range CMOS phase-locked loop clock generator for data communications. The building blocks for PLL are explored. The VCO includes a core circuit developed in Chapter 3 and a frequency control and stabilizing scheme which is proposed to achieve not only large and linear tuning range but also improved temperature and supply voltage sensitivity. Loop design and phase noise analysis is also presented. The measurement results of the monolithic implementation in a 0.35 μm CMOS process are summarized in Section 5.5.

In Chapter 6, concluding remarks and recommendations for further research in this area are presented.

Although inductor based oscillators are not the focus of this thesis, the design methodology is also explored. The design in a 0.35 μm CMOS process and measurement results are presented in Appendix A.

CHAPTER 2

Monolithic VCOs and Phase-Locked Loops

2.1 Introduction

The development of a high speed monolithic voltage controlled oscillator is a major part of this thesis. Therefore the first and largest section of this chapter deals with oscillator design. First in Section 2.2, VCO principles, design considerations and architectures for the RF frequency range is reviewed. Summaries of current state of the art research literature on the developments of monolithic LC, relaxation and ring oscillators are presented in several tables. In order to develop a viable design of a VCO circuit and explore the capabilities offered by CMOS technology, system architecture must also be considered. Therefore in Section 2.3 and 2.4, PLL clock recovery systems, clock generators and frequency synthesizers are discussed.

2.2 Monolithic Voltage Controlled Oscillators

2.2.1 Oscillator Design Principles

Oscillators come in a variety of different types, but perhaps the two major classifications are those that directly create sinusoidal outputs as opposed to those with square (or triangular) wave outputs (see Fig. 2.1). Sinusoidal-output oscillators employ a positive-feedback loop consisting of an amplifier and a frequency-selective resonator, such as cavity, crystal or LC tank. The amplitude of the generated sine wave is limited, or set, using a nonlinear mechanism, implemented either with a separate circuit or using the nonlinearites of the amplifying device itself [Gre72]. Circuits that generate square, triangular, pulse waveforms are called non-sinusoidal output oscillators. They usually require only one type of energy storage element (e.g., capacitor), and rely on the threshold switching characteristics of the circuit rather than on a frequency selective element to define an oscillatory waveform.

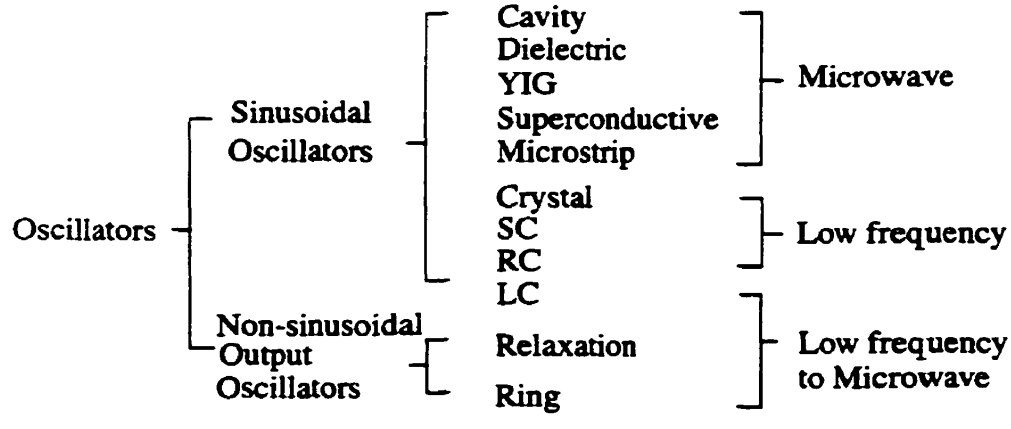


Fig. 2.1. Classification of oscillators

2.2.1.1 Feedback Principle

Electronic oscillators are inherently nonlinear circuits with feedback networks. However linear analysis techniques are very useful for analysis and design. They provide accurate information for predicting the frequency of oscillation but have limited use for predicting the amplitude of oscillation.

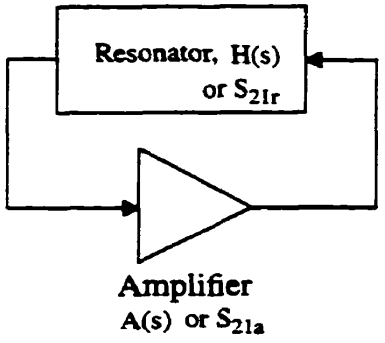


Fig. 2.2. Block diagram of a feedback oscillator

A feedback oscillator consists of an amplifier and a resonant circuit as shown in Fig. 2.2. The elements are designed to fit the following oscillation condition:

$$A(s)H(s) = 1 \tag{2.1}$$

or

$$S_{21_a} \cdot S_{21_r} = 1 \tag{2.2}$$

where A(s) and H(s) are the gain and transfer function for the amplifier and resonator circuits, respectively. S_{21a} and S_{21r} are the forward transmission S-parameter for the microwave or RF amplifier and resonator circuits, respectively. Both the input and output impedances of the amplifier are assumed to be equal to Z_0, and, practically, this is achieved by employing bandpass matching networks to operate near the carrier frequen-

cies [Rob95]. Eq. (2.1) and Eq. (2.2) implies that the product of the two gain magnitudes at the oscillation frequency is unity and the sum of their angles is a multiple of 2π. In other words, the gain of the amplifier must be sufficiently large to compensate for the loss in the resonator and the signal delay round the loop must be an integral multiple of 360 degrees. This is known as the *Barkhausen criterion* [Stra70]. Note that for the circuit to oscillate at one frequency the oscillation criterion should be satisfied at one frequency only (that is, ω_o), otherwise the resulting waveform will not be a single frequency sinusoid.

In oscillators, the frequency stability and close-to-carrier noise performance are basically determined by the selectivity of the resonator which can be characterized by quality factor, Q. The quality factor, Q is usually defined as 2π times the ratio of the stored energy and the dissipated energy per cycle for resonator based oscillator,

$$Q = 2\pi \cdot \frac{Energy\ stored}{Energy\ dissipated\ per\ cycle} \tag{2.3}$$

This definition is not only valid for electronic resonator-based oscillators, but is also applied to some photonic and mechanical oscillators. Q can be directly related to frequency selectivity as the ratio of the center frequency and the two-sided -3dB bandwidth ($\Delta\omega$),

$$Q = \frac{\omega_o}{\Delta\omega} \tag{2.4}$$

It is noted that the frequency of oscillation is determined by the phase characteristics of the feedback loop. The loop oscillates at the frequency for which the phase is zero. It follows that the stability of the oscillating frequency will be determined by the manner in which the phase $\phi(\omega)$ of the feedback loop varies with frequency. A "steep" function $\phi(\omega)$ will result in higher frequency stability. When there is a change in phase $\Delta\phi$ due to a variation in one of the circuit components, If $(d\phi)/(d\omega)$ is large, the resulting change in ω_o will be small, as illustrated in Fig. 2.3 [SeSm91]. Thus, Q can be defined as,

$$Q = \frac{\omega_o}{2} \cdot \frac{d\phi}{d\omega} \tag{2.5}$$

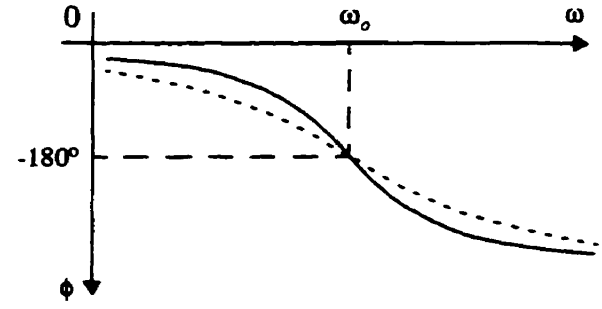


Fig. 2.3. Dependence of oscillator frequency stability on the slope of the phase response

The phase noise observed at the output of oscillator is a function of: (1) sources of noise in the circuit (e.g., thermal and flicker noise of transistors), (2) sources of noise externally and (3) how much the feedback system rejects (or amplifies) various noise components. According to Leeson linear noise model [Lee66], the oscillator phase noise is

$$S_\phi = S_\theta(\omega)\left(1 + \frac{\omega_o^2}{4Q^2(\Delta\omega)^2}\right) \cong \frac{\omega_o^2}{4Q^2(\Delta\omega)^2} \cdot \frac{P_{noise}}{P_{carrier}} \tag{2.6}$$

where $S_\theta(\omega)$ is the equivalent input noise power spectral density.

The equation illustrates three fundamental rules for low noise oscillator design: (a) use high-Q passive resonators; (b) minimize the number of active and lossy passive devices in the oscillation path; (c) maximize the oscillation swing.

2.2.1.2 Negative Resistance Principle

An alternative interpretation of an oscillator circuit is based on the negative resistance concept. It is the function of the amplifier to maintain oscillation by supplying an amount of

energy equal to that dissipated. This source of energy can be interpreted as a negative resistor in series with the resonator as shown in Fig. 2.4 [Rob95]. If the total resistance is positive ($Re(Z_L + Z_R) > 0$), the oscillations will die out, while the oscillation amplitude will increase if the total resistance is negative ($Re(Z_L + Z_R) < 0$). To maintain oscillation the two resistors must be of equal magnitude ($Re(Z_L + Z_R) = 0$). The operating frequency is determined by

$$Im(Z_L + Z_R) = 0 \tag{2.7}$$

In practice, the negative resistance is created by using feedback transistor based circuits.

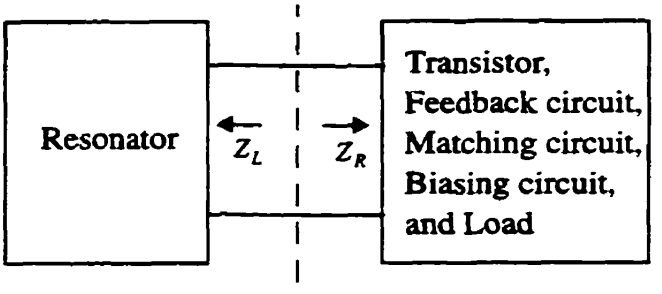


Fig. 2.4. Block diagram of a negative resistance oscillator

2.2.2 VCO Design Considerations

The specifications for a practical VCO depend on applications. However, the general design goals include low voltage operation, low power consumption, monolithic integration, large and linear tuning characteristics, low phase noise, good supply and substrate noise rejection, good temperature stability and low fabrication cost.

Phase noise generated by the oscillator at the transceiver can significantly affect the performance in digital and analog communication systems. In a PLL, VCO phase noise

components within the loop bandwidth can be greatly suppressed by the loop feedback characteristics. However, at large offset frequencies which lie outside the loop bandwidth, VCO phase noise is not corrected by the loop feedback characteristics. If integrated with digital circuits, VCOs must be highly immune to supply and substrate noise, e.g., the frequency divider can corrupt the VCO output by injecting noise into the common substrate. Such effects become more prominent if a PLL shares the same substrate and package with a large digital processor.

The tuning range of a VCO must accommodate application frequency range as well as process, power supply and temperature induced variation. Monotonicity of the frequency control characteristic is necessary to achieve loop stability. A linear frequency control characteristic is important for PLL FM demodulators. The variation of K_{vco} (gain factor in Hz/V) introduces harmonic distortion in the detected signal and must be below 1%. In other applications, this nonlinearity degrades the loop stability but it can be as high as several tens of percent.

2.2.3 Monolithic LC Oscillators

Fig. 2.5 shows a general circuit diagram of LC-tuned oscillators. The transconductance G_m implements a negative resistance to compensate for the losses in inductor, capacitor and loading. According to the Barkhausen criterion, oscillation will occur at the frequency at which the magnitude of the loop transfer function drops to one and the phase shift becomes equal to zero. Oscillation frequency can be tuned with an on-chip varactor or using characteristics inherent in the circuit configuration [NyMe92]. Varactor-controlled VCOs are attractive since an on-chip junction capacitance with a known temperature dependence can be compensated with an on-chip bandgap reference to cancel the temperature dependence of the VCO centre frequency [SoMe89].

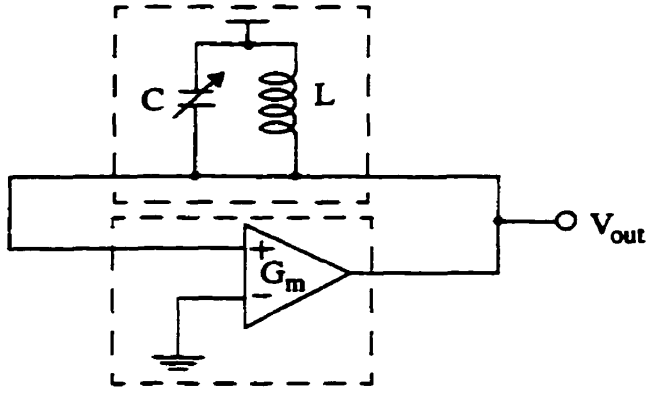


Fig. 2.5. General circuit diagram of a LC-tuned oscillator.

A number of different configurations can be used to realize an LC oscillator circuit such as the Colpitts, Hartley and Clapp Oscillator (which is a variation of Colpitts). The Colpitts oscillator uses the capacitively tapped resonator which is compatible with IC implementation. It has good phase noise performance and is popular in wireless applications.

In monolithic LC implementations, both inductors and varactors suffer from a low Q. The Q of inductors is limited by three mechanisms [LoCo97] [Raz972]: metal line resistivity, capacitive coupling to the substrate, and magnetic coupling to the substrate. At high frequencies, the conductor resistance increases due to the skin effect. Capacitive and magnetic coupling to the substrate are pronounced in silicon technologies with heavily-doped substrates (low resistance), yielding a saturation of Q. The methods employed to improve Q are summarized in Table 2.1.

Table 2.1 Q improvement techniques for monolithic inductors

Reducing series resistance of inductor metal by using	
copper or gold material	Neg94, BES98
thicker metallization	Ash96
stacking of metal layers in a multilevel metal process	BSJ96
Reducing the loss to the substrate	
thicker field oxide	Lar96
high-resistivity silicon substrates	Ash96
removal of silicon from beneath the inductor by chemical etching	CAG93
using patterned ground shield	YuWo97

Even with high Q inductors, the realization of a low series resistance, wide range varactor is difficult. In CMOS technology, grounded and floating varactor diodes exhibit significant resistance arising from the p-substrate and the n-well.

There is a trade-off between the phase noise and the tuning range for monolithic LC VCOs, especially at low supply voltages [Raz971]. To lower the relative phase noise at a given power dissipation, it is desirable to increase the value of the inductor (The upper bound on the value of L is determined by its self-resonance frequency). Considering the substantial parasitic capacitance of the inductor and the transistor(s), it is noted that the variable component of the LC tank capacitance is quite small. At low supply voltages and with large oscillation voltage swings, this component cannot be varied by more than roughly 50%, giving a tuning range of approximately 10%. Table 2.2 summaries some recent literatures on monolithic LC oscillator design and performance.

Table 2.2 Summary of recent publications on monolithic LC oscillator design

Process	Structure & Area (mm^2)	VDD (V)	f_o (GHz)	Tuning Range (MHz)	Power / Output	Phase Noise (dBc/Hz)	Reference
AlGaAs/ GaAs HBT	Single/ 2.16	2.5 -	15	600 (4%)	75mW/ 2dBm	-85 @100kHz	Yama92
BiCMOS 10 GHz	Single/ 0.2	5 -	1.75	200 (11%)	70mW/ -25dBm	-88 @100kHz	NgMe 92
CMOS 0.7 um	Diff./ 5.18	3 2.5(min.)	1.76	79.2 (4.5%)	24mW/ -35dBm	-107 @100kHz	CrSt95
BiCMOS 20 GHz	Diff./ -	3 2.7(min.)	2.048	-	3mW/ -25dBm	-74 @100khz	AyRa95
BiCMOS 12 GHz	Single/ 0.5	3.6 2.6(min.)	2.36	-	54mW/ 13.5dBm	-92 @1 MHz	Soyu96
NMOS 0.5 um	Diff./ -	3 2.3(min.)	4	9%	24mW -	-85 @100kHz	SJBH96
Bipolar 25 GHz	Diff./ -	3 2.7(min.)	0.913	-	10mW/ -3dBm	-101 @100kHz	AlTh96
CMOS 1 um	Diff./ -	3 -	0.85	120 (14%)	30mW/ -25dBm	-85 @100kHz	Rofo96
BiCMOS 11 GHz	Diff./ 2.5	3.6 2.5(min.)	1.476	150 (10%)	12mW/ -6.6dBm	-105 @100kHz	DCS97
CMOS 0.6 um	Diff./ -	3.3 -	1.8	120 (6.6%)	7.6mW/ -	100 @500kHz	Raz971
Bipolar 15 GHz	Diff./ 0.96	5.5 2.7(min.)	2.2	250 (11.4%)	- -3dBm	-99 @100kHz	JNL97

2.2.4 Relaxation Oscillators

In contrast to LC oscillators, relaxation oscillators require only one energy storage element, and rely on the threshold switching characteristics of the circuit rather than on a frequency selective element to define an oscillatory waveform. These circuits have become common because they can be easily implemented monolithically and take small die size.

However, due to their broad-band nature, these oscillators often suffer from large random fluctuations in the period of their output waveforms, termed the timing jitter.

A common system topology for a relaxation oscillator is given in Fig. 2.6. The integrator is usually a capacitor with a current source. The Schmitt trigger is a regenerative circuit with memory. The sign switch controls whether the capacitor should be charged or discharged. There is a feedback loop from the capacitor voltage back to the charging current. The oscillator operates by sensing the capacitor voltage and reversing current through it when this voltage exceeds a predetermined threshold. In principle this is a negative feedback loop that tries to suppress variations of the capacitor voltage. This loop has a pole at the origin. It is the hysteresis of the Schmitt trigger that prevents this loop from latching at a constant capacitor voltage. Relaxation oscillators can be divided into three basic classifications [Gre84]: (a) RC relaxation oscillators, (b) constant current charge-discharge oscillators and (c) emitter-coupled multivibrator. Table 3.3 summaries some recent literatures on relaxation oscillator design.

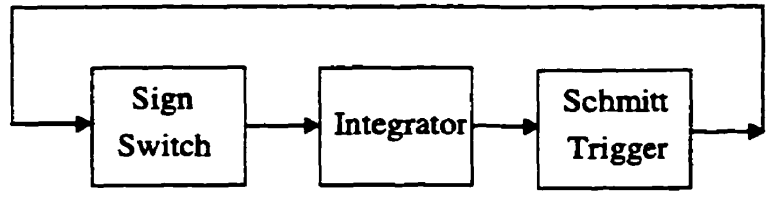


Fig. 2.6. A common topology for relaxation oscillators

Table 2.3 Summary of recent publications on monolithic relaxation oscillator design

Process	f_o (MHz)	Vcc (V)	Power (mW)	Timing Cap. (pF)	Tuning Range (MHz)	Temperature Stability (ppm/C°)	Phase Noise (dBc/Hz)	Reference
BiCMOS 2 um	128	5	25	-	1-128	50	-	Kato88
NMOS 0.5 um	1000	3	50	-	1000	-	-	Banu88
Silicon Bipolar 9 GHz	90	5	-	-	3-90	-	-	KHNK91
Silicon Bipolar 3 GHz	200	8	232	3	0-500	-	-121@ 1MHz	Ver92
Silicon Bipolar 0.8um	5000	3.6	70	0.1	1.99-7.4 GHz	1100	-	SoWa92
CMOS 1.2 um	80	5	20	-	0-80	99	160ppm	FiLi92
NMOS	190	-	10	-	60-250	200	-	CWC92

2.2.4.1 RC Relaxation and Constant Current Charge-Discharge Oscillators

An RC relaxation oscillator is composed of timing elements R_1, R_2, and C_1, a Schmitt trigger, and a grounding switch. A simplified circuit using a single-comparator Schmitt trigger is shown in Fig. 2.7(a) [Gre84]. The output changes state when the input voltage reaches a upper switching threshold, and reverts back to the original state when the input reaches a lower switching threshold. The stability of this circuit depends on the accuracy and stability of the threshold levels for the Schmitt trigger. The use of a dual-comparator Schmitt trigger results in some improvement in stability and high frequency capability. At frequencies above a few hundred kilohertz, switching delays in the comparator and flip-

flop sections will reduce the accuracy and stability of the oscillations, limiting the high frequency capability of this circuit.

The constant current oscillator is a variation of the RC relaxation oscillator. Current sources are used to charge and discharge the timing capacitor. The basic circuit configuration is shown in Fig. 2.7(b). C is charged by the current source I_1 until the upper threshold of the Schmitt trigger is reached, at which time its output changes state and turns on current sources I_2, discharging C. The operation repeats itself, producing a rectangular waveform at the output. This circuit lacks the high frequency capability of the emitter coupled oscillator due to switching delays associated with the Schmitt trigger circuit.

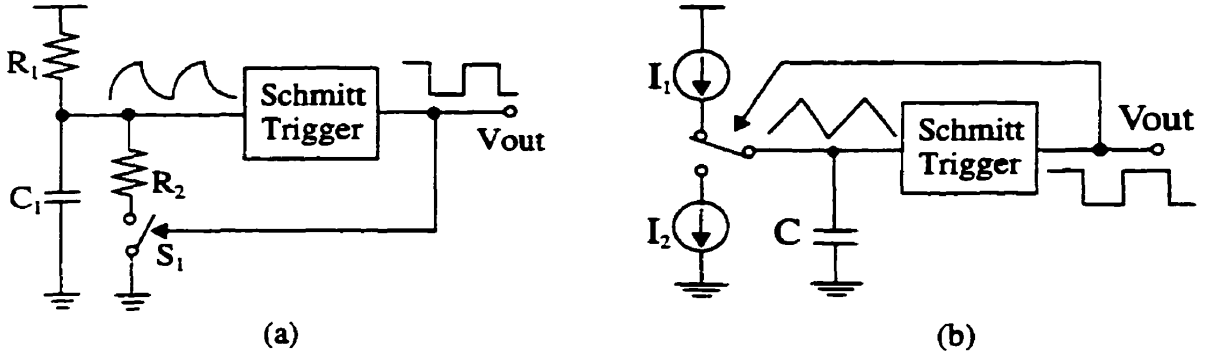


Fig. 2.7. (a) RC relaxation and (b) constant current charge-discharge oscillators

2.2.4.2 The Emitter-Coupled Multivibrator

The most popular relaxation oscillator circuits is the emitter-coupled multivibrator with a floating timing capacitor as shown in Fig. 2.8, which uses bipolar transistors as the active devices [Gre71]. It is a completely symmetric circuit which guarantees a duty cycle close to 50 percent. The timing capacitor (C) is alternatively charged and discharged by a constant current, I. The peak voltage across the timing capacitor alternates between $+V_{BE}$ and $-V_{BE}$ as the circuit oscillates between two astable states. The oscillation period is deter-

mined by the change in potential across the capacitor due to the constant current and the time (t_s) required by regenerative switching of the circuit,

$$T = \frac{4V_{BE}C}{I} + 2t_s \tag{2.8}$$

If the switching time of Q1 and Q2 is negligible compared to the charging or discharging time of the capacitor then the oscillation frequency is linearly related to the current I. The emitter-coupled multivibrator exhibits the highest reported oscillation frequency up to 7.4 GHz in the silicon bipolar process [SoWa92]. This circuit has been modified for greater stability against temperature drifts [Kato88] and other types of active devices are used, but in essence it is always equivalent to Fig. 2.8. For example, in [FlLi92] the single floating capacitor was replaced with two grounded capacitors in CMOS technology to improve duty cycle and reproducibility.

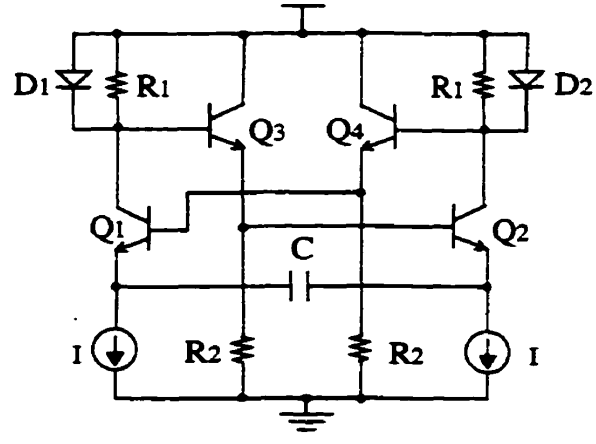


Fig. 2.8. Emitter-coupled multivibrator with floating timing capacitor

2.2.5 Ring Oscillators

A ring oscillator is realized by placing an odd number of inverting amplifiers in a loop as shown in Fig. 2.9. The simplest type of amplifier that can be used is a simple digital

inverter. The circuit intrinsic grounded parasitic capacitors are utilized as the charging and discharging capacitors which increase the attainable oscillating frequency. A minimum of three stages should be used to ensure reliable oscillation. This would make the total phase shift around the loop sufficient to allow complete switching in each stage. Each half-period, the signal will propagate around the loop with an inversion. When differential inverters are used, the number of stages in the ring need not be odd: an even number of inverters can be used and the inversion required around the loop can be achieved by simply interchanging the outputs of the last inverter before feeding them back to the input. Assuming each inverter has a delay of τ_d and that there are N inverters in the loop, we then have oscillation frequency,

$$f = \frac{1}{T} = \frac{1}{2N\tau_d} \tag{2.9}$$

By making the delay of the inverters voltage or current controlled, the ring oscillator's frequency can be tuned. The ring oscillators have the advantage that they do not require any kind of resonator and have a large tuning range, but their frequency and phase characteristics are somewhat poorer than those of high Q resonator-based approaches due to poor frequency selectivity and high number of active devices in the oscillation path. Table 2.4 gives a summary of the research work on monolithic ring oscillators. They are compared in terms of technology, structure and performance.

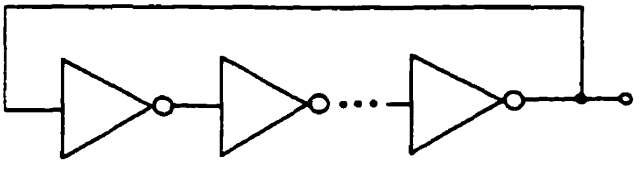


Fig. 2.9. Ring oscillator with N stage inverters

Table 2.4 Summary of recent publications on monolithic ring oscillator design

Process	Oscillator Structure	f_o (MHz)	Vcc (V)	Power (mW)	Tuning Range (MHz)	Timing Jitter or Phase Noise	Reference
CMOS 1.0um	single	320	5	-	110	-	EnAb90
AlGaAs/ GaAs(HBT)	diff.	6000	8	300	800	<1° rms	BMOK92
NMOS 1.0um	diff.	1100	5	-	-	-	EnAb92
CMOS 0.8um	diff.	220	5	-	10-220	-	YGW92
BiCMOS 1um, 20GHz	diff.	6000	2	-	700	-	RaSu94
CMOS 1.2um	single	800	5	6.5	125	-95 dBc/Hz @100kHz	KwAb95
CMOS 0.8um	diff.	1690	5	120	1600	-	JCSC97

A number of different configurations can be used as inverter/delay cells in a ring oscillator. However two group of VCO cells are most commonly used: the single-ended current-starved inverter (e.g., Fig. 2.10(a), (b), (c)) and the differential-pair inverter (e.g. Fig. 2.10(d), (e), (f)).

In Fig. 2.10(a) the two symmetric current sources are controlled by the biasing voltage [JBHK87] [WLS89]. To compensate for the asymmetry due to the difference in the mobility of electrons and holes, a width ratio is maintained in all the delay cell. In Fig. 2.10(b) the controlled PMOS current sources are used as loads which are in saturation for the most part [Raz95]. The transconductance of the PMOS transistors can be minimized to reduce their contribution to the phase noise. In Fig. 2.10(c) the delay cell combines an inverter in parallel with a voltage controlled resistor which permits the oscillator to be tuned over a suitable range [KwAb95]. The sizes of transistor M2 and M3 define the minimum and

maximum operation frequency, respectively.

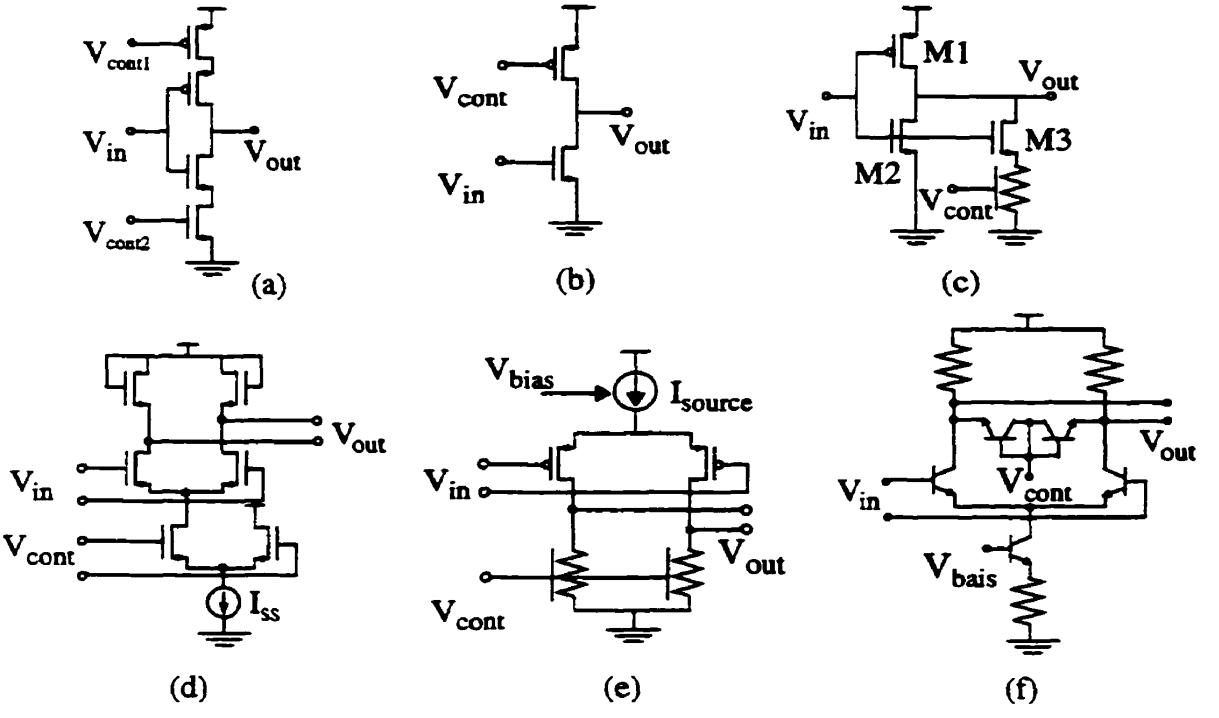


Fig. 2.10. Delay cell structures with a programmable delay

A fully differential inverter with a programmable delay is shown in Fig. 2.10(d). Both the signal path and the control path are differential to achieve high common-mode rejection [Raz96]. In Fig. 2.10(e) the delay cell is based on a PMOS source-coupled pair with voltage-controlled resistor (VCR) load elements [YGW92]. The use of PMOS devices makes the signals referenced to Vss, eliminating frequency shifts due to nonlinear drain junction capacitance. Tail current sources are cascoded for high impedance to V_{DD}. A BJT differential pair used as delay cell is shown in Fig. 2.10(f) [BMOK92]. The control voltage changes the oscillating frequency by varying the load capacitance of reversed biased base-emitter junctions. Additionally, the bias current adjusts the centre frequency to account for process and temperature variations.

2.3 PLL Based Clock Recovery

In many systems, data is transmitted or received without any additional timing reference. Timing information is derived directly from the received data in order to reduce hardware complexity, transmission bandwidth, and power consumption. For example, an optical communication receiver consists of an optoelectronic converter (photo-detector), preamplifier and equalizer, clock recovery circuit and data regenerator as illustrated in Fig. 2.11 [BMOK92][SuYi90][SuYi91]. The preamplifier and equalizer compensate for distortion introduced during transmission, and amplify the signal to the level required by the regenerator circuit. The regenerator is triggered by the timing clock in order to sample the received signal and decide whether a 1 or 0 pulse was transmitted. The function of the clock recovery circuit is to maintain uniform spacing of the regenerated pulses and to define the best time to sample the equalized pulse train in terms of the received signal-to-noise ratio.

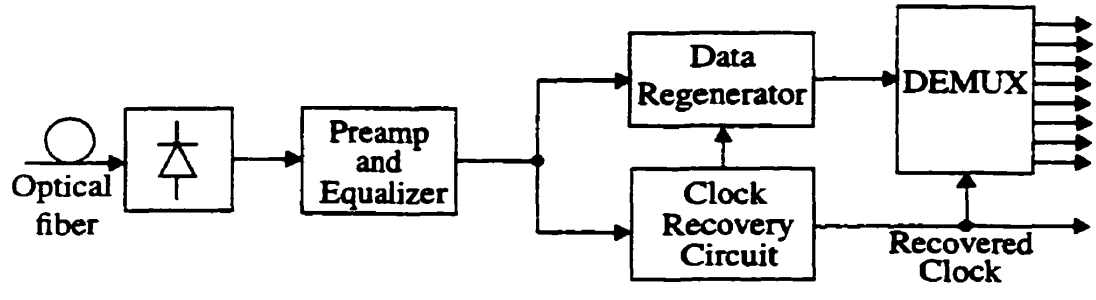


Fig. 2.11. Simplified block diagram of a fiber-optic digital receiver

The spectrum of the transmitted NRZ signal is a continuous ($\sin x/x$) function with a notch at the clock frequency. The conventional approach to this problem is to pass the NRZ signal to a NRZ-to-RZ converter to produce a reference signal having a strong component at the clock frequency (a half-bit delay line and a XOR circuit can be used to implement the NRZ-to-RZ converter [Wol91]). Then the newly generated RZ signal is

filtered with a narrow bandwidth filter such as an open loop filter or closed loop synchronizer (PLL). SAW filters have been used as high Q open loop filters to extract the clock as shown in Fig. 2.12. However, the background white spectral density in the vicinity of f_c will also pass through the filter, corrupting the clock. An open loop filter does not itself have the ability to adjust to the bit rate deviation from the transmitter port. Furthermore, it is difficult to integrate a high Q filter on the silicon substrate monolithically.

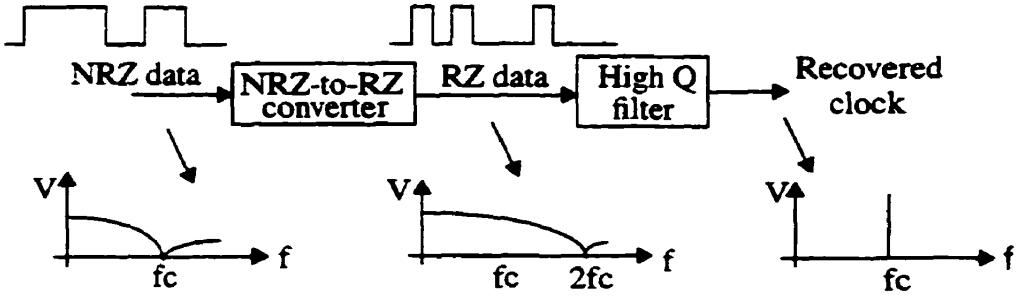


Fig. 2.12. Clock recovery using open loop filter method

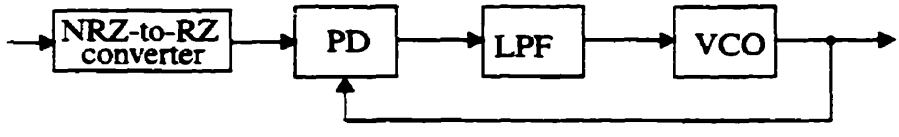


Fig. 2.13. Phase-locked loop based clock recovery

Most clock recovery circuits employ phase locking as shown in Fig. 2.13. A phase detector, loop filter and VCO are connected in a negative feedback configuration. This method generates an output frequency dependent on the DC control voltage at the input to the VCO. The control voltage is derived from the error between average input data rate and VCO frequency. The correction action of the loop forces the VCO to track the input average data rate. The advantage of PLL based clock recovery is that it has the tracking ability

to adjust the bit rate deviation. Furthermore, it can be fully integrated. This is desirable not only for the traditional cost and reliability benefits of monolithic integration, but also because of the excessive cost of packaging high frequency components and the power consumed by package interconnection in a 50 ohm environment.

The application of PLLs to clock recovery has some special design considerations. Hybrid PLL, using a combination of analog and digital components, can be designed in order to improve the performance of a purely analog or purely digital PLL. To minimize the jitter caused by the input noise, the loop bandwidth must be very small compared to the input frequency. This, in turn, reduces the pull-in range available from the loop. The initial VCO center-frequency offset is one of the main contributors to phase error together with the dc offsets in the phase detector and loop amplifier. As a results, it should be minimized against temperature and supply variations [SoMe89]. Both the phase detector and the VCO must be able to work at high frequency. Because of the random nature of data, the choice of phase detectors is restricted: Three state PDs, in particular, will not work. A two-state PD can help to suppress the random data pattern related jitter. A Hogge PD can be used to make it possible to recover clock directly from NRZ data as shown in Fig. 2.14 [Hog85]. With Hogge PD, the data is sampled by the rising clock edge, and the sampled data Q_1 is compared with the data by an exclusive OR. The result is a signal "UP" with pulses whose width goes from zero to T_B as input phase error goes from $-\pi$ to π. The waveform "DN" is needed as a reference to "UP", such that for $\theta_e = 0$, $V_{UP} - V_{DN}$ always has a zero average. Frequency detectors should be included with PDs to form PFDs in order to aid the loop lock acquisition.

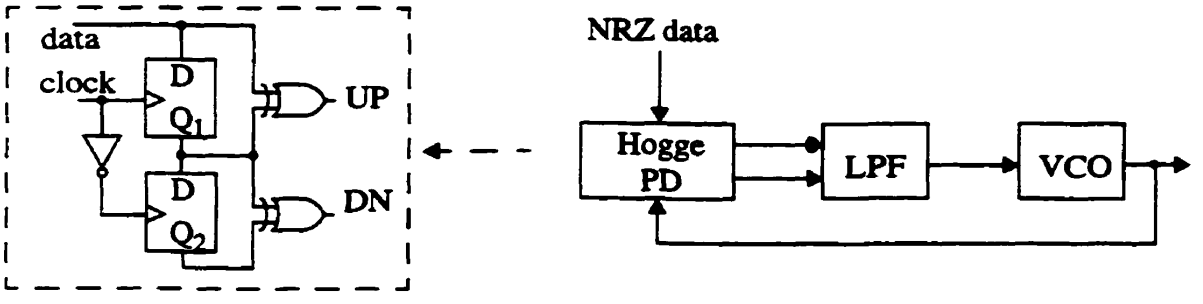


Fig. 2.14. Hogge detector based PLL clock recovery

Different from a conventional PLL which adjusts the phase of the clock to obtain phase alignment with the incoming data, delay-locked Loops (DLL) can be used to shift the input data to align with the clock. A system that does not require an external frequency reference is the combined DLL/PLL as shown in Fig. 2.15 [LeBu92]. The phase detector, loop filter and VCO form the PLL, while the phase detector, loop filter and voltage controlled phase shifter (VCPS) form the core of the DLL. The two loops in the DLL/PLL act in concert to null out phase errors as follows: if the clock is behind the data, the phase detector drives the VCO to a higher frequency and simultaneously increases the delay through the VCPS. Both of these actions serve to reduce the initial phase error since the faster clock picks up phase, while the delayed data loses phase. The combination of DLL and PLL achieve a good jitter filtering without compromising acquisition speed.

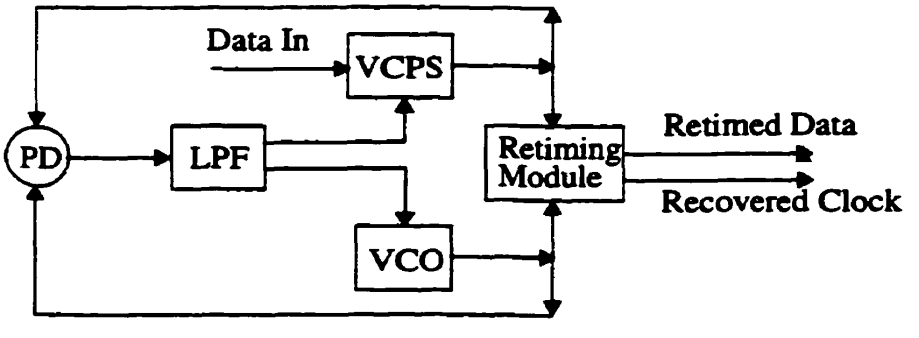


Fig. 2.15. DLL /PLL clock and data recovery

2.4 PLL Clock Generators and Frequency Synthesizers

2.4.1 PLL Clock Generators for Data Communications

Fig. 2.16 shows the simplified block diagram of a data transmitter [SuKw99]. It consists of Parallel to Series Converter (PISO), clock generator, retime unit and line driver. The PISO converts the internal byte serial stream to a bit serial stream. The clock generator provides a clean clock for both PISO and retime unit. The data sent to the transmitter front end from other building blocks may experience large jitter content due to the noise from devices and power supply rails. The transmitter will receive the data stream and synchronize it with a clean clock to generate retimed data. Table 2.5 summaries some recent literature on monolithic CMOS PLL clock generators.

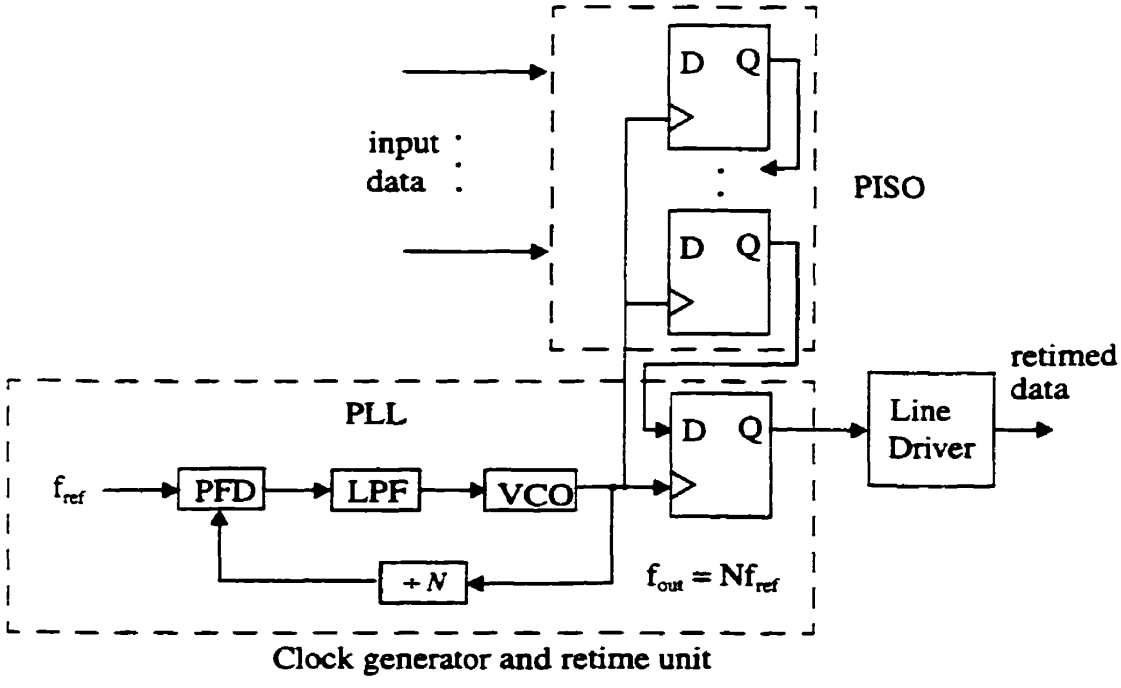


Fig. 2.16. Simplified block diagram of a data transmitter

Table 2.5 Summary of recent publications on CMOS PLL clock generators

Process	VCO Type*	VCO Range (MHz)	Power (mW) Supply (V)	Lock in Time (us)	Jitter (ps)	Area (mm^2)	Reference
CMOS 2.0 um	SE ring (3 stages)	112-209	500 5	NA	NA	1.5 x 3.7	KLS89
CMOS 1.0 um	SE ring (7 stages)	30-128	75 5	NA	50 (rms)	1.35	BiRe92
CMOS 0.8 um	Diff. ring (5 stages)	10-220	16 5	75	300 (P-P)	0.31	YGW92
CMOS 0.8 um	Diff. ring (6 stages)	50-330	800 5	NA	35 (rms) 184 (P-P)	1.25	Horo93
CMOS 0.5 um	SE ring (3 stages)	6-175	10 3.3	15	31 (rms)	0.52	ASGC95
CMOS 0.5 um	Diff. ring (3 stages)	15-240	33 3.3	15	100 (P-P)	0.82	Novo95
CMOS 0.35 um	SE ring (3 stages)	200-600	1.5 1.35	NA	NA	0.21	KAPD96
CMOS 0.5 um	SE ring (3 stages)	28-360	9 3.3	NA	12 (rms) 80 (P-P)	0.6 x 1.3	ZDL96
CMOS 0.8 um	SE ring (3 stages)	0.3-165	NA 5/3	NA	13 (rms) 81 (P-P)	NA	YLC97

*SE: single-ended ring oscillator; Diff: differential ring oscillator

2.4.2 PLL Frequency Synthesizers for Wireless Communications

Frequency synthesizers are widely used as local oscillators to provide accurately defined frequencies and channel selection for wireless transceivers. Some of the design considerations for frequency synthesis in wireless application include: frequency accuracy; phase noise; sidebands; switching time and sensitivity to noise [Craw94][Raz972].

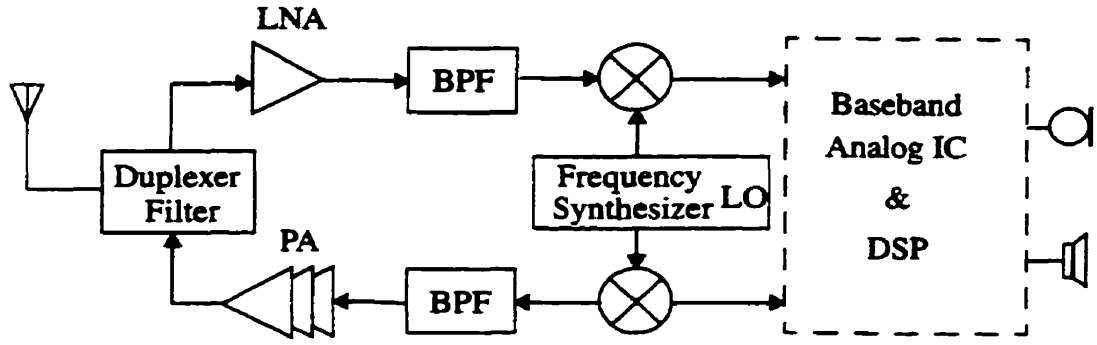


Fig. 2.17. A simplified block diagram of RF transceiver

Frequency synthesis techniques can be classified into two major categories: direct synthesis and indirect synthesis. Each category can be subdivided into several different techniques, as shown in Fig. 2.18.

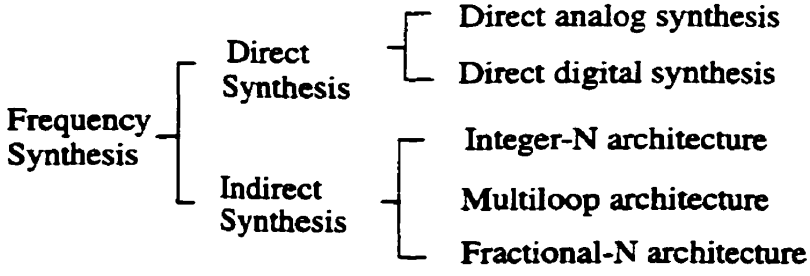


Fig. 2.18. Frequency synthesis techniques

Direct frequency synthesizer architectures utilize no feedback to generate the appropriate output frequencies. In a direct analog synthesizer (DAS), fixed precise frequency sources are combined with frequency multipliers, mixer, dividers, switches and filters to generate the necessary output frequencies. The advantage of the direct synthesizer approach is that the fundamental waveform can be generated using a clean source, such as a crystal oscillator. Thus, the phase noise characteristics of the resulting higher frequency

waveform can be excellent. However, direct analog synthesis has a number of drawbacks. The physical size of the components required to implement the multipliers, dividers, mixers and filters grows dramatically when multiple frequency output and/or fine frequency control is required. Furthermore, these synthesizers can generate significant level of spurious frequency components. They must be carefully filtered by a high Q band-pass filter which is very difficult to integrate monolithically. Thus, DAS is considered as unsuitable for mobile handset application.

Direct digital synthesis (DDS) produces a signal in the digital domain and utilizes digital-to-analog conversion (DAC) and filtering to reconstruct the waveform in the analog domain. As illustrated in Fig. 2.19, DDS employs a phase accumulator to produce a binary word indicating instantaneous phase which is then mapped to instantaneous amplitude in a look-up read-only memory (ROM) [Craw94]. As the input value, K (L bit binary word), increases, so does the rate at which the accumulator overflows, thus yielding a higher frequency for the output sinusoid.

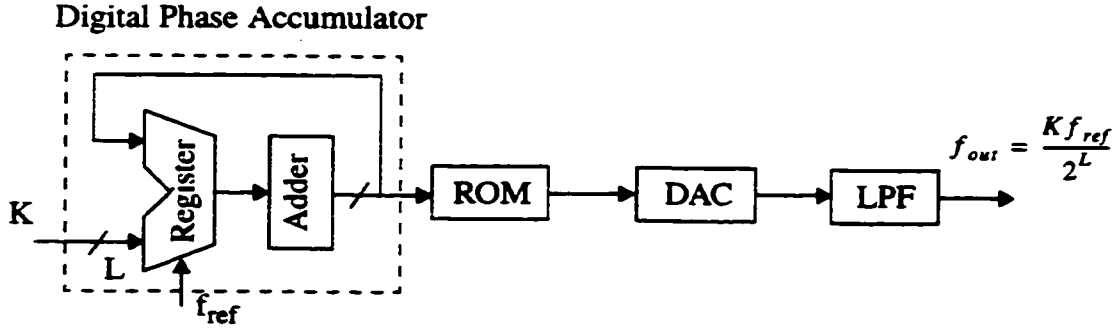


Fig. 2.19. Direct digital synthesis (DDS)

DDS provides a number of advantages: ease of monolithic integration, fine frequency steps, fast channel switching (which is important for frequency hopping in spread spectrum systems), and provision for direct modulation (e.g. GMSK, QPSK etc.). The phase

noise performance of a DDS is determined by the phase noise of the clock as well as quantization noise introduced by the sine look-up table and the DAC. Low close-in phase noise can be achieved with a high oversampling ratio. However the output spectrum suffers from spurious response and harmonic distortion due to DAC nonlinearites. Speed issues have limited the use of DDS in the RF range, especially if power dissipation is critical. This is due to the Nyquist criterion which requires the clock frequency to be at least twice the output frequency. (In order to relax the LPF rejection requirements, the clock frequency is typically about three to four times the maximum output frequency).

2.4.2.1 Multi-loop and Hybrid Architectures

A PLL incorporating a programmable integer-N divider in the feedback path can operate as a synthesizer. The minimum channel span (resolution) is equal to the reference frequency. Low reference frequency results in a narrow loop bandwidth, inadequate phase noise suppression and longer settling time.

The relationship between the channel spacing and the reference frequency of integer-N synthesizers can be altered by employing two (as shown in Fig. 2.20) or more loops. In two loop architecture, the loop bandwidth of the first PLL can be kept high due to large reference frequency and fixed divider ratio. Thus, the phase noise problem is relieved. The second PLL performs the tuning function, but its impact on output phase noise is small since it operates at a much lower frequency. This technique achieves high resolution while maintaining a fast switching speed and optimum noise performance. Synthesizers that combine the features of various synthesis methods are called hybrid. Most hybrid structures use a DDS to replace the slower PLL or reference frequency generator. However, the overall complexity and power consumption of the synthesizer increases.

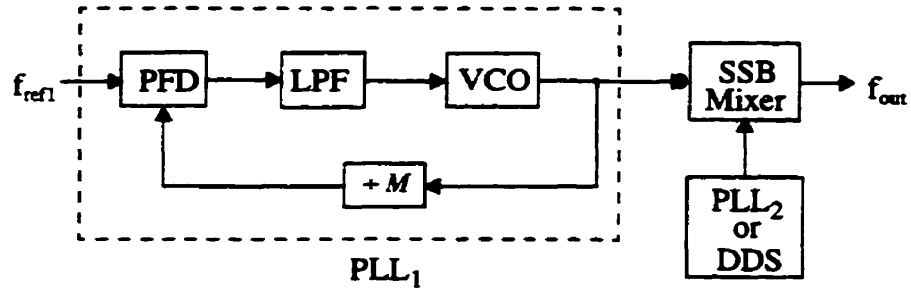


Fig. 2.20. Dual-loop or hybrid architecture

2.4.2.2 Fractional-N Architecture

Fractional-N indirect frequency synthesis based on a PLL (as shown in Fig. 2.21) is particularly well suited to wireless applications and integrated circuit implementations. The technique allows very narrow channel spacing relative to the output frequency, large loop bandwidth in the PLL relative to the channel spacing, and high output frequency relative to the processing technology used in the IC fabrication [Rho83]. To realize fraction-N division function, the multi-modulus frequency divider (MMD) can be controlled by several techniques: pulse swallowing phase interpolation [Has84], Wheatley random jittering [Whea83] and Delta-Sigma ($\Delta\Sigma$) modulation [Jaq90][Dong92][RCK93]. The use of $\Delta\Sigma$ modulation concepts in modulus controllers results in a beneficial noise shaping of the phase noise (jitter) introduced by fractional-N division. Noise in the vicinity of the divided carrier frequency is small and noise at the higher offsets can be suppressed by the lowpass filter following the phase/frequency detector. The technique is capable of achieving low phase noise, good spurious frequency suppression while providing fast settling time, desirable channel resolution and wide tuning bandwidth.

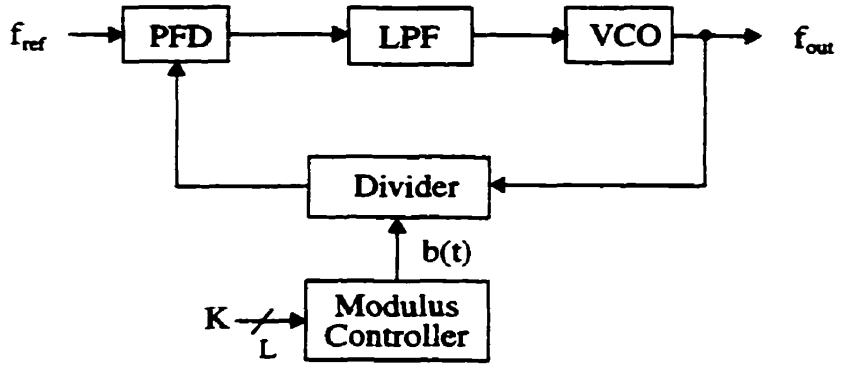


Fig. 2.21. Fractional-N frequency synthesizer

The choice of appropriate high order $\Delta\Sigma$ structure requires the consideration of many factors including noise shaping, spurious content of the output spectrum, output levels, loop filter order and circuit complexity [SuKw991]. The output noise spectral density of higher order structures monotonically increases at greater rates per unit frequency, resulting in greater SNR or bit resolution per given baseband bandwidth at lower frequencies. However, the price to be paid for this is that a higher order of band noise levels requires a corresponding higher order of loop filter being implemented in the PLL. Typically, the loop filter is set one order higher than the order of the modulator to produce the necessary suppression of quantization noise generated by the modulator. Furthermore, the high order $\Delta\Sigma$ modulators increase the complexity of circuits, thus increasing chip size and power consumption.

2.5 Summary

The oscillator is one of the most important components in analog RF circuits. Although the operation principles of oscillators are basically quite simple and straightforward, there are design considerations when tight specifications must be met. Current wireless and data

communication systems require low phase noise, wideband tunable oscillators with sufficient output power and efficiency. Although there are many different types of active devices, resonators and circuit topologies that can be used, the choices are usually limited by other factors such as size, cost, operating frequency, supply voltage, power consumption and reliability.

High-frequency and RF/microwave voltage/current controlled oscillators can be implemented monolithically with LC oscillators and ring oscillators. Monolithic LC oscillator using spiral inductors can achieve low phase noise but have relatively narrow tuning range and take a large silicon area. Considerable effort has been expended in develop high-Q monolithic inductors. Ring oscillators exhibit relatively large phase noise due to poor frequency selectivity and contain many noisy devices in the oscillation path. However, ring oscillators exhibit wide tuning range, high speed and ease of monolithic integration and take a small chip size. They can provide quadrature or multiple phase output signals which are important for PLL based modulation systems, clock recovery and high speed sampling systems. The development of technique and design methodology to improve speed (operation frequency), phase noise while maintaining low power is a major challenge for both monolithic CMOS oscillator and PLL design.

CHAPTER 3

Design and Analysis of GHz Monolithic CMOS Ring Oscillators

3.1 Introduction

Ring oscillators are very attractive for multiphase and quadrature clock signal generation required for many timing recovery circuits [EnAb92][RaSu95], modulators/demodulators [Gard85], high-speed sampling systems [KHG90] and microprocessor clock synchronization [JBHK87]. In the Symbolic Processing Using RISC's (SPUR) chip set, for example, a four-phase nonoverlapping clock is used for internal communications [Hil86] and stringent phase relations must be maintained for interchip communication between the central processing unit (CPU) and processor cache controller (PCC). In high speed disk drive applications, a 16 stage differential ring oscillator operating at 30MHz was used to give an effective data sampling rate of 1GHz (32 x 30MHz) as shown in Fig. 3.1 [KHG90]. If a ring oscillator operates at 120 MHz, the effective sampling rate would be 4 GHz.

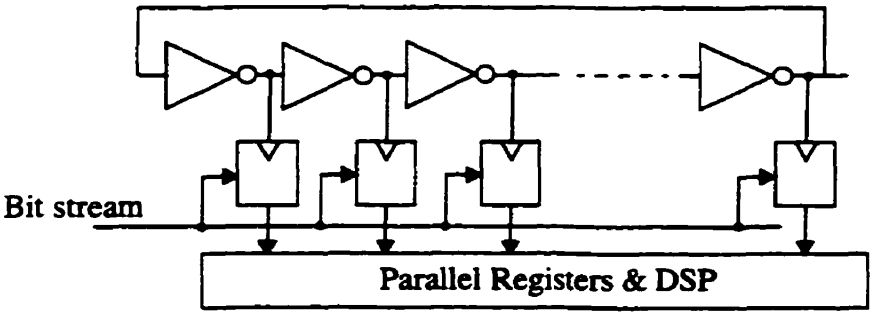


Fig. 3.1. Multiphase sampling with ring oscillator [KHG90]

Since the volume of data traffic in LANs are expanding almost exponentially from one year to the next, high speed operation has become a critical requirement in many data communication transceivers, where the VCO oscillating frequency often limits the maximum obtainable data rate. The oscillation frequency of conventional ring oscillator is determined by the delay of the inverting stages and the number of gates in the oscillator. In order to improve speed, the conventional method is to utilize unavoidable parasitic capacitors as reactive elements and minimize all parasitics by using the delay cell circuits with minimum complexity [ThKw95]. Other techniques have been developed to circumvent the speed limitation. One approach utilizes a four stage ring oscillator where the outputs of the circuit are mixed with each other, and twice the output frequency results (Fig. 3.2) [BuMa91]. An output frequency of four times the ring is available if the V_{out1} and V_{out2} signals are themselves multiplied. Another approach increases the speed by sensing and combining the transition in a ring oscillator to achieve a period equal to two inverter delays (Fig. 3.3) [RaSu94]. However, in both circuits, the number of the multiphase high speed outputs is limited.

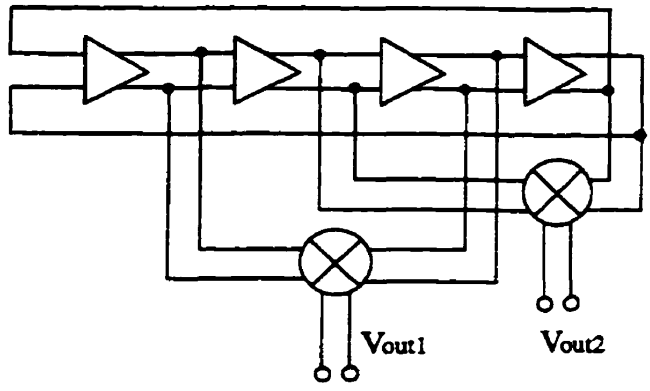


Fig. 3.2. A four stage ring oscillator with quadrature output and doubling frequency [BuMa91]

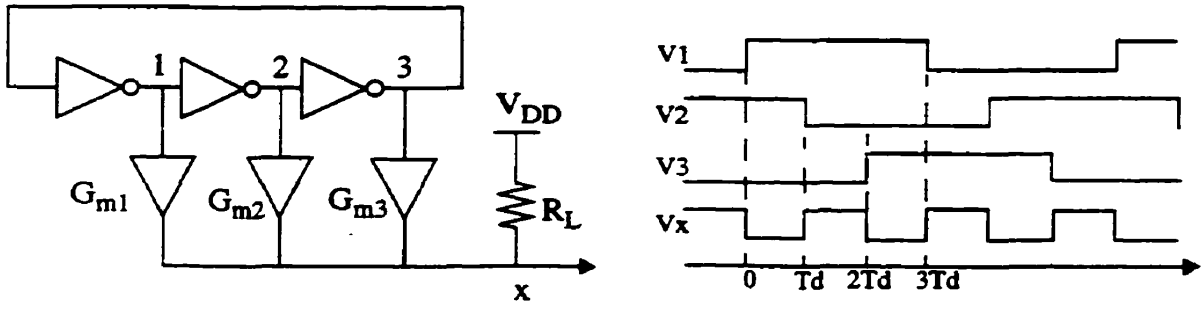


Fig. 3.3. Sensing and combining the transition in a ring oscillator [RaSu94]

To obtain more different phase outputs, more inverter stages are needed at the cost of reducing the maximum available operating frequency. Although a VCO based on two taps delay interpolating was proposed to speed up the circuit as shown in Fig. 3.4 [EnAb86][EnAb92], the phase relationship between inverter stages is not fixed when the control voltage changes.

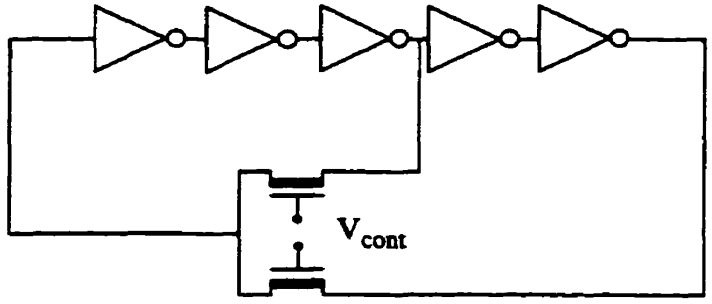


Fig. 3.4. Two-ring oscillators employing potentimetric mixing of feedback signal [EnAb92]

In the next section of this chapter, a general ring oscillator circuit topology capable of achieving high speed operation, multiple phase output and a wide tuning range is introduced. Oscillation frequency formulae are developed based on a linearized model. Possible improvements in operating frequencies are analyzed in both the frequency and time domains. Detailed implementations of the topology are also presented. In Section 3.3, the topology is extended to differential oscillators. A quadrature output ring oscillator based on three-stage sub-feedback loops is proposed and analyzed. Both single-ended and differential ring oscillator circuits are designed and fabricated in a 0.5μm CMOS process. Implementation issues and measurement results for ring oscillators are presented and discussed in Section 3.4. Only key results are presented. Detailed measurements and simulation results can be found in Appendix B.

3.2 High Speed Wide Tuning Range Multiphase Output Ring Oscillators

3.2.1 Topology and Analysis

For a feedback loop with N (odd number) inverter stages cascaded as shown in Fig. 2.9, the oscillation period of the ring is $2N\tau_d$, where τ_d is the delay of each stage. The minimum delay of each stage depends on the process parameters and the size of transistors. The size of transistors affect the delay through its effect on driving strength, self-loading and loading to the previous stage. The improvement in speed can be obtained by circuit optimization. However, the achievable improvement in speed is limited, especially for a long chain of ring oscillators. To solve the conflict between speed and multiphase output, we can split the single feedback loop into N interconnected sub-feedback loops. Each sub-feedback loop contains a minimum number of inverters that can keep a circuit reliably oscillating (e.g., three stage inverters). The overall oscillation frequency is within the range of frequency for a stand-alone three stage ring oscillator and an N stage ring oscillator depending on the control voltage. Thus, a large tuning range and high speed operation can be achieved. The phase relationship between inverter stages remains unchanged due to the symmetrical structure.

Fig. 3.5 shows the proposed general topology of a ring oscillator with sub-feedback loops. The nodes and their interconnections have been correspondingly labeled. We define i as *the feedback index*. It is an integer ($1 \le i < N$) representing the number of inverter delay down the loop from where the feedback signal is derived, e.g., when $i = 2$ we have three stage inverters in the sub-feedback loops.

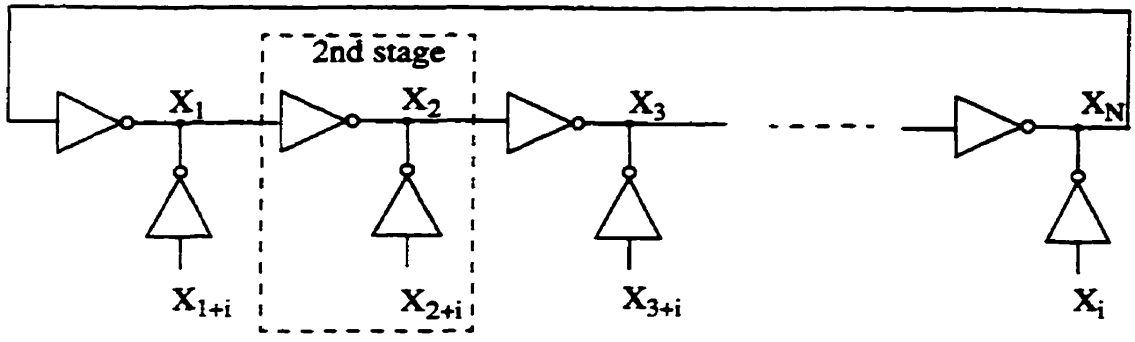


Fig. 3.5. General topology of ring oscillator with sub-feedback loops

Fig. 3.6 shows the block diagram of a five stage ring oscillator with five voltage controlled sub-feedback loops as an example of the topology. Each sub-feedback loop contains three inverters and is established as a fast loop. The main feedback loop (five stages) is the slow loop. The oscillation period can be understood as the weighted sum of delay through the fast loop and slow loop. By adjusting the delay of added inverter cell in fast loops, the frequency of oscillation can be tuned in a range of about 5:3 where we define the range of oscillation as f_{max}/f_{min}.

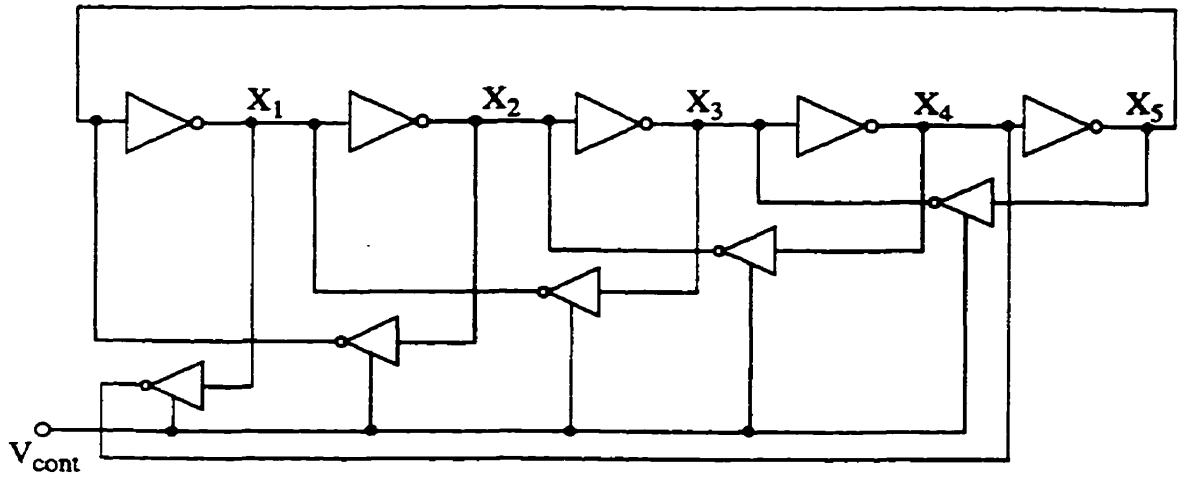


Fig. 3.6. Block diagram of a five stage ring oscillator with sub-feedback loops

To explain the principle behind improved operating frequency in more detail, we model the signal path in the VCO with a linearized circuit, assuming its oscillation amplitude remains small and the waveform is sinusoidal like. Fig. 3.7 shows a combined single stage diagram and its small signal model for first order analysis. R and C represent the equivalent output resistance and the total parasitic loading capacitance at node X_n, respectively. The parasitic load capacitance includes the gate-source capacitance of the input transistor of the following stage, output capacitance of the local stage, which would normally be due to junction capacitance. As well, there is always capacitance from the drain wiring to the substrate.

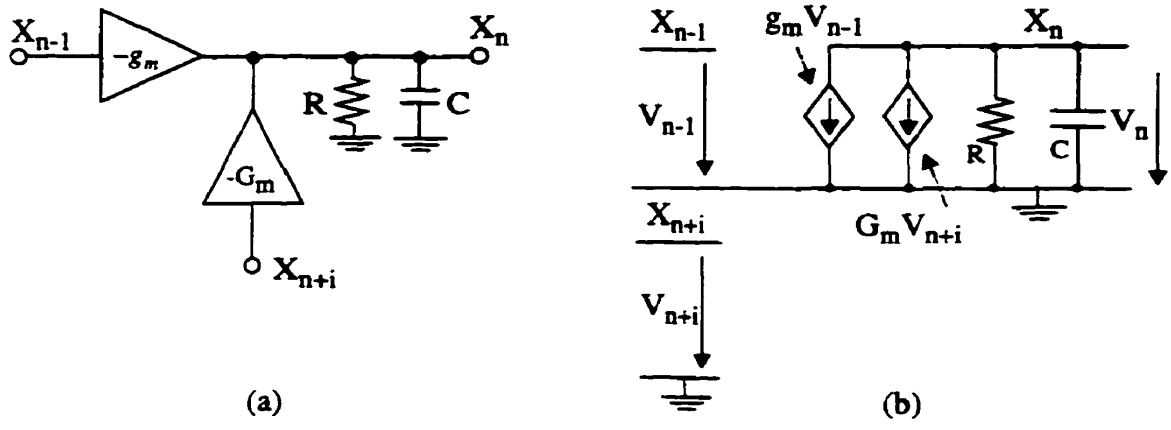


Fig. 3.7. (a) A combined single stage and (b) its small signal linearized model

For a ring oscillator in stable oscillation mode, there is a fixed phase relation between stages. Assuming all stages are the same, the transfer function $H(j\omega)$ of a single stage can be found as

$$H(j\omega) = \frac{V_n}{V_{n-1}} = \frac{-g_m R}{(1 + G_m R\cos\phi) + j(\omega RC - G_m R\sin\phi)} \tag{3.1}$$

where g_m and G_m represent the transconductance of the inverter in the main loop and sub-feedback loop, respectively. Angle ϕ is the phase difference between node (n) and node (n+i).

According to the Barkhausen criterion of oscillation, the ring oscillator would oscillate if, at ω_0, the loop has unity voltage gain and phase shift of 2π or a multiple of 2π. Thus by solving the following equation,

$$\left[\frac{-g_m R}{(1 + G_m R\cos\phi) + j(\omega_0 RC - G_m R\sin\phi)}\right]^{2N} = 1 \tag{3.2}$$

we have

$$\omega_0 = \frac{G_m R\sin\phi + \tan\theta[1 + G_m R\cos\phi]}{RC} \tag{3.3}$$

and minimum required dc gain

$$\begin{aligned} g_m R &= \sqrt{(1 + G_m R\cos\phi)^2 + (\omega_0 RC - G_m R\sin\phi)^2} \\ &= (1 + G_m R\cos\phi)\cdot\sqrt{1 + (\tan\theta)^2} \end{aligned} \tag{3.4}$$

where θ is the phase difference between adjacent nodes (e.g., $\theta = 4\pi/3$, for $N = 3$ and $\theta = 6\pi/5$, for $N = 5$) and we have $\phi = i\theta$.

It should be noted that because of nonlinearity in the active device, the zero-phase frequency is not exactly equal to the steady-state frequency of the oscillator. Nevertheless, it is a good approximation in the analysis of relative frequency improvement. Eq. (3.3) can be rewritten as

$$\begin{aligned} \omega_0 &= \omega_{01} + \Delta\omega = \frac{\tan\theta}{RC} + \frac{G_m R[\sin(i\theta) + \tan\theta\cdot\cos(i\theta)]}{RC} \\ &= \omega_{01} + k_0 G_m / C \end{aligned} \tag{3.5}$$

where ω_{01} is the oscillation frequency of the ring oscillator when $G_m = 0$.

The first term of Eq. (3.5) is the operating frequency of conventional ring oscillator. The second term corresponds to the increment/decrement of the operating frequency. The frequency variation coefficient k_0 in Eq. (3.5) is an important parameter which relates to

the increase or decrease of operating frequency compared to the conventional single-loop ring topology. k_0 is defined as

$$k_0 = \sin(i\theta) + \tan\theta \cdot \cos(i\theta) \tag{3.6}$$

Following is the discussion based on Eq. (3.4) and Eq. (3.5):

3.2.1.1 Increasing the Oscillator Speed

In order to achieve increased oscillation frequency ($\Delta\omega > 0$), k_0 should be positive. Since θ is fixed for a ring oscillator with a given number of stages, whether oscillation frequency is increased or decreased depends on the feedback index i which is the number of delay stages down the loop from where the feedback signal is derived. Table 3.1 lists the corresponding value of k_0 and the feedback index i for N from 4 to 13. The highest values of k_0 are highlighted. The sub-feedback loops can contain even or odd number of inverters. Odd number sub-feedback loop increases the operating frequency, while the even number sub-feedback loops cause a decrease in operating frequency. For a long chain ring, there exists an optimum feedback index i which gives the highest operating frequency.

Table 3.1 Corresponding value of k_0 and feedback index i for N = 4 to 13

i	N=4	N=5	N=6	N=7	N=8	N=9	N=10	N=11	N=12	N=13
1	-1.414	-1.17	-1.0	-0.868	-0.765	-0.68	-0.618	-0.5635	-0.5176	-0.4786
2	**1.0**	**1.175**	**1.15**	**1.08**	**1.0**	0.92	0.85	0.7877	0.7321	0.6830
3	-	-0.726	-1.0	-1.08	-1.08	-1.048	-1.0	-0.948	-0.8966	-0.8476
4	-	-	0.577	0.868	**1.0**	**1.048**	**1.05**	**1.031**	**1.0**	0.9630
5	-	-	-	-0.482	-0.765	-0.922	-1.0	-1.0316	-1.0353	-1.0224
6	-	-	-	-	0.414	0.684	0.85	0.948	**1.0**	**1.022**
7	-	-	-	-	-	-0.364	-0.62	-0.7877	-0.8966	-0.9630
8	-	-	-	-	-	-	0.325	0.5635	0.7321	0.8476
9	-	-	-	-	-	-	-	-0.2936	-0.5176	-0.6830
10	-	-	-	-	-	-	-	-	0.2679	0.4786
11	-	-	-	-	-	-	-	-	-	-0.2465

Taking a 7 stage ring oscillator as an example ($\theta = 8\pi/7$), we have the corresponding value of feedback index i and frequency variation coefficient k_0 as listed in Table 3.1. When sub-feedback loops contain three (i=2) or five (i=4) inverters, $k_0 > 0$, thus, frequency is increased compared to a conventional ring oscillator. A three stage sub-feedback loop (i=2) has a larger k_0 value compared to that of a five stage sub-feedback loop (i=4) which means that a higher operation frequency can be achieved in the i=2 case. However, when sub-feedback loops contain four (i=3) or six (i=5) inverters, frequency is decreased ($k_0 < 0$) compared to a conventional 7 stage ring oscillator.

This can be easily confirmed with HSPICE time domain simulation as shown in Fig. 3.8. A simple single-ended inverter was used as a delay cell in the simulations. The device sizes of inverters in the major loop are 30μm/0.6μm (W/L) and 10μm/0.6μm for PMOS and NMOS, respectively. The device sizes of inverters in the sub-feedback loop are 15μm/0.6μm (PMOS), 5μm/0.6μm (NMOS), respectively. The simulation was run with HP 0.5μm CMOS process parameters and a power supply of 3.3V. It was also observed that although the circuit achieve highest speed when i=2, it produces a sinusoidal like waveform when i=4 (speed is slightly lower than that for i=2). This phenomena will be analyzed and discussed in Chapter 4.

Similar observation can be found for a 9 stage ring oscillator as shown in Fig. 3.9. The highest speed is achieved for i=4 due to the largest value of k_0 (see Table 3.1). For i=6, the waveform is more sinusoidal like with a small compromise of speed compared to that for i=4. The simulation results of operating frequency versus stage number are summarized in Fig. 3.10 for N=5, 7, 9, 11, 13 with the feedback index i as parameter.

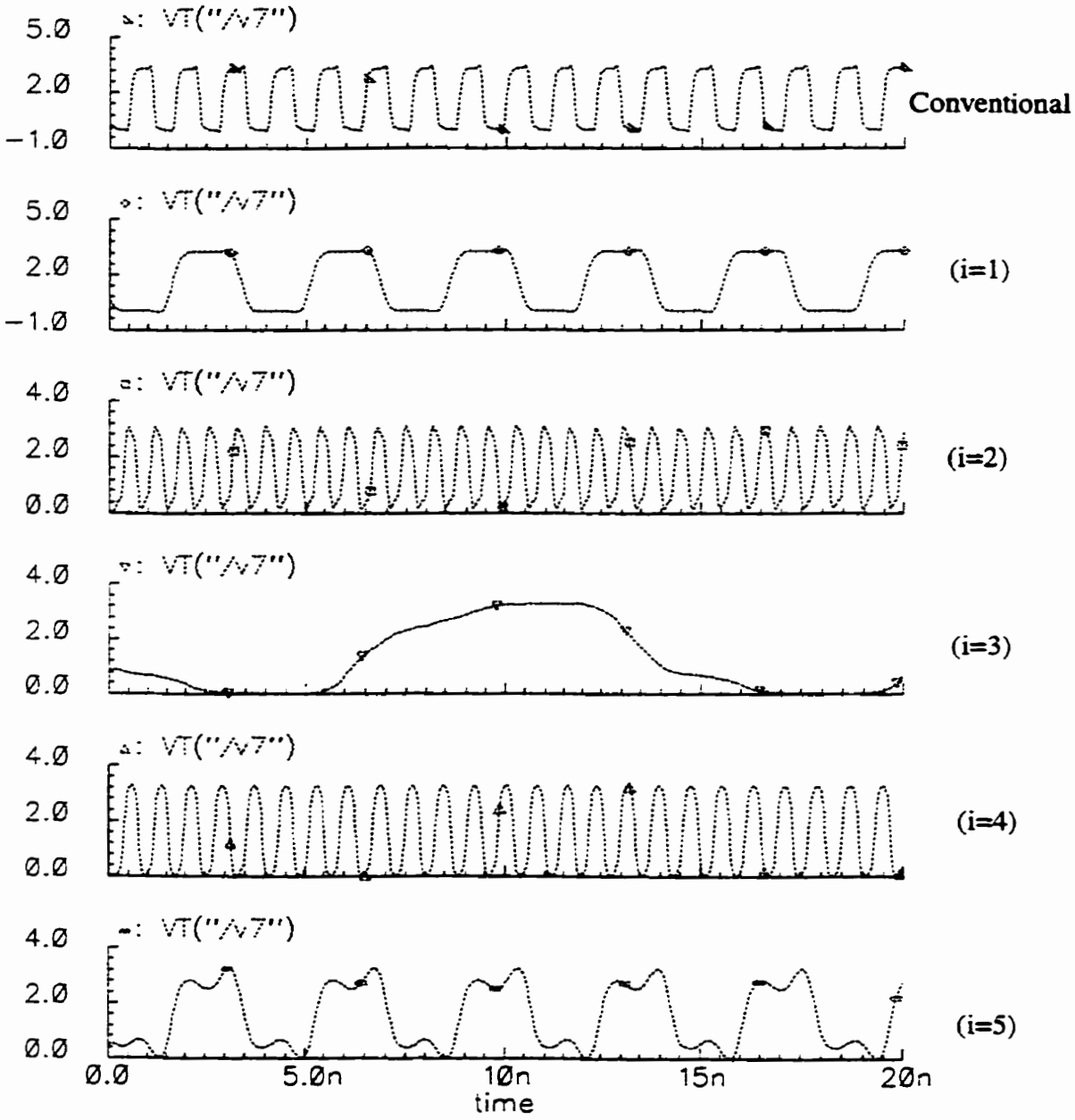


Fig. 3.8. Time domain waveforms for different values of the feedback index *i* (7 stages ring)

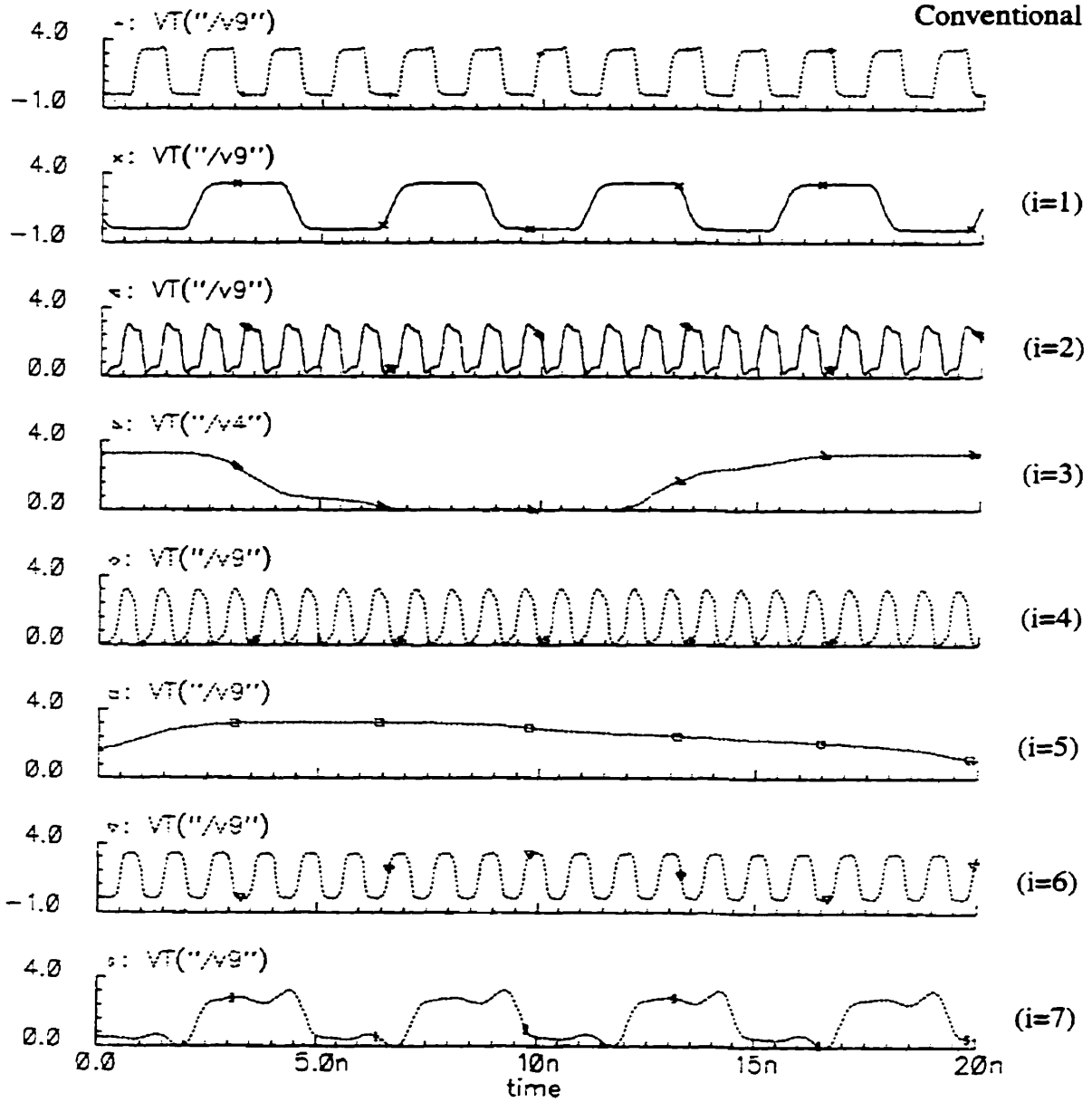


Fig. 3.9. Time domain waveforms for different values of the feedback index *i* (9 stages ring)

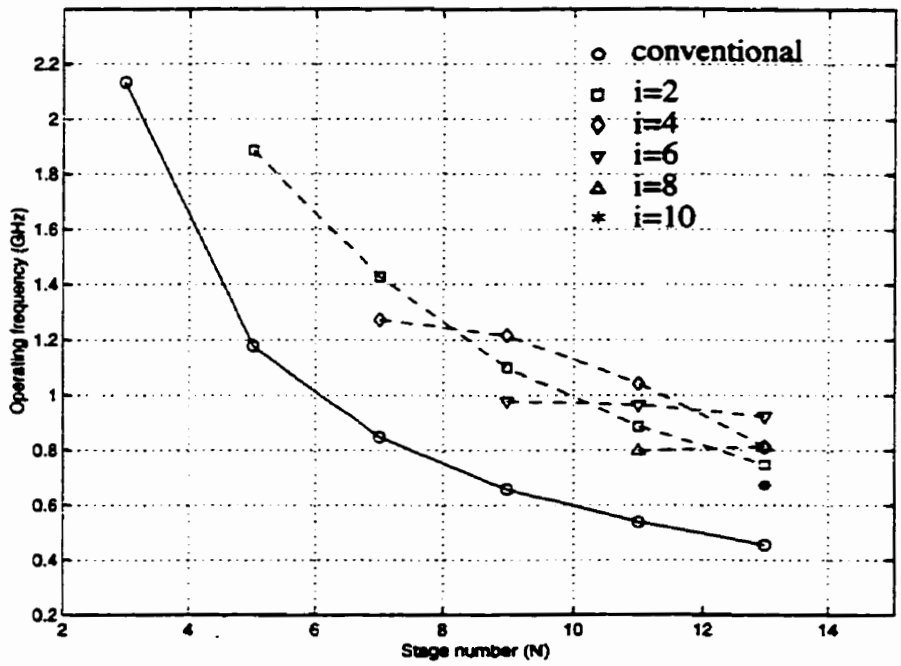


Fig. 3.10. Operating frequency as function of the stage number (N) and the feedback index (i)

The relative frequency increase can be found as,

$$\frac{\Delta\omega}{\omega_{00}} = \frac{k_0 G_m R(C_1/C) + \tan\theta \cdot (C_1/C - 1)}{\tan\theta} \tag{3.7}$$

where ω_{00} and C_1 are the operating frequency and parasitic loading capacitance of each stage for conventional topology (without sub-feedback inverters), respectively. The sub-feedback inverters should be introduced without significant increase of the loading capacitors. We have assumed that R remains the same. Since G_m is related to the unity-gain frequency (ω_T) of the CMOS transistor by $G_m \approx \omega_T C_{gs}$, thus from Eq. (3.5) we have,

$$\Delta\omega = k_0 \omega_T \cdot \left(\frac{C_{gs}}{C}\right) \tag{3.8}$$

Eq. (3.8) shows that the increased oscillation frequency is proportional to the unity-

gain frequency of CMOS transistor in the sub-feedback loops and the ratio of its gate-source capacitor to the total node capacitor. When $G_m = 0$, we have the oscillation frequency for a conventional ring oscillator as

$$\omega_0 = \omega_{01} = \frac{\tan\theta}{RC} \tag{3.9}$$

and minimum required dc gain as

$$g_m R = \sqrt{1 + (\omega_0 RC)^2} = \sec\theta \tag{3.10}$$

Since the longer chain of a ring oscillator corresponds to a smaller θ, thus it requires lower dc gain for loop to maintain oscillating. For a sub-feedback loop based ring oscillator, the dc gain of the inverter in the major loop should be kept greater than minimum value for oscillation to occur. However, excess large value should be avoided to achieve low phase noise.

3.2.1.2 Frequency Tuning

From Eq. (3.5), we observe that the oscillation frequency of an N stage ring oscillator with a fixed feedback index i can be tuned by varying anyone of three parameters: loading capacitance (C), loading resistance (R) and transconductance (G_m). Capacitive tuning has the drawback of lowering the maximum speed of operation because the minimum value of capacitor still loads the circuit. Although resistive tuning can provide a large frequency variation, it causes voltage swing and voltage gain variation. When transistors operating at the triode region are used as a loading resistor, their nonlinearity degrades the common mode noise rejection. If polysilicon resistors are used as loading for a conventional single loop ring oscillator, the time constant at the drain of the driving transistor does not directly depend on the tail current [Fig. 3.38], thus, the tuning range is very small.

The frequency of the ring oscillator with sub-feedback loops is directly proportional to G_m with a linear slope according to Eq. (3.5). When G_m is controlled by an external voltage, $\Delta\omega$ ($= k_0 G_m / C$) is the tuning range. Since G_m is also a function of transistor sizes, the gain (or sensitivity) of the VCO can be adjusted with the choice of appropriate driving transistor sizes in the sub-feedback inverters. Thus the sub-feedback loops topology provides an alternative way for frequency tuning which can also be understood as changing the effective number (N_{eff}) of delay stages within the range of ($i+1$) and N.

3.2.1.3 Speed Power Product

When conventional single-ended inverters are used in Fig. 3.5, there is a time overlap when both the NMOS and PMOS transistors are conducting (M_1 and M_4 or M_2 and M_3 are on at the same time as shown in Fig. 3.11). The conductance overlap causes increased power consumption.

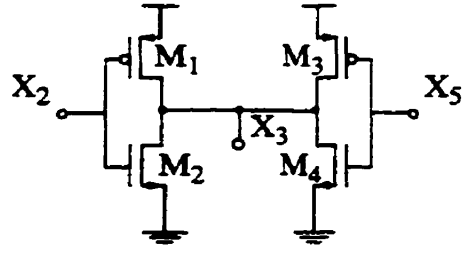


Fig. 3.11. Contention between two inverters

We are more interested in the speed-power product (SP) which is simply the product of the oscillation period and total power consumption. The result is a measurement of power efficiency. Table 3.2 lists the simulated results of the speed power product for i=0, 1, 2, 4 (7 stage ring) when simple inverters are used as gain stages. The circuit has the highest power efficiency for conventional single ring structure (smallest SP) and is least

efficient when i=1. Improved speed comes at the expense of greater power consumption due to the time overlap when both transistors (M_1 and M_4 or M_2 and M_3) are on. In order to improve the power efficiency, a constant current source is proposed to be used in the inverter circuit to avoid excessive power consumption. Detailed implementation will be discussed in the next section.

Table 3.2 Speed-power product for i=0, 1, 2, 4 (7 stages ring oscillator)

i	T (ns)	P (mW)	SP (pJ)
0	1.176	11.22	13.2
1	3.33	16.5	54.9
2	0.7	39.6	27.7
4	0.88	29.7	26.1

3.2.1.4 Time Domain Analysis

The improvement of oscillation frequency can also be understood in the time domain. Fig. 3.12 redraws the signal paths driving node X_3 for the five stage ring oscillator previously shown in Fig. 3.6. The delay from X_5 to X_3 is a weighted sum of the two path delay,

$$T_d = \alpha T_f + \beta T_s \tag{3.11}$$

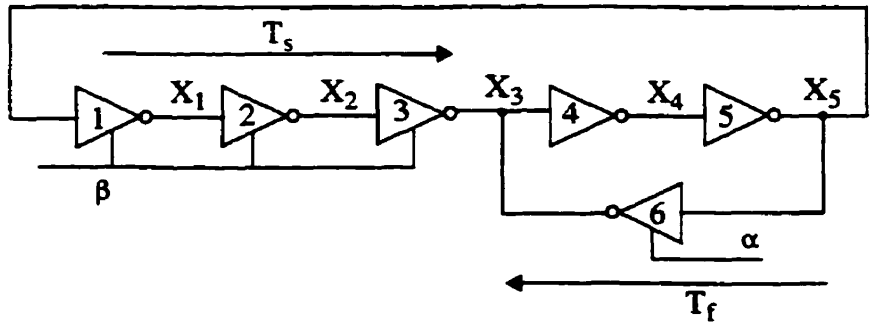


Fig. 3.12. The signal paths driving node X_3

By changing the weighting distribution (α or β, or both at the same time in the form of push-pull) with a single-ended or differential control voltage, a continuously variable delay is produced. However, it should be noted that when the weighting distribution is controlled with an external voltage, the dc gain condition in Eq. (3.4) for inverters in the major loop should be maintained at greater than the minimum value for stable oscillation.

3.2.2 Circuits and Simulations

There are a variety of inverter circuits that can be used as delay cells. Conventional single-ended inverters have a gate-source voltage proportional to the power-supply voltage. When the amplitude of the power supply voltage increases, the charging and discharging currents of the inverters increase in proportion to the square of the power-supply voltage [JoMa97]. Thus, any noise present on the power-supply voltage will cause the oscillator output waveform to have jitter. This poor power-supply rejection is one of the major sources of jitter in integrated oscillators. Further, as analysed in the previous subsection, the use of simple inverters for sub-feedback loop based ring oscillators cause increased power consumption.

Fig. 3.13 shows a proposed single-ended implementation example of the topology. In each delay stage as shown in Fig. 3.14(a), M_3 and M_4 are drive transistors for the common source gain stage. The wide swing cascoding PMOS current sources M_1, M_2 are used as shared active load. The frequency control mechanism is achieved through the use of voltage-controlled resistor (R_V) connected between the source of M_4 and ground. M_4 and R_V together provide a voltage-controlled transconductance G_m to the oscillator. As an alternative to single-ended voltage control, differential control voltage can be used by placing a second voltage controlled resistor (R_{V2}) between the source of M3 and ground as shown in Fig. 3.15. However it should be noted that g_m in the major loop should be large enough, in order to satisfy the minimum required dc gain condition for stable oscillation as shown in

Eq. (3.4).

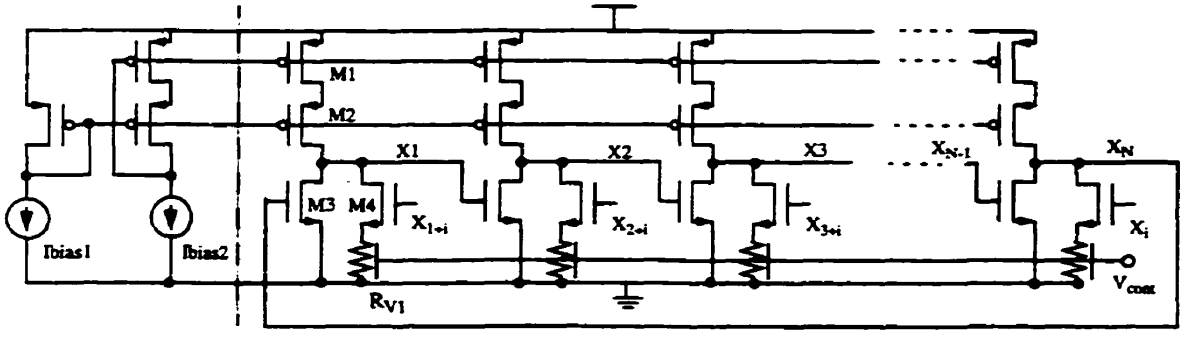


Fig. 3.13. Proposed implementation of the topology

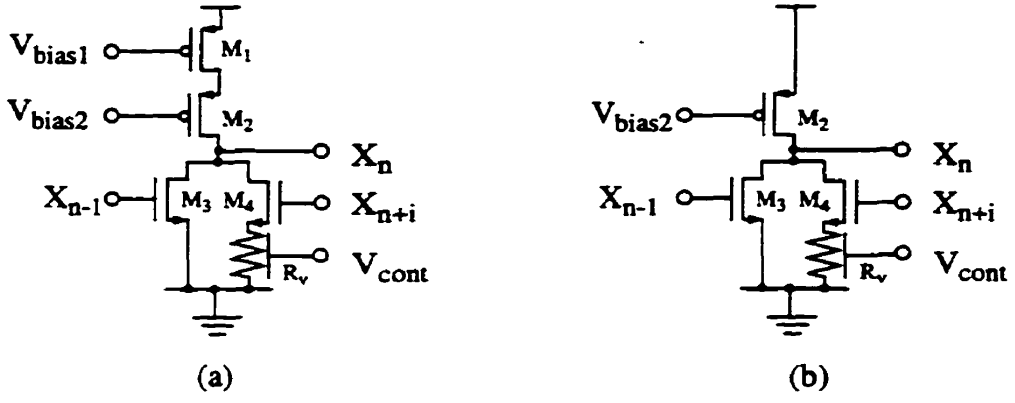


Fig. 3.14. (a) Schematic of a single delay cell and (b) its alternative

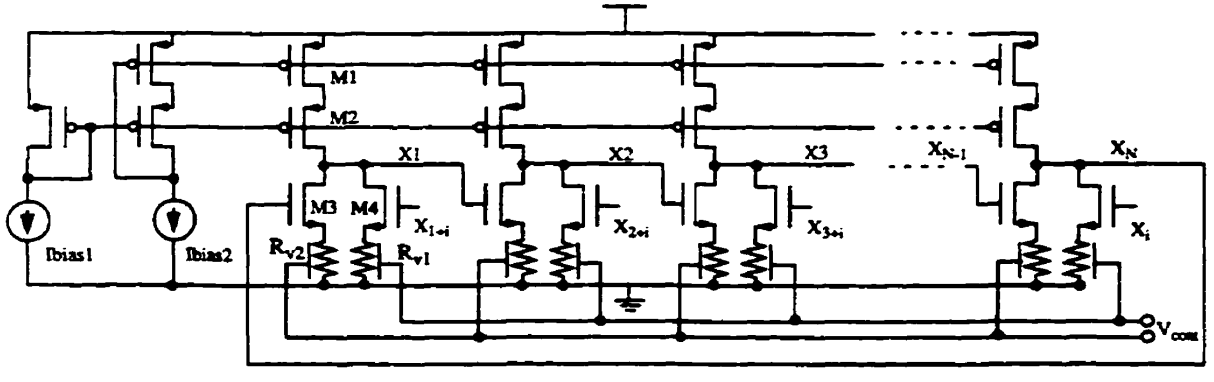


Fig. 3.15. Another version of Fig. 3.13 with the use of differential control voltage

The use of a cascode current source in the load provides high impedance to buffer the output from the power supply V_{DD}. Since the voltage swings in the VCO are not rail-to-rail, the PMOS loads are in saturation for the most part, thereby reducing the noise injection from V_{DD} to the output. The use of a current source in the load also prevents an excessive increase of power consumption when the operating frequency increases. A cascode constant current source can be replaced by a conventional current source as shown in Fig. 3.14(b) to save a voltage bias, though this is at the cost of finite output impedance of the load.

The sizes of transistors M_3 and M_4 need to be ratioed to operate properly. When the width of M_4 increases, its transconductance increases resulting in an oscillating frequency increase. However there exists a maximum value of G_m at which a stable oscillation condition (3.4) can be maintained. The choice of the size of M_4 depends on the current source value and size of M_3. An improvement in speed can be obtained by optimizing device sizes in a circuit simulator like HSPICE.

Taking the five stage ring oscillator (Fig. 3.13) as an example, we simulate the circuit ($i = 2$) using 0.35 μm CMOS technology at a temperature of 75 degrees with a power supply V_{DD} of 3.3V. The device sizes of M_3 and M_4 are 10μm/0.35μm and 5μm/0.35μm, respectively. R_{v1} is realized with a NMOS transistor of size 10μm/0.35μm. Fig. 3.16 shows the simulation result of the voltage to frequency transfer characteristics with power supply V_{DD} as parameter. The VCO's sensitivity to power supply variations ($((\Delta f)/f)/\Delta V_{dd}$) is very low (<1%/V) when the control voltage is around 1.2 V. The voltage control linearity can be improved by the use of linearized resistors. The usage of voltage controlled resistors has the additional advantage that a V-to-I (voltage to current) converter which consists of an opamp and current mirrors is not needed. The current source in the loading can be connected to a temperature compensated biasing circuit to im-

prove the temperature sensitivity.

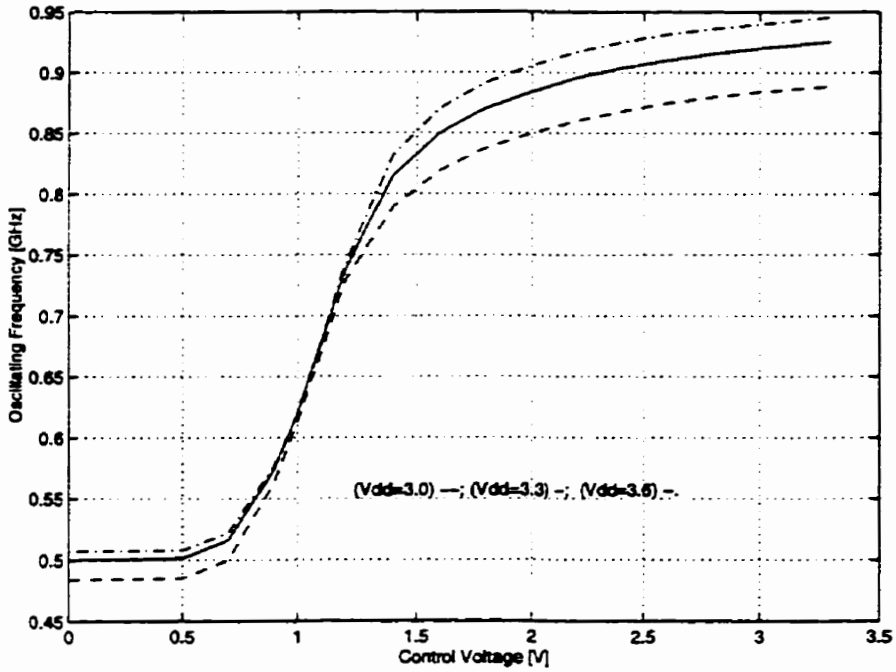


Fig. 3.16. Simulation result of the voltage to frequency transfer characteristics with power supply V_{DD} as parameter

3.3 A Quadrature Output Ring Oscillator Based on Three-stage Sub-feedback Loops

3.3.1 Topology

The topology in Fig. 3.5 can be extended to a differential structure. Fully differential inverters are used to reduce the sensitivity to power supply fluctuation and substrate noise, which are two of the major sources of jitter in high frequency oscillators. Differential architecture also produces 50% duty cycle waveform which is important in many applica-

tions. Since each differential delay stage has two outputs, the total number of outputs are doubled compared to singled-end circuits.

Fig. 3.17 shows the block diagram of the four stage ring oscillator. Compared with conventional ring oscillators, four inverter gates are embedded to construct the sub-feedback loops. With feedback index i=2, the inputs of the feedback circuits are derived from the (n+2)th output node which has a phase delay of 90 degrees. Each sub-feedback loop contains three inverters and is established as a fast path. The main feedback loop with four stages is the slow path. Fig. 3.18 shows the phase relationship for the four stage ring oscillator. When matched delay stages are used, A and C are quadrature pairs as are B and D. Imposing these phase relations to Eq. (3.4) and Eq. (3.5) we have oscillation frequency,

$$\omega_o = 1/(RC) + G_m/C \tag{3.12}$$

and minimum required dc gain,

$$g_m R = \sqrt{2}. \tag{3.13}$$

Since dc gain is not related to G_m, it is much easier to maintain oscillation when G_m is controlled with external applied voltage. A delay stage of the ICO core circuit is shown in Fig. 3.19. The two NMOS source-coupled pairs share the same loads, but have two separated current sources. The balanced differential design helps to minimize jitter due to power supply and substrate noise coupling. The load resistors are shared by the two pairs of differential drivers. I_{b2} and I_{b1} are used as coarse and fine tuning, respectively.

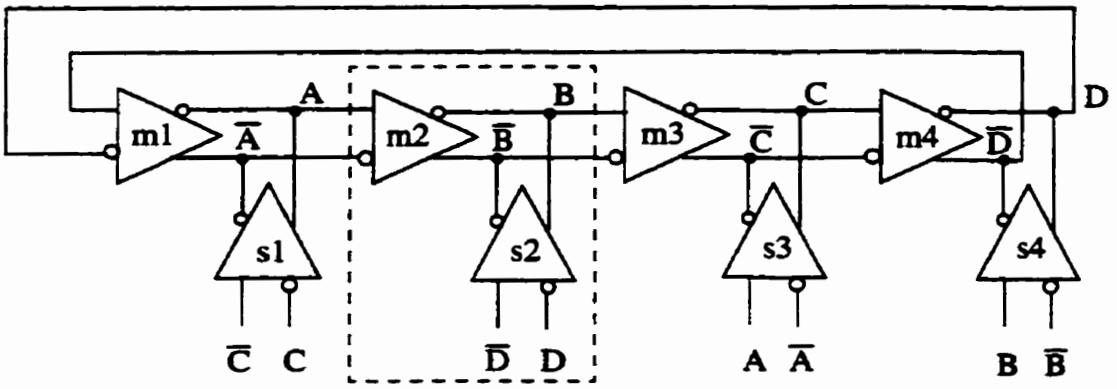


Fig. 3.17. A quadrature output ring oscillator based on three stage sub-feedback loops

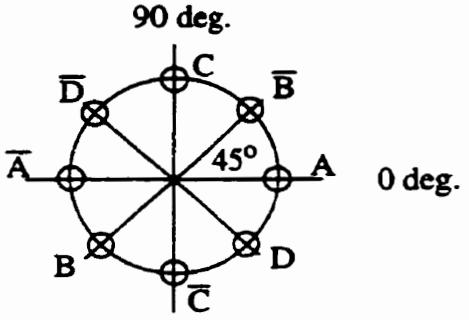


Fig. 3.18. Phase relationship for circuit in Fig. 3.17

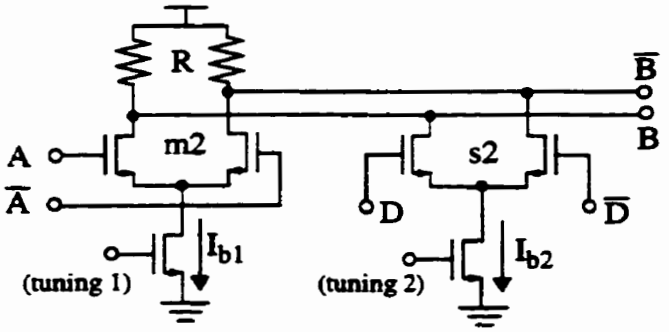


Fig. 3.19. A differential delay stage

The architecture can also be implemented using a non-inverter stage as shown in Fig. 3.20. The phase shift between adjacent stages is 45 degrees as shown in Fig. 3.21.

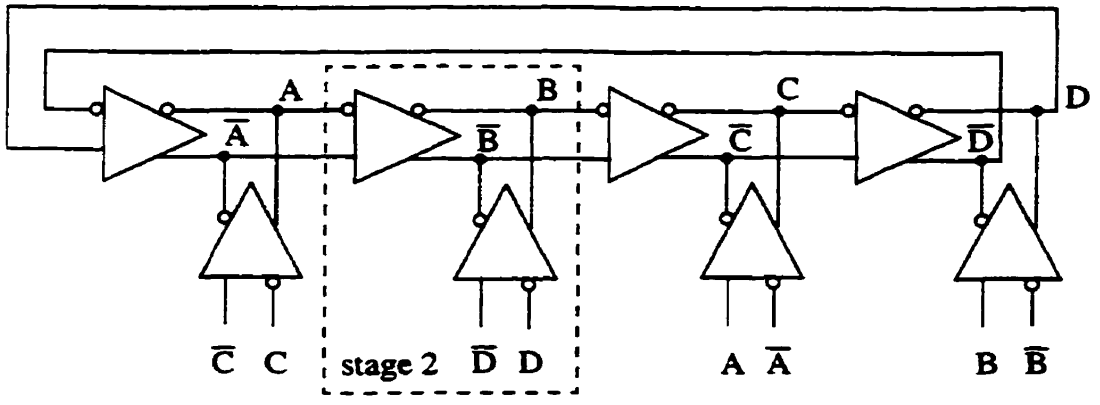


Fig. 3.20. Differential ring oscillator based on non-inverter stage

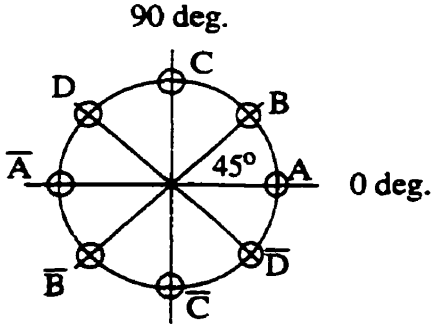


Fig. 3.21. Phase relationship for circuit in Fig. 3.20

By redrawing the circuit in three dimensions, sub-feedback loops can be more easily viewed, as shown in Fig. 3.22 (only the single-end is plotted for simplicity). There are four sub-feedback loops in the topology (m1-m2-s4; m3-m4-s2; m2-m3-s1; m4-m1-s3). It should be noted that stages in altitude and latitude are designed not to oscillate in two stage ring oscillator mode to ensure reliable oscillation and reduction of phase noise.

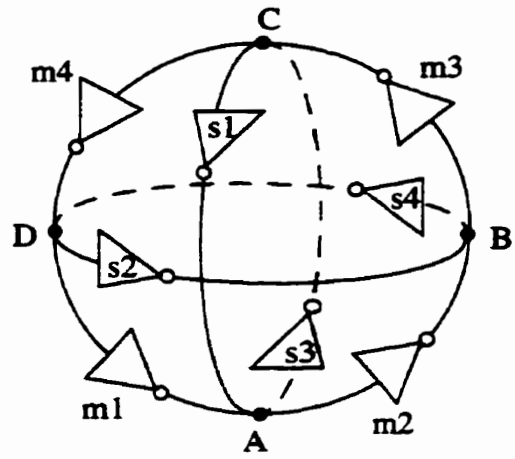


Fig. 3.22. 3-D representation of ring oscillator from Fig. 3.17

Fig. 3.23 shows another proposed differential inverter implementation for the 4 stage sub-feedback loop-based ring oscillator. The VCO cell is a differential inverter with two pairs of source-coupled PMOS inputs ((M_1, M_2) and (M_3, M_4)). The gates of M_1 and M_2 are connected to the output of the previous (n-1) stage (n represents local stage), while the gates of M_3 and M_4 are connected to the output of the (n+2) stage for establishing the sub-feedback loop. The n-well containing the PMOS transistors is biased at a voltage referenced to Vss. This eliminates noise coupling from the power supply to the signal nodes. The use of PMOS devices references the node signals to Vss, eliminating frequency shifts due to nonlinear capacitances. Tail current sources are cascoded for high impedance to V_{DD}. The NMOS transistor pair (M_5, M_6) is used as the load of the differential inverter. The cross coupled structure of M_5 and M_6 increases the gain of the cell. They can be replaced by diode-connected transistors. However, the circuit has a relatively lower operating frequency compared to the counterpart using NMOS as driver transistors as shown in Fig. 3.19 due to the lower transconductance of the PMOS driver.

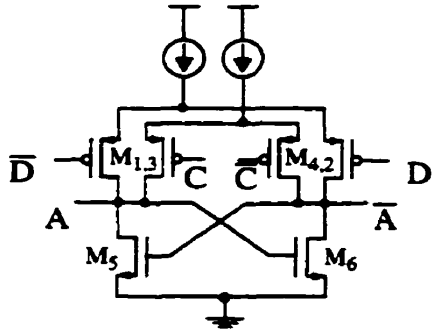


Fig. 3.23. Alternative to the proposed differential implementation

Frequency tuning can be accomplished using single-ended or differential control voltage. Greater control sensitivity is achieved by decreasing the current in slow loop and increasing the current in the fast loop at the same time (push-pull). Fig. 3.24 shows the proposed control differential voltage to a differential control current converter for circuits in Fig. 3.19 and Fig. 3.23. Control sensitivity can be adjusted by choosing the appropriate transistor size in the current mirrors.

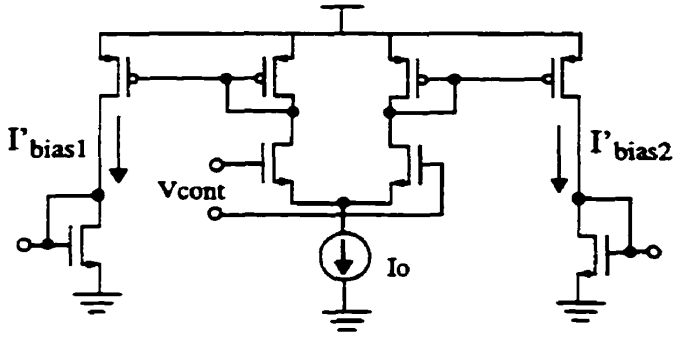


Fig. 3.24. A differential voltage to differential control current converter

3.3.2 Design and Analysis

In the single stage circuit (which combines inverters for the major and sub-feedback loops) as showed in Fig. 3.25, the shared active loads can be replaced with passive loads and implemented using a polysilicon layer to reduce 1/f noise in active loading and achieve linear symmetrical function. The gate-drain connected MOSFET can also be used as a resistive load, as shown in Fig. 3.25, to save chip size but at the cost of degraded linearity. As the tail current is adjusted, the impedance of the load devices and the transconductance of the differential pairs varies accordingly, causing the variation of operation frequency. Frequency tuning is achieved either with I_{b2} controlled with a single-ended signal or both I_{b1}, I_{b2} controlled (push-pull) with a differential signal as shown in Fig. 3.24.

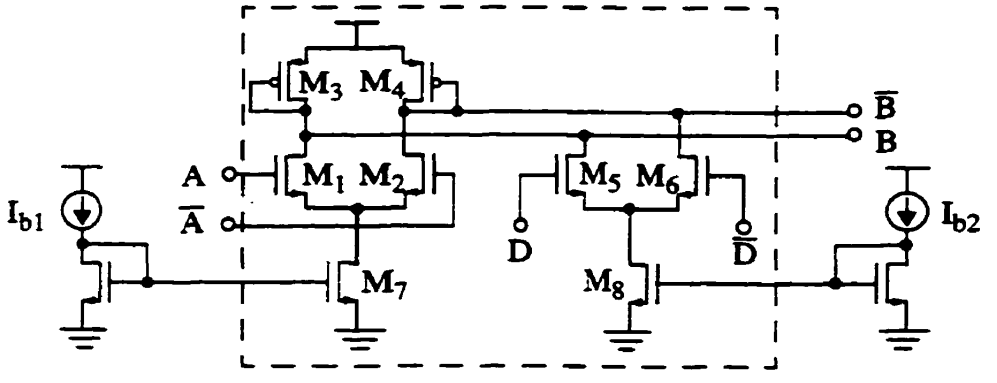


Fig. 3.25. A single stage circuit with biasing current

The initial value of transistors can be determined from small-signal linearized analysis. We have dc gain,

$$g_m R = \frac{\sqrt{2\mu_n C_{ox}(W_1/L)(I_{b1}/2)}}{\sqrt{2\mu_p C_{ox}(W_3/L)(I_{b1}+I_{b2})/2}} = \sqrt{\frac{\mu_n}{\mu_p}\frac{W_1}{W_3}\cdot\frac{1}{(1+I_{b2}/I_{b1})}} \tag{3.14}$$

where I_{b1}, I_{b2} are tail currents. The gain should be larger than $\sqrt{2}$ as shown in Eq. (3.13) for oscillation to occur. The percentage increase of frequency relative to a single loop oscillator is approximated by,

$$\frac{\Delta\omega}{\omega_{01}} = G_m R = \sqrt{\frac{\mu_n}{\mu_p}\frac{W_5}{W_3}} \cdot \frac{1}{(1 + I_{b1}/I_{b2})} \tag{3.15}$$

We have assumed that a differential pair uses its smallest gate length given by the process technology, whereas its gate width is optimized for speed. The width of transistors affects the loading effect on the previous stage, driving strength and phase noise. In Eq. (3.12) C is the total capacitance at the output node referred to ground. Consider the schematic of a switching node shown in Fig. 3.26,

$$C = C_L + C_{db3} + C_{gd1} + C_{db1} + C_{gd5} + C_{db5} \tag{3.16}$$

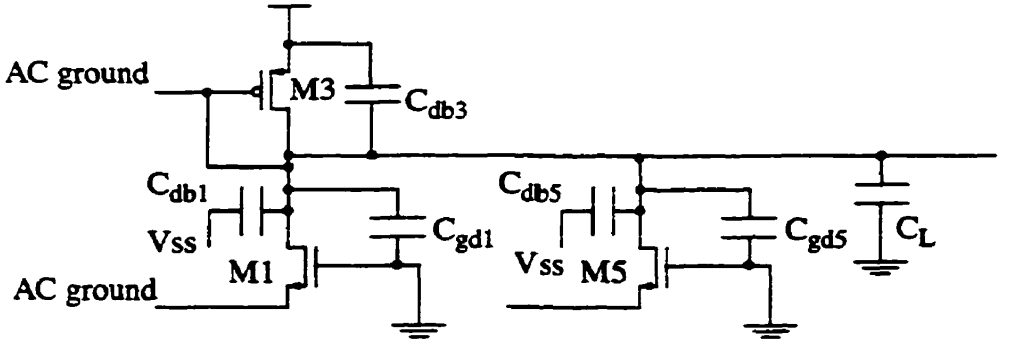


Fig. 3.26. Parasitic capacitance at each output node

For small loading effect it is preferred to use small size drive transistors. However, oscillation conditions for the loop gain and speed improvement require the opposite. In general, the larger the gate width W (while holding L constant), the lower the V_{GS} (at a given bias current). Furthermore, common mode range (CMR) is increased, noise is lowered, matching is better, and gain is increased. The main drawbacks are an increased layout area

and parasitic capacitances. With the initial width value, improvement in speed can be obtained by optimizing different device widths in a circuit simulator like HSPICE.

Two parallel PMOS transistors as shown in Fig. 3.27 can be used to improve the linearity and dynamic range of the loading resistors to the differential pair [MZN90][Mane96]. Fig. 3.27 shows the simulated I-V characteristics for three cases: (a) $I_{d1} - V_{DS}$ curves for a single transistor with V_{GS} as parameter; (b) $I_{d2} - V_{DS}$ curve for a single transistor with gate-drain shorted; (c) $I_d - V_{DS}$ curves for two parallel PMOS transistors with V_{GS} as parameter. The sizes of both PMOS transistors for simulation are 3μm/0.6μm. The degree of convexity in (a) and concavity in (b) of the two drain current curves can be adjusted until they are the same by simply using the same shape factor W/L for both transistors. Then, the nonlinearity of individual transistors will be cancelled in certain range of V_{DS} as shown in Fig. 3.27(c). Improved linearity can thus be achieved.

A ring oscillator structure having equal voltage amplitudes and slopes at each switching node is a solution to the optimization objective for phase noise [Abou96] and balanced output. Buffer circuits such as differential-to-single-ended converters can be used in each pair of switching nodes to convert the differential output into a single-ended signal. It consists of an NMOS differential pair and PMOS load as shown in Fig. 3.28. If we want to operate the PMOS current mirror at the same effective gate-source voltage (V_{eff}), its chosen size should be μ_n/μ_p times wider, since they are connected in series with NMOS transistor and therefore run at the same bias current. The size of M_1 and M_2 transistors are chosen to have a small loading effect to the core VCO circuit but large enough to drive the buffer circuit.

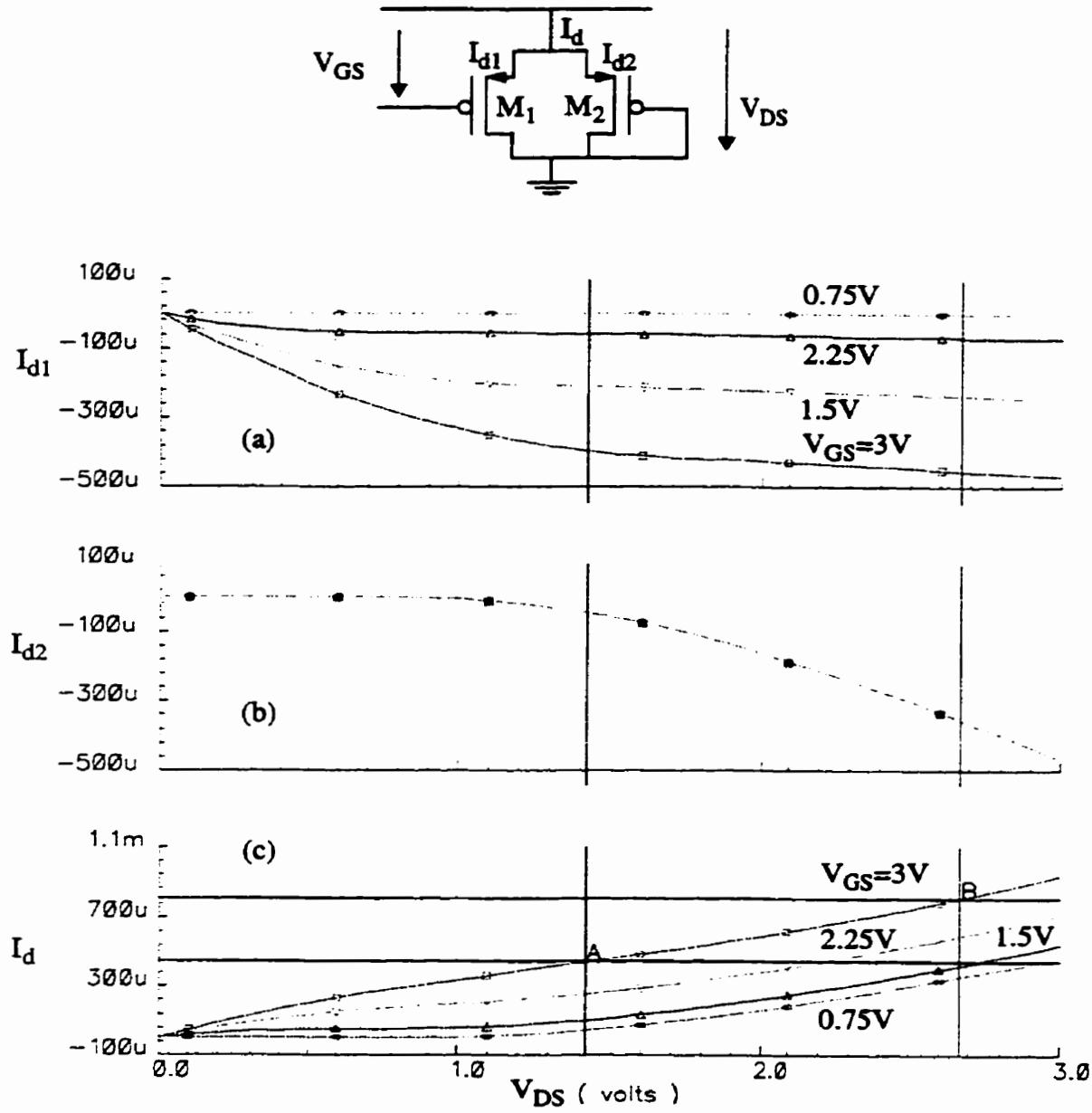


Fig. 3.27. I-V characteristics for transistor as loading resistor. (a) $I_{d1} - V_{DS}$ curve (V_{GS} as parameter) (b) $I_{d2} - V_{DS}$ curve (c) $I_d - V_{DS}$ curve (V_{GS} as parameter)

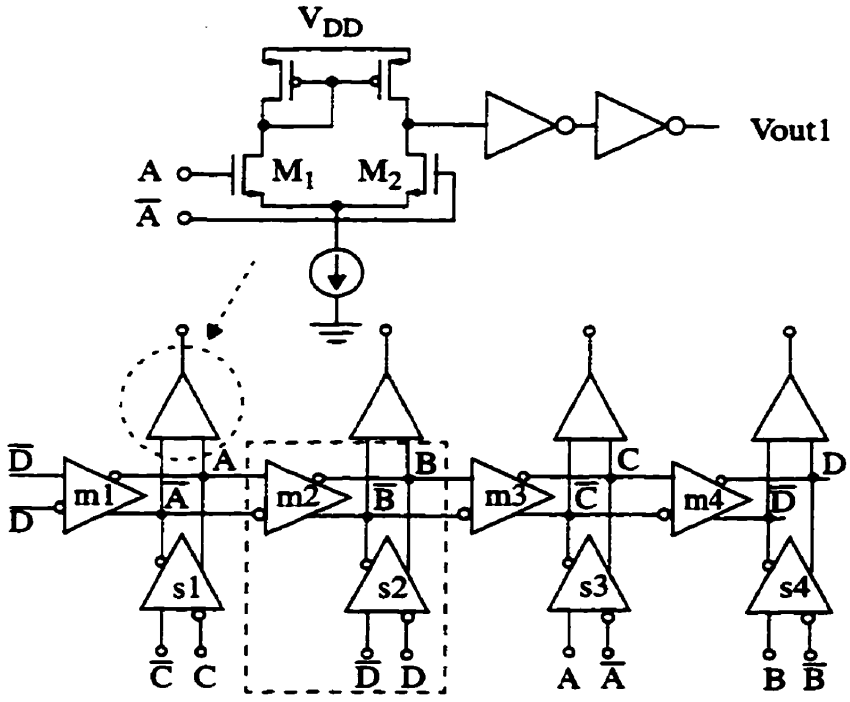


Fig. 3.28. The differential-to-single-ended converter

3.4 Implementation Issues and Measurement Results

3.4.1 Testability Consideration

In order to characterize the performance of the designed VCO, it is important to be able to probe the VCO output at a reasonable power level. A bonding pad can have a capacitance of about 0.5 pF; bonding wire inductance varies in the range of a few nH depending on the bonding diagram and package. Furthermore, the pin capacitance's value can be up to a few pF. A typical equivalent circuit is shown in Fig. 3.29. The series inductors are dominant in GHz range. All these parasitics increase the difficulty in testing the output signal especially at GHz. Although the use of a frequency divider at the VCO output allows the circuit to be tested at lower frequency, it adds some extra noise to the output signal.

Furthermore, it should be noted that it reduces the measured output phase noise power by a factor of $20\log N$ dBc/Hz.

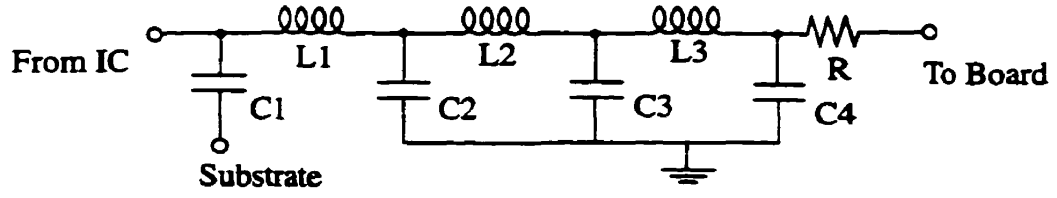


Fig. 3.29. Equivalent circuit of packaging

Conventional digital output buffers are incapable of driving the signal at high frequency. When using a custom designed multistage single-ended inverter to drive the output pad and off-chip circuitry, the number of stages that can be used is limited. The reason for this is that a single-ended inverter amplifies the common mode (or offset) signal. The signal output can die out at either V_{DD} level or ground level when there is an imbalance between the NMOS and PMOS driving strength or there is an offset signal at the input.

A source follower circuit is designed to provide large driving current to an off-chip load as shown in Fig. 3.30. The transistor M_2 between M_1 source and ground is used to supply bias current and adjust output impedance for matching. Large MOSFETs, required to drive off-chip loads, are especially susceptible to latch-up because of the large drain depletion capacitances. The only way to design latch-up free output drivers is to use only one type of MOSFET, in most cases n-channel. Eliminating the n-well and the p-channel transistor eliminates the possibility of latch-up. The size of the M_1 and M_2 are optimized to provide large enough driving current and to avoid overloading the pre-driver.

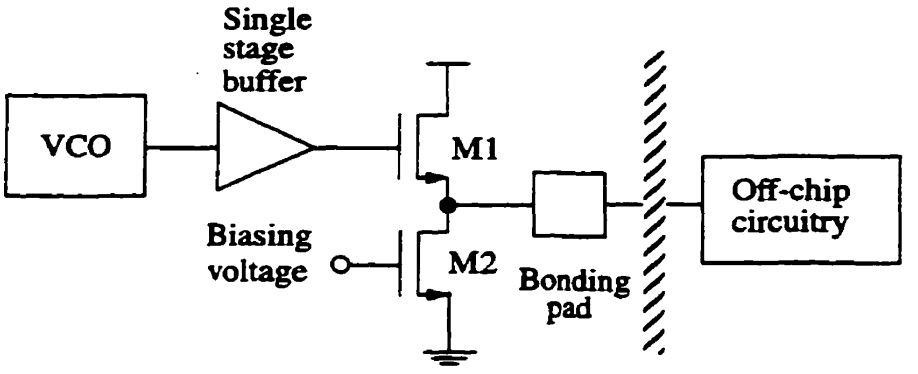


Fig. 3.30. VCO and source follower output buffer

3.4.2 Circuit Layout Considerations

For circuits to operate at frequencies close to those of their pre-layout simulation results, the parasitic capacitance needs to be minimized. The core VCO layouts were made as compact as possible, and all interconnections were made using metal layers. Devices with large width are divided into a parallel connection of MOSFET transistors. The drain and source area are shared between adjacent MOSFETs to reduce the depletion capacitances and layout size. Due to very high-speed operation, standard output pads for the VCOs can not be used and have to be redesigned. The use of a top metal layer as high frequency output reduces the effect of parasitic capacitance to the substrate. To compensate for the edge effects, dummy elements are added to a common-centroid layout [JoMa97]. The dummy element does nothing electrically but is simply used to ensure that the matched transistors see the same adjacent structure.

Every time a digital gate or buffer changes state, a charge impulse is injected into the power supply and into the surrounding substrate. By having the VCO power supplies separate, we prevent this noise from affecting its circuitry. Separate pins are used for the positive power supply and for ground in both the VCO core circuit and buffer circuits which

can inject very large current spikes.

The VCOs are separated by guard rings and wells connected to the power-supply voltages. The p^+ connections to ground help to keep a low-impedance path between the substrate and ground and avoid noise from propagating through the resistive substrate. The use of the n well increases the resistive impedance between the isolated regions due to the pn junction depletion region, which also acts as bypass capacitor to help lower the noise on V_{DD} [Abou96][JoMa97]. Fig. 3.31 illustrates the layout of a 4 stage sub-feedback loop based differential ring oscillator (VCO3).

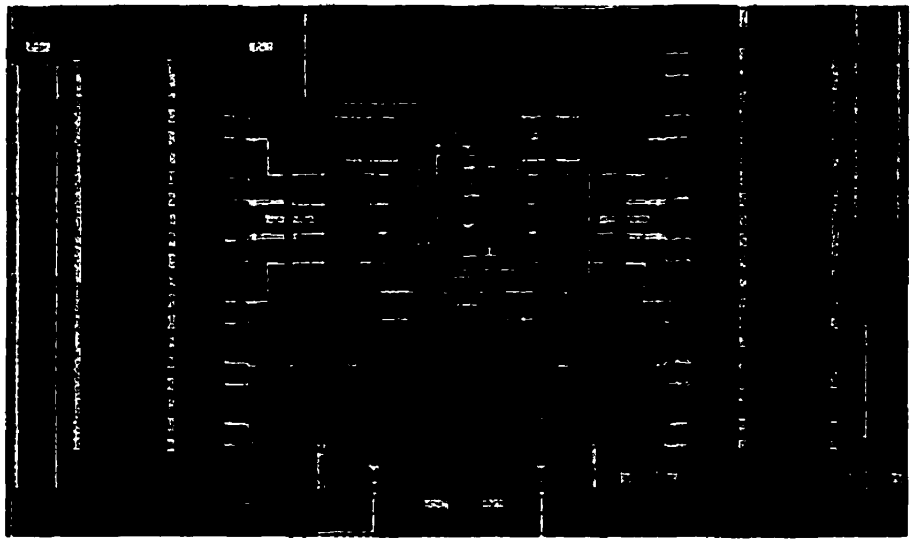


Fig. 3.31. Layout of VCO3 core circuit

3.4.3 Experimental Results

Both single-ended and differential ring oscillators based on the proposed topology were designed and implemented with HP 0.5 μm CMOS technology (HP CMOSIS5) in a single chip. HP CMOSIS5 is a triple metal, single poly CMOS process allowing a minimum drawn feature size of 0.6 μm. The die photo of the chip is shown in Fig. 3.32. The chip has

a size of 2 mm by 1.5 mm, determined by the minimum bonding pad size and the number of pads. It was fabricated through Canadian Microelectronics Corporation (CMC). A 24-lead ceramic flat package (CFP) is chosen for the die bonding packaging. The 24 leaded CFP has a small cavity and is suitable for high-frequency (up to 2 GHz) designs. The chip layout, pin and bonding diagram are shown in Appendix B. The chip package (CFP) was surface mounted to a RF PCB test fixture (provided by CMC) as showed in Fig. 3.33.

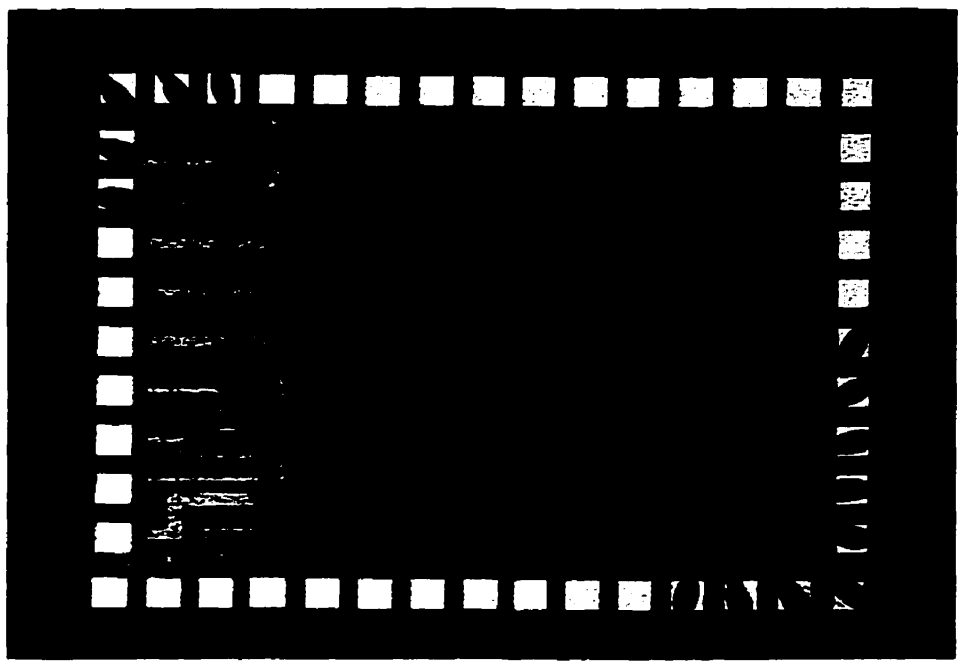


Fig. 3.32. Die photograph of VCOs

The measurement setup used to evaluate the performance of free running (or open loop) VCOs is shown in Fig. 3.34. The power supply is 3.3V. Decoupling capacitors of 0.1 μF are connected across the power supply and control voltage package pins to filter the power supply high frequency noise. Separate power supply pins for the VCOs allow for power dissipation measurement for the VCO core circuitry excluding power dissipated in the output buffers. The following measurements were performed: (a) spectrum analyzer power spectral output; (b) oscilloscope traces for the VCO output waveform; (c) voltage to

frequency transfer characteristics; (d) power dissipation as a function of the oscillation frequency and (e) sensitivity to power supply variation. Several phase noise testing techniques are discussed in Appendix E. Detailed simulation and measurement results can be found in Appendix B. The key measurement results of the three different structures of VCOs are presented and discussed in the following subsections.

Fig. 3.33. DUT on a RF PCB (6 cm x 6 cm)

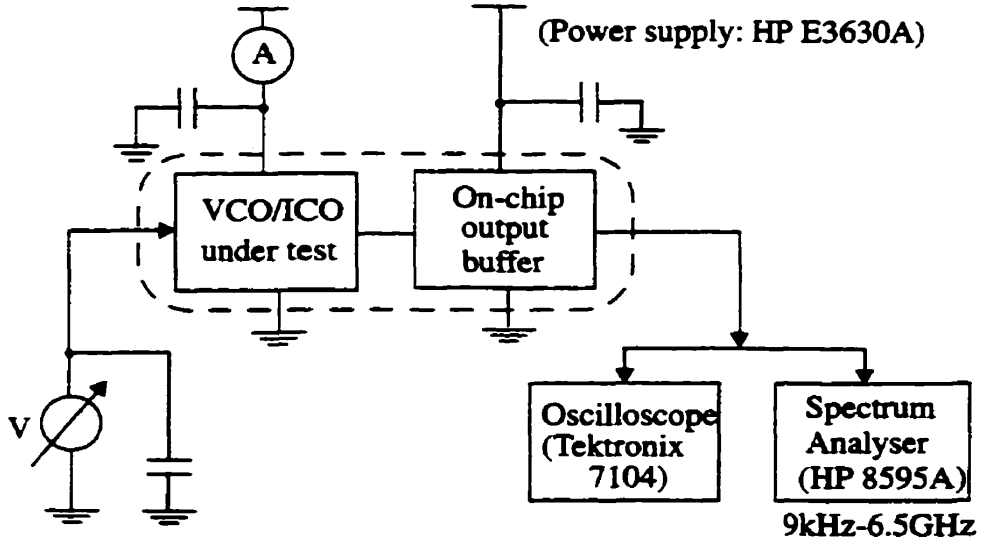


Fig. 3.34. VCOs test setup

3.4.3.1 The Five Stage Single-ended Ring Oscillator Based On Sub-feedback Loops (VCO1)

VCO1 is a single-ended five-stage ring oscillator with sub-feedback loops as illustrated in Fig. 3.35. The voltage controlled resistor was implemented with a single NMOS transistor (M_5). All five stages use the same size to achieve equated waveform amplitude at each output node. A small size pre-buffer is used to reduce its loading effect to the core circuit.

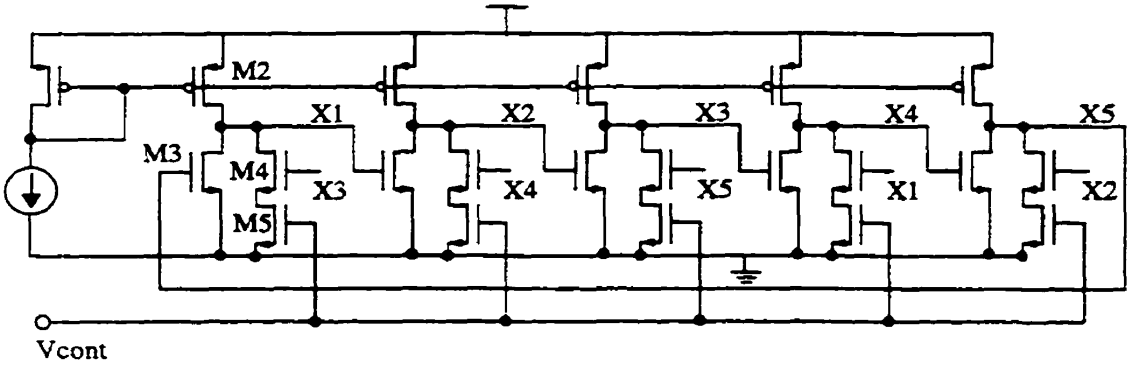


Fig. 3.35. Five stage ring oscillator (VCO1)

Fig. 3.36 shows measurement results of control voltage to oscillation frequency transfer characteristics. VCO1 can operate from 800 MHz to 1.28 GHz corresponding to a control voltage from 0 to 3.3 V. The tuning range is about 500 MHz which is also the increment of frequency for the proposed topology compared to that for the conventional 5 stage ring oscillator ($V_{cont} = 0$). The percentage of achieved improvement is 62.5%. The power consumption is 6 mW at 1.28 GHz against 5.5 mW at the 800 MHz. The proposed circuit is more power efficient since it has lower speed-power product (4.68 pJ against 6.87 pJ). The reported power consumption includes that of the VCO core and pre-buffer amplifier. The sensitivity of oscillation frequency to power supply can be improved with the use of the delay cell proposed in Fig. 3.14(a) in future implementation, since the cascoded current source in the load provides larger impedance to V_{DD} than a single transistor

current source does. Fig. 3.37 illustrates the power spectrum from a spectrum analyzer for the VCO1 output at 1.25 GHz. The measured phase noise is -97.5 dBc/Hz at 1 MHz offset frequency with power consumption of 6 mW.

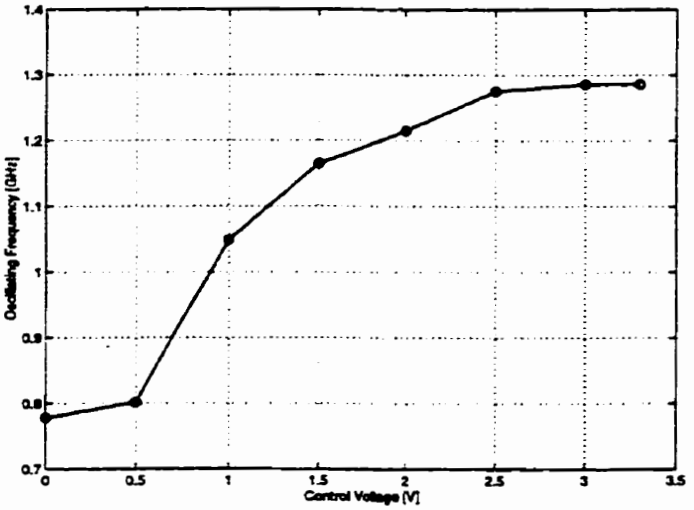


Fig. 3.36. Measured transfer characteristic of VCO1

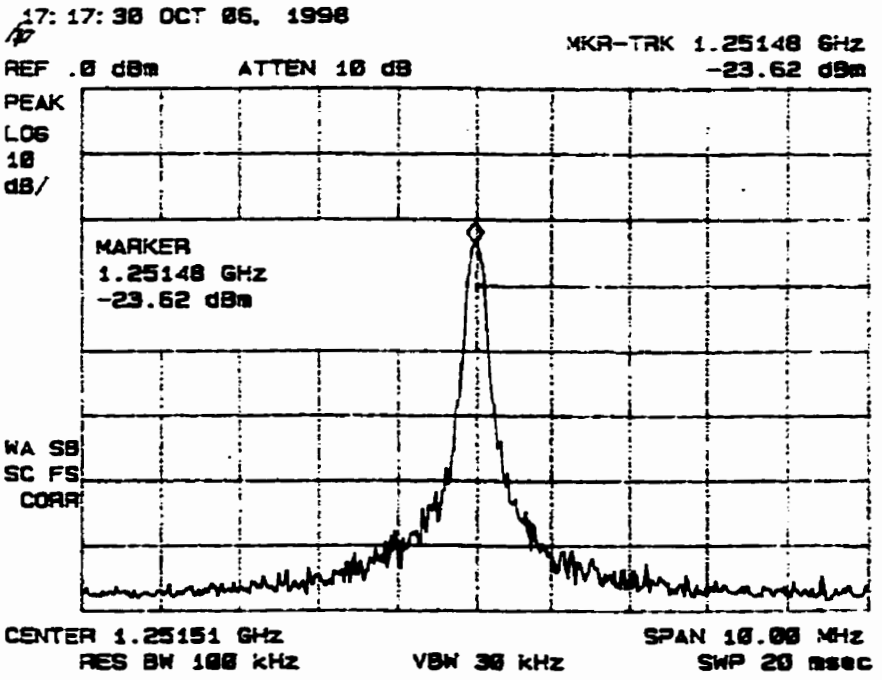


Fig. 3.37. Measured output spectrum of VCO1 at 1.25 GHz

3.4.3.2 The Conventional Four Stage Ring Oscillator (VCO2)

VCO2 is a conventional four-stage fully differential ring oscillator as shown in Fig. 3.38. It is implemented for comparison to VCO3. The differential-to-single ended converter transfers the differential output into a single-ended signal which then drives an output buffer.

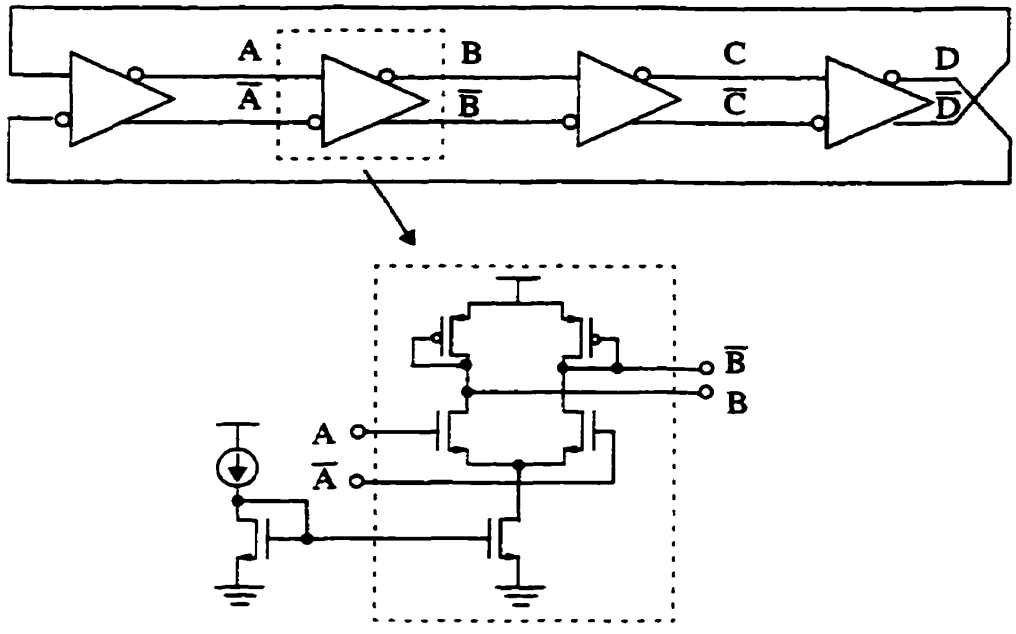


Fig. 3.38. Four stage conventional differential ring oscillator

The measurement results of control current to oscillation frequency transfer characteristics are shown in Fig. 3.39. VCO2 operates from 670 MHz to 980 MHz corresponding to a controlled tail current from 100 μA to 400 μA with tuning range of 300 MHz. Fig. 3.40 shows the spectrum analyzer power spectrum for the free running VCO2 output at 937 MHz. The phase noise is -97.5 dBc/Hz at 1 MHz offset frequency. Power consumption is 5 mW at 980 MHz.

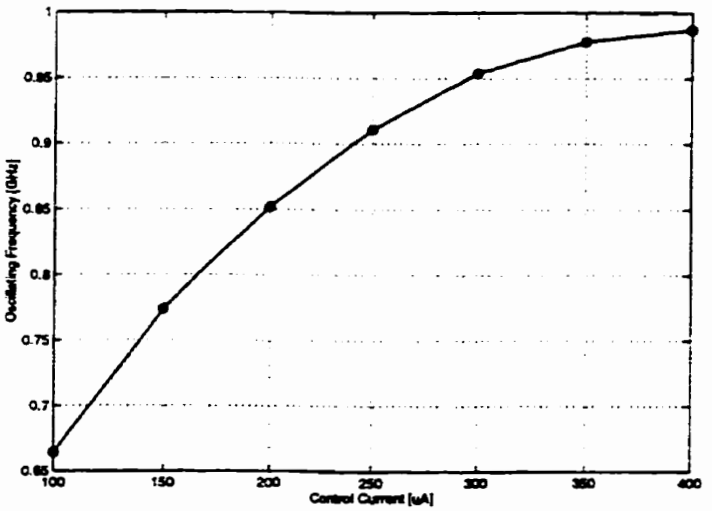


Fig. 3.39. Measured result of transfer characteristic of VCO2

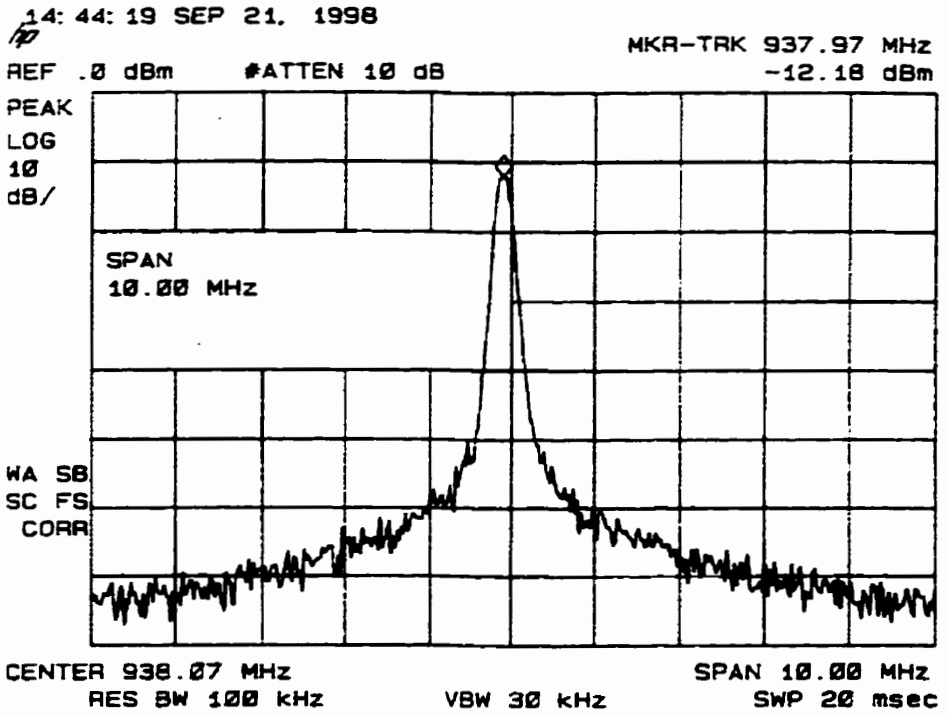


Fig. 3.40. Measured output spectrum of VCO2 at 937 MHz

3.4.3.3 The Four Stage Ring Oscillator Based On Sub-feedback Loops (VCO3)

VCO3 is based on the proposed circuits in Fig. 3.17 and Fig. 3.25. Gate-drain connected PMOS transistors are used as a resistive load to the differential delay cell. The measurement results of control current to frequency transfer characteristic are shown in Fig. 3.41. The dash curve represents the measurement results when $I_{b2} = 0$ (conventional four stage ring). The operating frequency range is from 400 MHz to 620 MHz. The solid curve corresponds to measurement results with I_{b1} constant biased ($I_{b1} = 100\mu A$) and I_{b2} used as controlling current. VCO3 can operate from 400 MHz to 2 GHz corresponding to I_{b2} variation from 0 to 300 μA. The tuning range is over 1 GHz with good linearity. The measured phase noise at 1.25 GHz is -103 dBc/Hz at 5 MHz offset frequency as shown in Fig. 3.42. Power consumption is 3 mW and 5.3 mW at 1.25 GHz and 2 GHz, respectively.

VCO3 can be controlled with a differential signal as presented in Section 3.31. Fig. 3.43 illustrates the measurement results of frequency versus differential control current. The total biasing current ($I_b = I_{b1} + I_{b2}$) is kept constant at 500 μA. Oscillation frequency has a negative and positive linear slope against I_{b1} and I_{b2}, respectively. We can consider I_{b1}/I_b and I_{b2}/I_b as a weighting factor for slow loop (β') and fast loop (α'), respectively (see Fig. 3.12). Fig. 3.43 demonstrates that overall oscillation frequency is proportional to the weighted sum of the slow loop oscillating frequency and fast loop oscillating frequency.

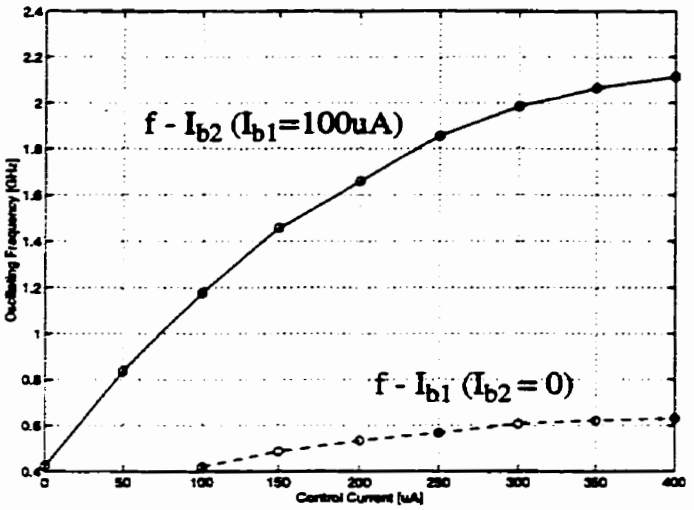


Fig. 3.41. Measured transfer characteristic of VCO3

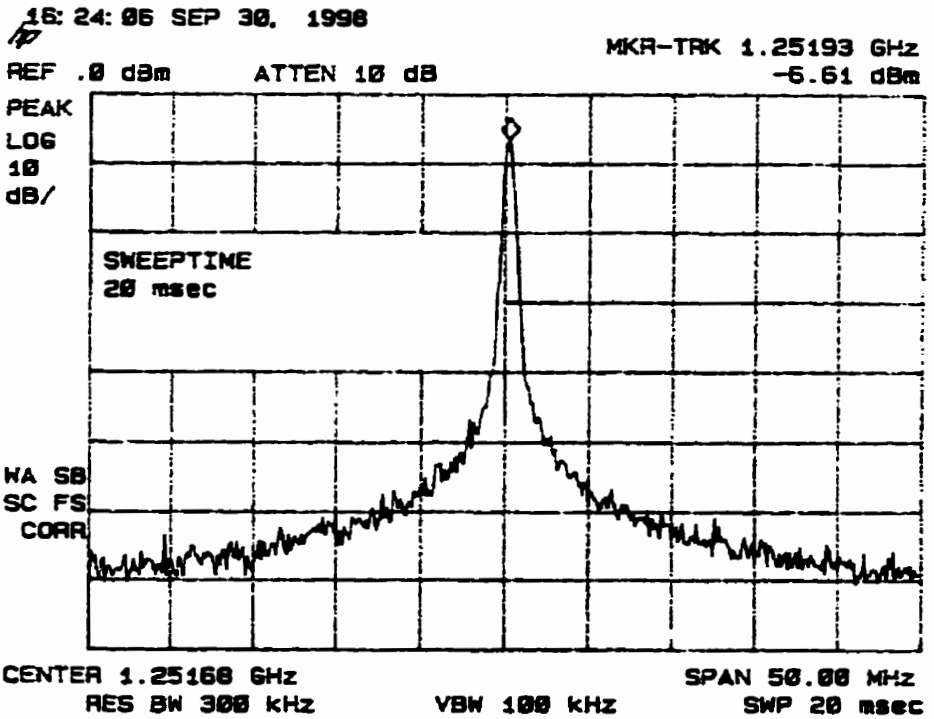


Fig. 3.42. Measured output spectrum of VCO3 at 1.25 GHz

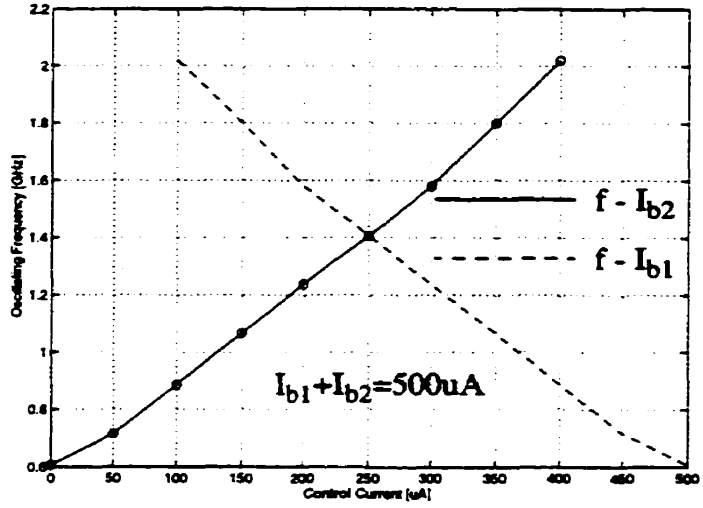


Fig. 3.43. Oscillation frequency versus the differential controlled current

3.5 Summary

This chapter places the priority on speed with the CMOS ring oscillator design, especially for multiphase output. The phase noise analysis will be presented in next chapter. A general oscillator circuit topology capable of achieving high speed operation and multiple phase output has been proposed. The topology used controlled sub-feedback inverters to construct fast loop for long chain ring oscillators to achieve higher speed. The analysis based on a linearized model leads to the establishment of a relationship between speed increment/decrement and feedback index i, which is the number of delay stages down the loop from where the feedback signals are derived, e.g., for a 7 and 9 stage sub-feedback loop based ring oscillators, the highest speed can be achieved with i=2, and 4, respectively.

The frequency of the ring oscillator is directly proportional to the transconductance (G_m) of sub-feedback inverters with a linear slope. G_m can be controlled with an external voltage. Thus, the sub-feedback loops based topology also provide an alternative way to

conventional capacitive and resistive tuning, which can be also understood as changing the effective number (N_{eff}) of delay stages within the range of ($i+1$) and N. Both single-ended and differential inverters stage and control voltage can be used for the topology. In order to improve power efficiency, a constant current source is suggested for use in the inverter circuit to avoid excessive power consumption.

Detailed implementation of the topology for both single-ended and differential circuits has been proposed and analyzed. For a sub-feedback loop based ring oscillator, dc gain of inverters in the major loop should be kept greater than minimum value for oscillation to occur. However, large value should be avoided to achieve low phase noise. The design was fabricated in 0.5 μm CMOS technology. VCO1 is a single-ended five stage ring oscillator with sub-feedback loops. It demonstrates an increase of frequency of 62% with power consumption of only 6 mW. The VCO3 is a four stage quadrature output ring oscillator with three stage sub-feedback loops. Compared with the VCO2, which is a conventional four stage differential ring oscillator of the same size, doubling of speed has been achieved. The linearity of transfer characteristics has also been improved. The proposed topology and circuits are suitable for applications such as high speed multiphase sampling, clock generation and data recovery systems. Measurement results are summarized in Table 3.3.

Table 3.3 Summary of measurement results

	VCO1	VCO2	VCO3
Tuning range	0.8-1.28 GHz	670-980 MHz	0.4 -2.1 GHz
Phase noise	-97.5 dBc/Hz @ 1 MHz (1.25 GHz)	-97.5 dBc/Hz @ 1MHz (937 MHz)	-103 dBc/Hz @ 5MHz (1.25 GHz)
Power consumption (3.3 V supply)	5.5 mW (0.8GHz), 6 mW (1.28GHz)	5 mW (980 MHz)	3 mW (1.25 GHz) 5.3 mW (2 GHz)

CHAPTER 4

Analysis of Phase Noise in Ring Oscillators

4.1 Introduction

Phase noise is a major figure of merit for oscillators used in communication systems. Thus, analysis and prediction of the phase noise is an important issue for oscillator design. There are numerous publications available on this topic [Lees66][AbMe83] [Robi91] [McNe94] [WKG94][Raz961] [HaLe98] [DMR98], and the problem has been approached in different ways. [Lee66] [Robi91] [Raz961] use linear time-invariant (LTI) analysis to model the oscillator and characterize the phase noise in the frequency domain. [AbMe83] [McN94] [WKG94] predict the timing jitter of the relaxation and ring oscillator by using analytical techniques on a simplified model. [HaLe98] analysed the phase noise with a time variant model by decomposing perturbations into two orthogonal components, generating purely phase and amplitude deviations, respectively. However this orthogonal decomposition may not be valid [DMR98]. Instead [DMR98] proposed a numerical

method in the time and frequency domains for predicting phase noise. However the method does not provide an intuitive guideline for oscillator design.

The major objective of this chapter is to analyze the phase noise of the ring oscillators proposed in the previous chapter. First, the fundamental concepts of phase noise and timing jitter, and their impairment in communication systems are overviewed in Section 4.2. The noise sources in the CMOS oscillator are also discussed. In Section 4.3, phase noise in a single-ended ring oscillator is analyzed based on the time domain noise model. Analysis is simplified to make the results easier to interpret. The derived analytical expressions provide guidelines and enable decision making at early stages of the design. In Section 4.4, the linearized model of the ring oscillator is utilized to obtain an estimate of noise performance. The noise sources are classified into three groups according to different mechanisms to output phase noise. The dependence of phase noise on feedback index i and the consequent limitations on available phase noise are investigated. The analysis leads to intuitive guidelines for designing low noise sub-feedback loop ring oscillators.

4.2 Phase Noise Concept

The oscillator's frequency stability is defined by its long-term and short-term stability [Rut78][HP88]. Long-term frequency stability refers to slow changes in the average frequency with time (e.g., due to the temperature variation, aging in the oscillator components). Usually called a frequency drift, it can be eliminated if the oscillator is locked in a PLL configuration with a PLL bandwidth larger than the possible frequency drift rate. Short term stability refers to frequency variations over short time periods (a few seconds or less), which are observed as random and/or periodic fluctuations about a mean.

There are two types of short-term frequency variation. The first type is the determinis-

tic (non-random) discrete signal, commonly called spurious. This type of signal is related to known phenomena in the signal sources, such as power line frequency, vibration frequency, or mixing products. The second type is random (continuous) frequency variation, commonly called phase noise. Both non-random (discrete) and random signals cause timing jitter.

Phase noise in the oscillator are caused by both internal and external noise sources. The internal noise sources include thermal noise, shot noise and flicker noise, in passive and active components of a frequency source. Supply and substrate noise belong to external noise. Even though the gain stage is designed as a differential circuit, it nonetheless suffers from some sensitivity to supply and substrate noise.

4.2.1 Phase Noise Characterization

In the time domain a sinusoidal signal with frequency ω_0 can be written as:

$$V(t) = [A + a(t)]\sin[\omega_0 t + \phi(t)] \tag{4.1}$$

where $a(t)$ and $\phi(t)$ represent the "amplitude" and "phase" noise of the oscillator.

Since amplitude noise can be eliminated using a limiter, we will only discuss the phase noise here. If $\phi(t)$ is constant, this signal is a pure sine wave and its spectrum is a single line as shown in Fig. 4.1(a). On the other hand, if $\phi(t)$ is a random process, the spectrum of V(t) will have some power spread over a narrow bandwidth around the centre frequency f_0 as shown in Fig. 4.1(b). The phase noise on a signal is usually quantified in terms of single-sided spectral noise density (L) in units of decibel carrier per Hertz (dBc/Hz) at a certain offset frequency ($\Delta\omega$),

$$L(\Delta\omega) = 10 \cdot \log\left(\frac{P_{noise}(\Delta\omega)}{P_c}\right) \tag{4.2}$$

where P_c is the carrier level (dBm), P_{noise} is the noise power in a 1Hz bandwidth at offset frequency $\Delta\omega$.

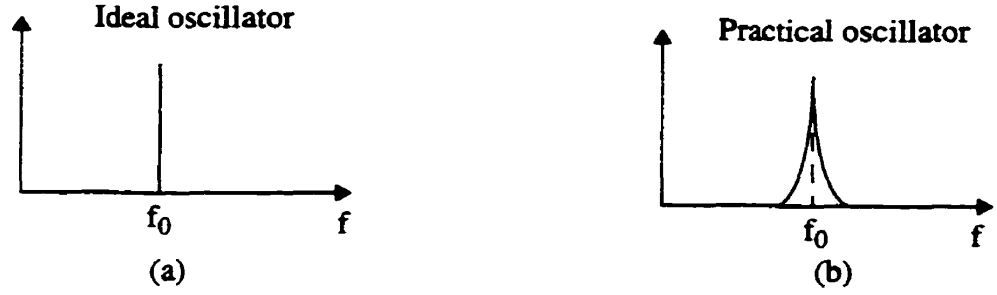


Fig. 4.1. Oscillator power spectrum for (a) ideal sinusoidal oscillator (b) practical oscillator

In data communications, oscillators for clock generation and clock recovery generate a square-wave like waveform. The deviation of the oscillator period itself is of more concern rather than the power spectrum distribution. Thus, the concept of "timing jitter" is used as the noise performance measure. This can be defined in terms of the standard deviation of the oscillator period, or called cycle-to-cycle jitter,

$$\sigma = \lim_{N \to \infty} \sqrt{\frac{1}{N} \cdot \sum_{n=1}^{N} (T_{n+1} - T_n)^2} \tag{4.3}$$

Fig. 4.2 shows the effect of noise in the time domain on the output waveform of a square wave oscillator with respect to an ideal oscillator. Timing jitter can be determined from phase noise by relating the spectral density of the normalized frequency fluctuations to the instantaneous error in the period of oscillation. The following formula can be used to transfer phase noise to the timing jitter for white noise sources [WeKi94][HeRa98],

$$\sigma^2 = \frac{2\pi}{\omega_0^3} S_\phi(\omega)(\omega - \omega_0)^2 \tag{4.4}$$

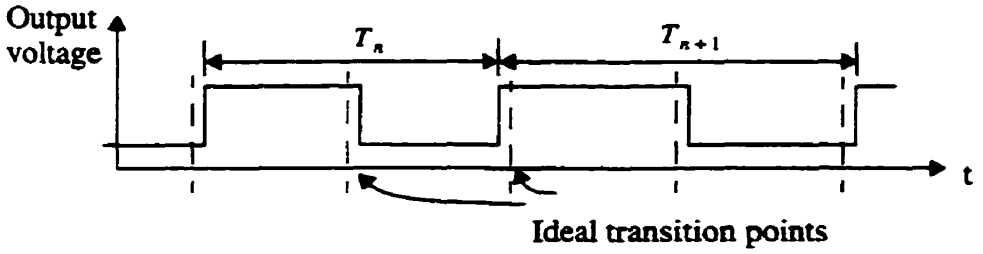


Fig. 4.2. Output waveform of a square wave oscillator showing the effect of noise

4.2.2 Phase Noise Impairments in Communication Systems

In the clock recovery/data acquisition system, the clock timing jitter added to the expected data jitter reduces the effective decoding window, which imposes constrains on the maximum operating frequency of the system and causes degradation in the expected bit error rate (BER) performance.

In a wireless communication system, phase noise in the transmitter can cause contamination of adjacent frequency channels as shown in Fig. 4.3 [Craw94]. Due to the very narrow channel spacings used in cellular telecommunication networks, extremely low phase noise levels are required. For the European Global System for Mobile communications (GSM) system, a single sided spectral noise density of -100 dBc/Hz is specified at 10 kHz offset from the carrier.

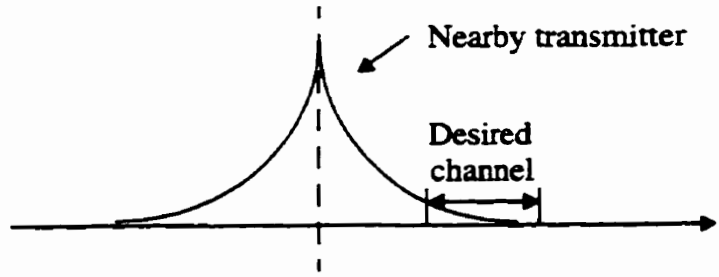


Fig. 4.3. Effect of phase noise on transmit paths

In the wireless receiver path, if the local oscillator exhibits finite phase noise, the presence of strong adjacent signals mixing with the local oscillator phase noise sidebands results in a corresponding reduction in the receiver's sensitivity [Fig. 4.4].

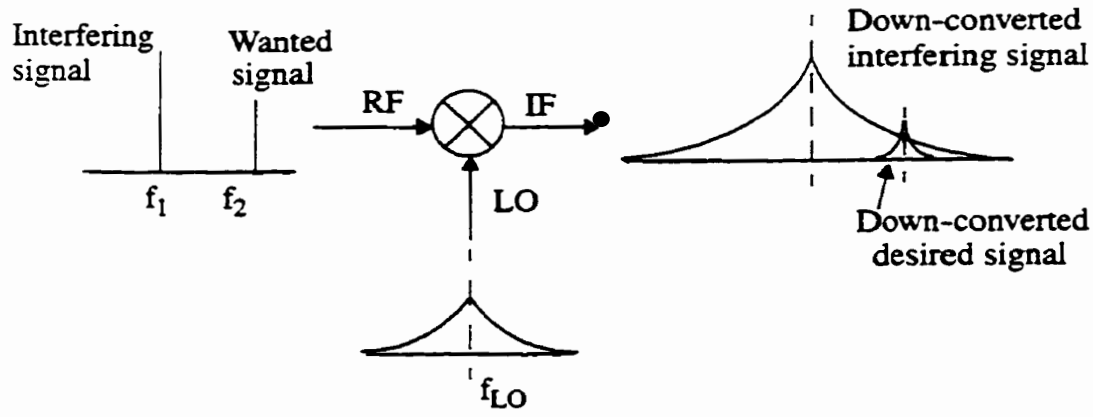


Fig. 4.4. Reciprocal mixing due to high phase noise sidebands in a receiver

4.2.3 Noise Sources in MOSFET Devices

The dominant noise sources for active MOSFET transistors are flicker and thermal noise. The shot noise is generated by the gate leakage current and is usually very small.

4.2.3.1 Thermal Noise

Thermal noise is due to the random thermal motion of the electrons associated with resistors. The thermal noise current in MOSFET transistor is generated by effective channel resistance and by parasitic drain, source, gate and substrate resistances.

The MOSFET thermal noise model due to the channel resistance that is used in most of the literature and in circuit simulators such as SPICE is

$$I_d^2(f) = 4kT\left(\frac{2}{3}\right)g_m \tag{4.5}$$

where k is Boltzman's constant, T is temperature in degrees (Kelvin), g_m is the transconductance at the operating point [Tsiv87].

This noise model does not accurately predict the thermal noise of MOSFET. One of the problems with this model is that it is invalid in the triode region. In analog circuit design, MOSFETs are often operating in the triode region. A model that is valid in the triode region of operation but not widely used in circuit simulators is [Fox93]

$$I_d^2(f) = 4kT\gamma g_{do} \tag{4.6}$$

where g_{do} is the channel conductance with zero drain-to-source voltage, with $2/3 < \gamma < 1$ in triode, and $\gamma = 2/3$ in saturation.

This model works reasonably well for long channel devices. However, it is not adequate for short channel devices, especially in saturation. For short-channel devices, the noise is higher [Abi83]. Hot-electron effects further raise the value. In fact, γ is much greater than 2/3 for short-channel devices operating in saturation. In a submicron process, γ may be as high as two to three, depending on bias conditions [WHS92].

4.2.3.2 Flicker Noise

Flicker noise is caused mainly by traps associated with contamination and crystal imperfections. These traps capture and release carriers in a random fashion and the time constants associated with the process give rise to a noise signal with energy concentrated at low frequencies. Flicker noise in the MOSFET transistor is found experimentally to be represented by a drain-source current generator [GrMe93]

$$I_d^2(f) = K_1\left(\frac{I_D^\alpha}{f}\right) \tag{4.7}$$

where I_d is the drain bias current, K_1 is a constant for a given device, and α is a constant between 0.5 and 2.

The flicker noise can also be modeled as a voltage source referred to gate in series with the gate of value

$$\overline{V_g^2}(f) = \frac{K}{WLC_{ox}f} \tag{4.8}$$

where the constant K is dependent on device characteristics and can vary widely for different devices in the same process.

In most cases, the magnitude of the input-referred flicker noise component is approximately independent of bias current, and voltage and is inversely proportional to the active gate area of the transistor. The latter occurs because as the transistor is made larger, a larger number of surface states are present under the gate, so that an averaging effect occurs that reduces the overall noise. It is also observed that the input-referred flicker noise is an inverse function of the gate-oxide capacitance per unit area [DaMo74]. In typical submicron CMOS devices the 1/f noise corner may be as high as 1MHz. Typically p-channel transistors have less noise than their n-channel counterparts since their majority carriers (holes) are less likely to be trapped. In order to suppress the flicker noise, PLL bandwidth

needs to be chosen wider than the corner frequency.

4.3 Analysis of Phase Noise in Single-Ended Ring Oscillators

Ring oscillators based on a simple CMOS inverter (as showed in Fig. 4.5) use fewer noisy transistors than any other ring oscillator circuitry and can achieve large (rail-to-rail) output voltage swings which are two important factors for low noise design. Furthermore, they consume very low power, have a wide tuning range and are easy to design. Considering the circuit's threshold switching characteristic, time domain analysis is used to characterize the phase noise. The time domain method for a relaxation oscillator [AbMe83] is extended to ring oscillator topology for analysing the timing jitter due to internal noise sources. The derived explicit analytic expressions provide a minimum time jitter that can be achieved by a ring oscillator. Jitter due to power supply and substrate noise will also be analysed. The derived formulae provide a straightforward insight for low phase design.

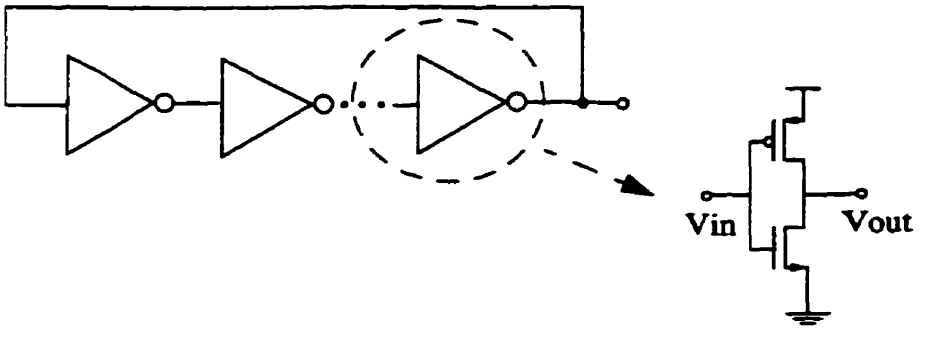


Fig. 4.5. CMOS ring oscillator with inverters as delay cells

4.3.1 Timing Jitter due to Internal Noise Sources

The output waveforms of a three stage CMOS ring oscillator are shown in Fig. 4.6. Each inverter stage in the ring contributes a time delay to the total period of oscillation. The delays contributed by the ith stage τ_{ri} and τ_{fi} are measured from the time the output begins switching to the time it reaches the threshold voltage (V_{sp}) of the input to the next stages, respectively. Hence the period of oscillation T_0 for an N stage ring oscillator is given as

$$T_0 = \sum_{i=1}^{N} (\tau_{ri} + \tau_{fi}) \tag{4.9}$$

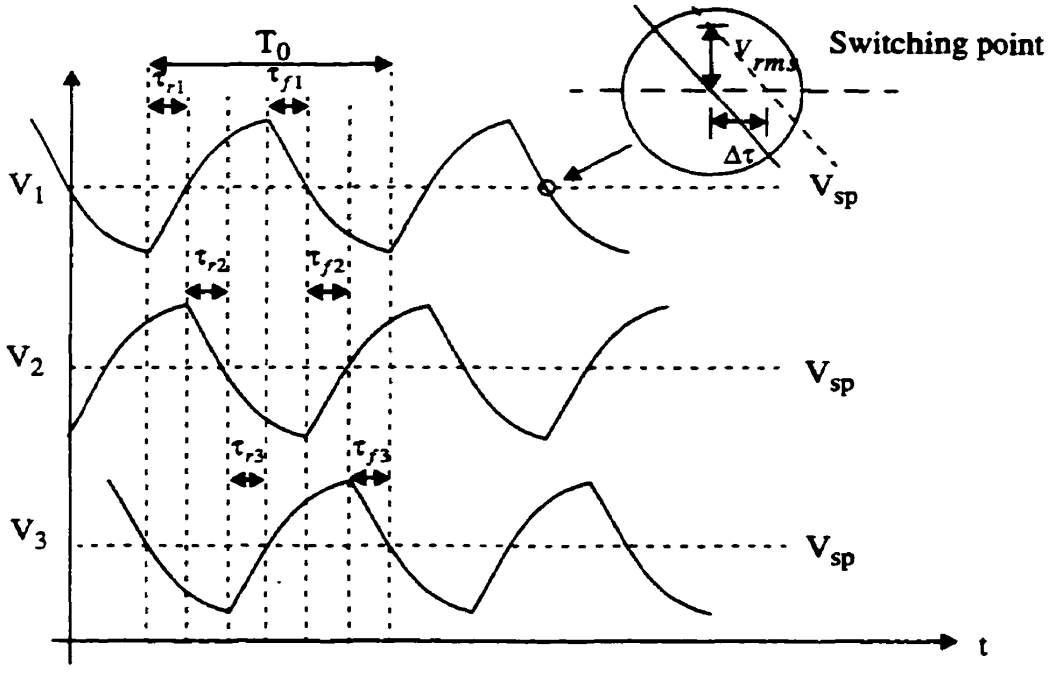


Fig. 4.6. Output waveforms for 3 stage CMOS ring oscillator

Considering that the oscillation of an inverter ring oscillator relies on threshold switching of transistors, a noise model is proposed in Fig. 4.7. Each stage is modeled as a cas-

cade of an integrator and Schmitt trigger. The equivalent noise current produces perturbation voltage on the integrator, thus altering the time taken to reach switching thresholds. This timing error passes to other stages in the ring and contributes to the total output jitter. As shown in [AbMe83] an rms noise voltage $V_{rms}(t_x)$, at the time of threshold crossing, causes timing jitter which is proportional to the voltage error divided by the slopes (S_i) of the output waveform (Fig. 4.6). Thus, we have cycle-to-cycle jitter for N stage ring oscillator as

$$\sigma = \sqrt{\sum_{i=1}^{N}\left[\left(\frac{V_{rms}(t_{spr})}{S_{ri}}\right)^2+\left(\frac{V_{rms}(t_{spf})}{S_{fi}}\right)^2\right]} \tag{4.10}$$

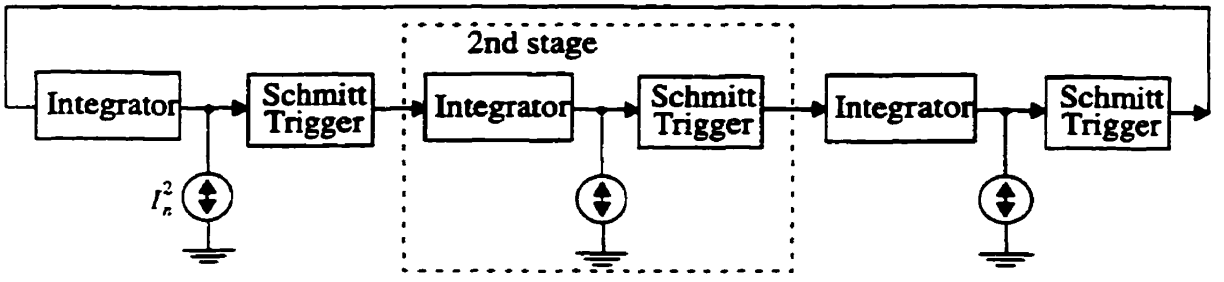


Fig. 4.7. Noise model of ring oscillator at time domain

In order to express timing jitter as a function of period (or oscillation frequency) instead of as a stage number, we need to calculate τ_{ri} and τ_{fi}. It is evident that the fall time, τ_f, consists of two intervals: (a) the period during which NMOS is in saturation and the capacitor voltage, Vout, drops from V_{DD} to (V_{DD}-V_{tn}): (b) the period during which NMOS is in triode region and the capacitor voltage, Vout, drops from (V_{DD}-V_{tn}) to V_{sp}. Thus we have

$$\tau_f = \frac{2C_L}{\beta_n(V_{DD}-V_{tn})}\cdot\int_{(V_{DD}-V_{tn})}^{V_{DD}} dV + \frac{C_L}{\beta_n(V_{DD}-V_{tn})}\cdot\int_{V_{sp}}^{(V_{DD}-V_{tn})} \frac{1}{\frac{V^2}{2(V_{DD}-V_{tn})}-V}\cdot dV \qquad (4.11)$$

$$= k_1\cdot\frac{C_L}{\beta_n V_{DD}}$$

where C_L corresponds to the total output capacitance of the ith stage. $\beta_n = \mu_n C_{ox}(W/L)$ and

$$k_1 = \frac{2n}{(1-n)^2} + \frac{\ln(3-4n)}{(1-n)} \qquad (4.12)$$

with $n = V_{tn}/V_{DD}$. k_1 has value between 1 and 2 for V_{DD}=3 to 5V and V_{tn}=0.5 to 1V. We have assumed threshold voltage V_{sp} ($= V_{DD}/2$).

A similar approach can be used to obtain the rise time, τ_r,

$$\tau_r = k_1\cdot\frac{C_L}{\beta_p V_{DD}} \qquad (4.13)$$

Thus we have oscillation period

$$T_0 = 2Nk_1\cdot\frac{C_L}{\beta V_{DD}} \qquad (4.14)$$

where we have assumed $\beta_n = \beta_p = \beta$ to achieve an equal driving strength from both NMOS and PMOS transistors.

Eq. (4.14) discloses that the period of a single-end ring oscillator is a function of the power supply voltage, the capacitance at output node and the ratio of W/L.

In order to obtain the slope value at the switching point, we develop an analytic model that describes the switching characteristics of a CMOS inverter. The equivalent circuits at the switching point are shown in Fig. 4.8. When the output is at the falling switching point, the PMOS transistor is modeled as an open circuit, and the NMOS transistor can be modeled as a resistor since it is in the triode region.

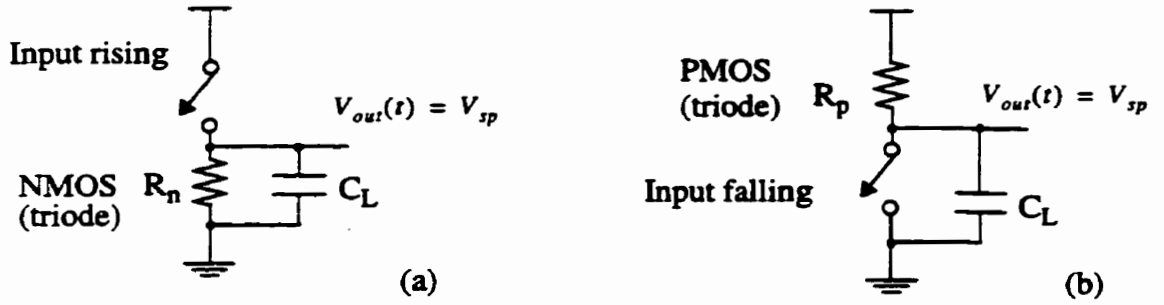


Fig. 4.8. Equivalent circuit for slope value determination at switching point (a) output falling and (b) output rising

From Fig. 4.8, we have $C_L \cdot \frac{dV}{dt} = -\beta_n\left[(V_{DD} - V_{tn}) \cdot V_{sp} - \frac{V_{sp}^2}{2}\right]$. Thus, the waveform falling slope at the switching point is

$$\begin{aligned} S_f &= \frac{1}{C_L} \cdot \beta_n\left[(V_{DD} - V_{tn}) \cdot V_{sp} - \frac{V_{sp}^2}{2}\right] \\ &= k_2 \cdot \frac{\beta_n V_{DD}^2}{C_L} \end{aligned} \tag{4.15}$$

where $k_2 = 0.375 - 0.5n$.

Similarly we have the waveform rising slope at the switching point as $S_r = k_2 \cdot \frac{\beta_p V_{DD}^2}{C_L}$.

The mean square thermal noise voltage for the i_{th} stage output at the switching point is

$$\begin{aligned} V_{n,rms}^2 &= I_n^2 R^2 \int_0 \frac{1}{(1 + j2\pi RC_L f)^2} df = (4kT\gamma g_{m1}) \cdot R^2 \left(\frac{\pi}{2}\right) \frac{1}{2\pi RC_L} \\ &= \frac{kT\gamma}{C_L} \end{aligned} \tag{4.16}$$

where γ is thermal noise parameter as shown in Eq. (4.6).

Substituting Eq. (4.14), Eq. (4.15) and Eq. (4.16) into Eq. (4.10), we have explicit cycle-to-cycle jitter due to thermal noise,

$$\sigma = \sqrt{\frac{T_0}{\tau_r + \tau_f} \cdot \frac{kT\gamma}{C_L} \cdot \left[\frac{1}{S_{ri}^2} + \frac{1}{S_{fi}^2}\right]} = \sqrt{\frac{T_0 kT\gamma}{k_1 k_2^2 \beta V_{DD}^3}} \tag{4.17}$$

Using Eq. (4.4) to transfer timing jitter to phase noise due to thermal noise, we have,

$$S_\phi(\omega) = \frac{\sigma^2 \omega_0^3}{2\pi(\omega - \omega_0)^2} = \frac{kT\gamma\omega_0^2}{k_1 k_2^2 \beta V_{DD}^3 (\omega - \omega_0)^2} \tag{4.18}$$

Eq. (4.17) or Eq. (4.18) leads to the following conclusions:

(a) cycle-to-cycle jitter is inversely proportional to power supply voltage and power consumption ($CV^2 f$), that is, increasing supply voltage reduces jitter;

(b) Jitter is independent of the number of stages if operation frequency is the same;

(c) For a fixed oscillation period, jitter can be reduced by increasing the ratio of W/L. This is due to the increased slope at the threshold crossing point. Thus, attempting to reduce the noise lead to penalties in power and size.

These conclusions are similar to those for the conventional differential ring oscillators in [WKG94]. To prove the effect of selecting the device sizes for the ring oscillator phase noise, we use the test results of [Abou96]. Two VCOs having exactly the same structure as that of Fig. 4.9 were implemented in a 1.2 μm CMOS process. The first circuit was implemented with the process's smallest NMOS device size, and the other with its device size three times as that of the first VCO. SSB Phase noise measurement results at 689 MHz are showed in Fig. 4.10, which demonstrates an improvement of about 3 dB for second circuits at different offset frequencies, except for offset frequencies in the range of the oscillator's noise floor. However, it should be noted that the second circuit employed three times the silicon area and dissipated three times the power (6.5 mW and 19 mW, respec-

tively) which proves that there is a trade-off between power consumption and phase noise.

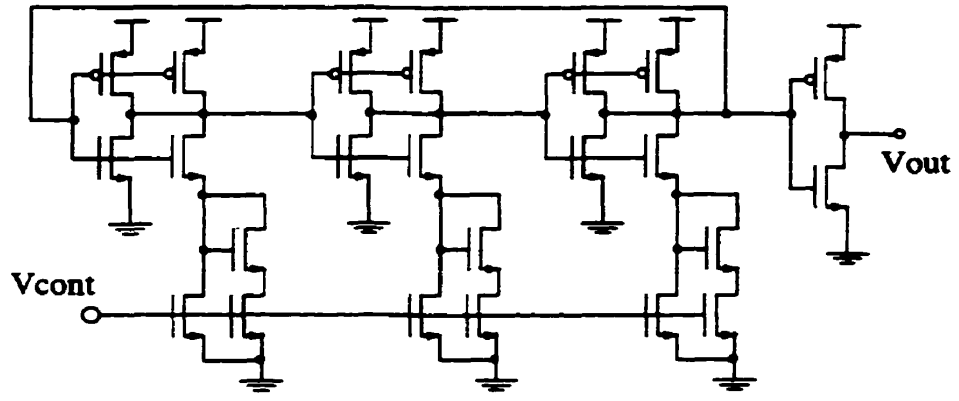


Fig. 4.9. Schematic of the 3 stage CMOS ring oscillator

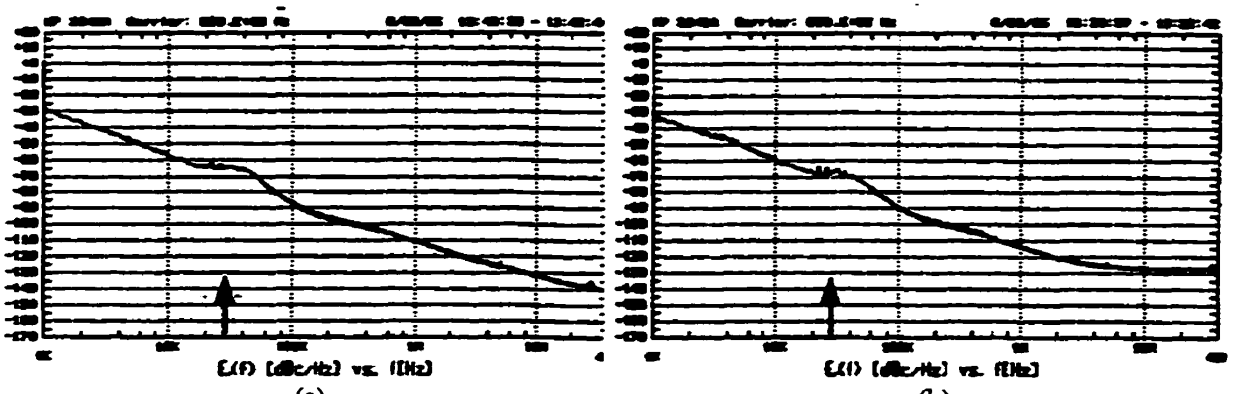


Fig. 4.10. Measured SSB phase noise for (a) minimum device sizes (b) three times the minimum device sizes [Abou96]

The circuit in Fig. 4.9 was optimized and implemented in the Nortel 1.2 μm BiCMOS process by [Abou96], and in the HP 0.5 μm and tsmc 0.35 μm CMOS process by the author, respectively. Fig. 4.11 and Fig. 4.12 show the measured output spectra. Table 4.1 gives a comparison of theoretical and measurement results of phase noise in three different processes. Taking the circuit in the 0.5μm CMOS process as an example, the measured

phase noise at 2.14 GHz is -96.3 dBc/Hz at 1 MHz offset frequency [Fig. 4.11]. The calculated phase noise from Eq. (4.18) is -100 dBc/Hz. All three cases demonstrate a good level of agreement between measurement results and developed analytical formula for phase noise prediction.

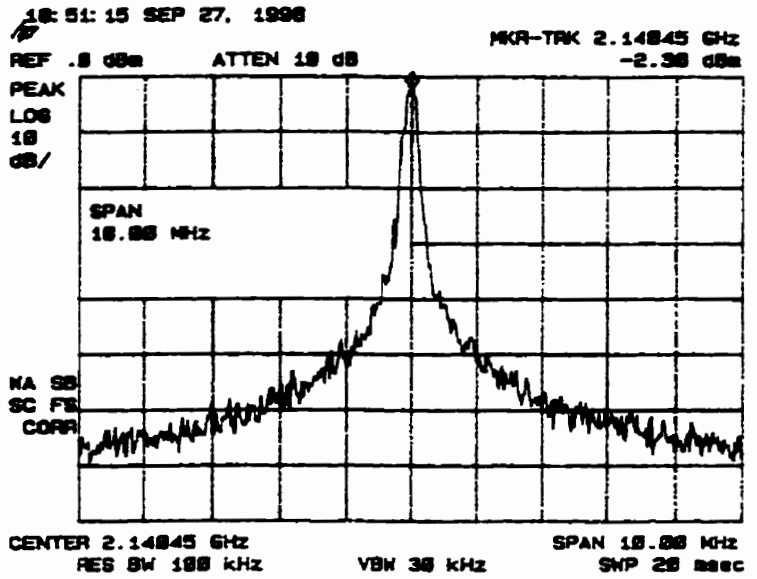


Fig. 4.11. Measured output spectrum of the Fig. 4.9 circuit at 2.14 GHz (0.5 µm CMOS)

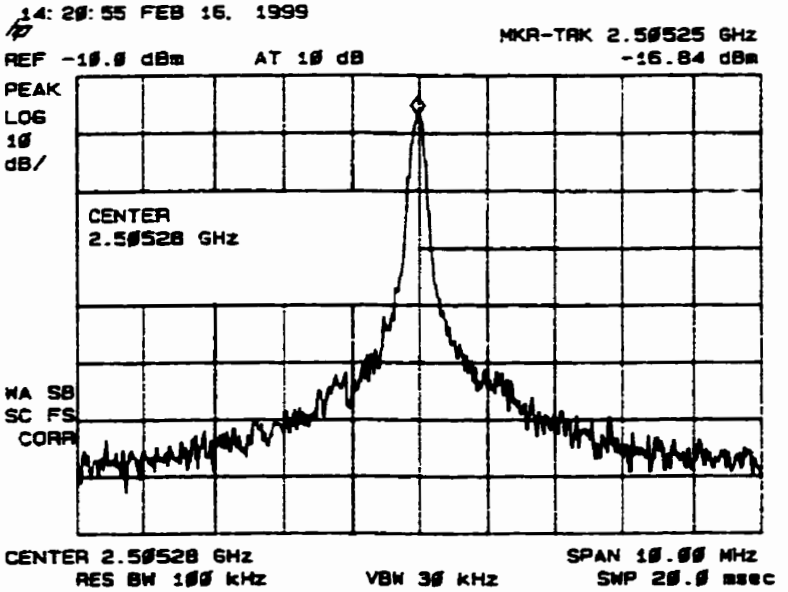


Fig. 4.12. Measured output spectrum of the Fig. 4.9 circuit at 2.5 GHz (0.35 µm CMOS)

Table 4.1 Theoretical and measurement results of phase noise

Technology	f_o	Phase Noise (Theoretical)	Phase Noise (Measurement)	Power Consumption
1.2 μm BiCMOS (VCO2) [Abou96]	720 MHz	-109 dBc/Hz at 1 MHz offset	-112 dBc/Hz at 1 MHz offset	6.3 mW (5V)
0.5 μm CMOS (VCOREF)	2.14 GHz	-100 dBc/Hz at 1 MHz offset	-96.3 dBc/Hz at 1 MHz offset	10.9 mW (3.3V)
0.35 μm CMOS (VCO1)	2.5 GHz	-99.4 dBc/Hz at 1 MHz offset	-96 dBc/Hz at 1 MHz offset	8 mW (3.3V)

4.3.2 Timing Jitter due to Supply and Substrate Noise

According to Eq. (4.14) the oscillation period is dependent on power supply voltage. This is due to ordinary CMOS inverters having a charging/discharging current proportional to the power supply voltage. From Eq. (4.14) we have frequency sensitivity to supply voltage as

$$\frac{\Delta f}{\Delta V_{DD}} = \frac{\beta}{2Nk_1C_L} \tag{4.19}$$

Assuming there is a small sinusoidal perturbation, $\Delta V_{DD}(t) = V_m \cos\omega_m t$ superimposed on the power supply. The deviation of the period from the mean is

$$\Delta T = 2Nk_1 \cdot \frac{C_L}{\beta}\left(\frac{1}{V_{DD}} - \frac{1}{V_{DD}+V_m\cos\omega_m t}\right) \approx 2Nk_1 \cdot \frac{C_L}{\beta}\frac{V_m\cos\omega_m t}{V_{DD}^2} \tag{4.20}$$

The autocorrelation function of Eq. (4.20) with respect to t is

$$C_{TT}(\tau) = \overline{\Delta T(t+\tau)\cdot\Delta T(t)} = 2\left(Nk_1 \cdot \frac{C_L}{\beta}\frac{V_m}{V_{DD}^2}\right)^2 \cdot \cos\omega_m\tau \tag{4.21}$$

It can be proved that mean square cycle-to-cycle jitter σ^2 is equal to $2C_{TT}(\tau)|_{\tau=0} - 2C_{TT}(\tau)|_{\tau=1/f_0}$ [HeRa98], Thus from Eq. (4.21), we have

$$\sigma = \frac{T_0^2 \omega_m}{\sqrt{2}} \cdot \left(\frac{V_m}{V_{DD}}\right) \tag{4.22}$$

Eq. (4.22) indicates that for a fixed oscillation period, jitter is proportional to both perturbation amplitude as a fraction of the power supply voltage and perturbation frequency. For a 2 GHz oscillator with noise voltage 1% of supply voltage and noise frequency of 1GHz, we obtain a jitter of 1.5 ps from Eq. (4.22), which is larger than the jitter due to the internal noise source (<1 ps). Although an on-chip voltage regulator can be used to reduce low frequency supply noise sensitivity [WLS89], high frequency noise remains a critical noise source causing degradation of timing jitter. Furthermore, it reduces the effective supply voltage applied to VCO core circuits, making it undesirable for low-supply applications. In most practical applications, fully differential inverters are used to obtain lower supply and substrate noise sensitivity at the cost of decreased voltage swing, speed, tuning range and increased power consumption.

4.4 Analysis of Phase Noise in Sub-feedback Loop Based Ring Oscillators

In this section, phase noise will be analysed in the frequency domain. The first order linear frequency domain noise analysis method [Lee66][Raza96] is extended to sub-feedback loop based ring topology. Compared to time domain analysis, frequency domain analysis provides more insight to both time domain waveform shaping (as we observed in Fig. 3.8 and Fig. 3.9) and noise filtering introduced by the sub-feedback loop based architecture.

Fig. 4.13 illustrates a single stage circuit of a differential ring oscillator with feedback inverter and noise sources. The noise in each transistor and resistor has been modeled using an equivalent current noise source. Power supply noise is modeled as an equivalent voltage noise source. These noise sources can be classified into three groups according to

their different mechanism to the output phase noise: (1) noise from driving transistors and loading resistors (M_1, M_2, M_3, M_4, R_1, R_2) which are connected directly to the signal path, (2) tail current noise which modulates the oscillation frequency and (3) power supply and substrate noise which belong to external interference signals. The following subsection is the analysis of phase noise corresponding to each group of noise sources.

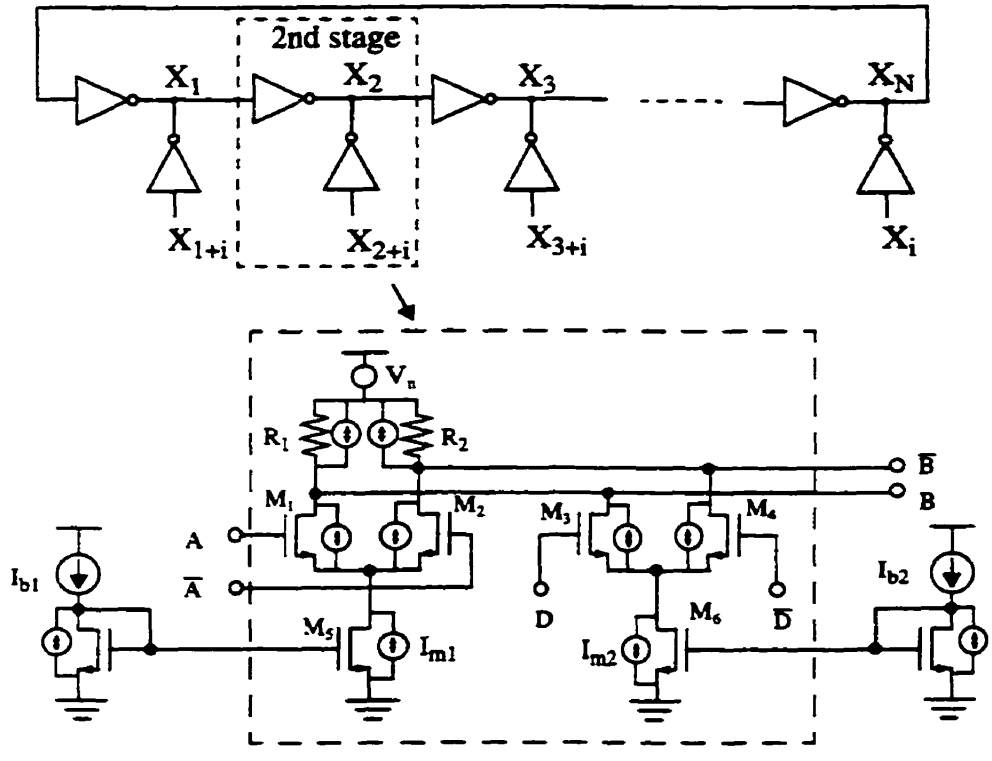


Fig. 4.13. A single stage circuit including noise sources

4.4.1 Driving Transistor and Loading Resistor Noise

In order to analyse the phase noise contributed by transistors (M_1, M_2, M_3, M_4) and resistors (R_1, R_2) which are directly connected to the signal path, we will first model the oscillator with a linear system, assuming that oscillation amplitude is small and that gain stages operate in its linear region. The mixing or modulation effects that result from the nonline-

arity of circuits will be considered later and the formula derived from the linear model will be modified. A linear oscillator model is shown in Fig. 4.14. The output noise power density of the closed-loop system is

$$V_{out}^2 = V_{in}^2\left[\frac{T_1(j\omega)}{1+T(j\omega)}\right]^2 \tag{4.23}$$

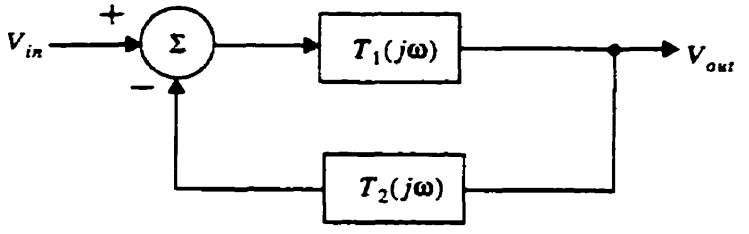


Fig. 4.14. Linear oscillator model

where $T(j\omega) = T_1(j\omega)\cdot T_2(j\omega)$ is open loop transfer function and V_{in}^2 represents input noise power.

For frequencies close to the carrier, both $|T_1(j\omega)|$ and $|T(j\omega)|$ are approximately equal to one, and the open-loop transfer function can be approximated as $T(j\omega) \approx T(j\omega_0) + \Delta\omega \cdot \frac{dT}{d\omega}$. Thus, the output noise density is

$$V_{out}^2 = V_{in}^2\frac{1}{\left[\Delta\omega \cdot \frac{dT}{d\omega}\right]^2} \tag{4.24}$$

Let $T(j\omega) = A(\omega)\exp[j\Phi(\omega)]$, and hence $\frac{dT}{d\omega} = \left(\frac{dA}{d\omega} + jA\frac{d\Phi}{d\omega}\right)\exp(j\Phi)$. Since for $\omega = \omega_0$, $A = 1$, Eq. (4.24) can be written as [Raz961],

$$V_{out}^2 = V_{in}^2\frac{1}{(\Delta\omega)^2\left[\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\Phi}{d\omega}\right)^2\right]} \tag{4.25}$$

To perform a first order analysis of the phase noise of the topology proposed in Chap-

ter 3, we will model the sub-feedback loop based ring oscillator with a linearized circuit as shown in Fig. 4.15. The additive noise of each stage, which are connected directly to the signal path, are modeled as current sources I_n, injected on to the corresponding node.

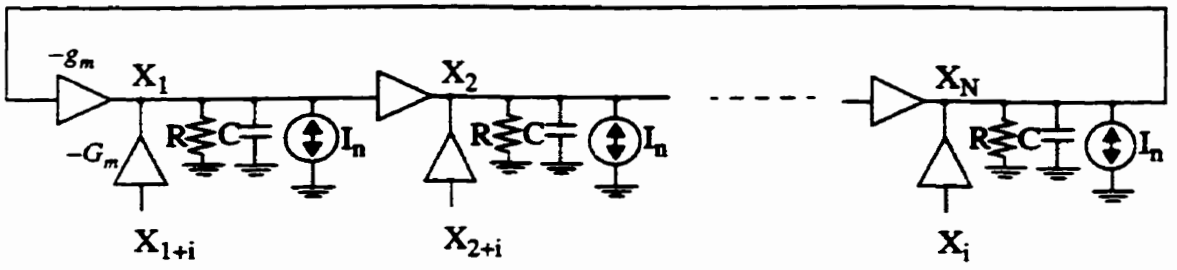


Fig. 4.15. Linearized model of the ring oscillator for additive noise in signal path

From Eq. (3.1), we have the open loop transfer function

$$T(j\omega) = \left[\frac{-g_m R}{(1 + G_m R\cos\phi) + j(\omega RC - G_m R\sin\phi)}\right]^N \tag{4.26}$$

Thus,

$$\begin{cases} \dfrac{dA}{d\omega} = \dfrac{N(\omega RC - G_m R\sin\phi)RC}{(g_m R)^2} \\ \dfrac{d\Phi}{d\omega} = \dfrac{N(1 + G_m R\cos\phi)RC}{(g_m R)^2} \end{cases} \tag{4.27}$$

Substituting Eq. (4.27) into Eq. (4.25), we have noise power density,

$$\begin{aligned} V_{out}^2 &= V_{in}^2\left(\frac{g_m R}{N\omega_0 RC}\right)^2\left(\frac{\omega_0}{\Delta\omega}\right)^2 \\ &= \frac{(1 + G_m R\cos\phi)^2 \cdot [1 + (\tan\theta)^2] \cdot V_{in}^2}{(\tan\theta + k_0 \cdot G_m R)^2 N^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \end{aligned} \tag{4.28}$$

Considering that $V_{in}^2 = I_n^2 Z^2 = (I_n^2 R^2)/[1 + (\tan\theta + k_0 \cdot G_m R)^2]$, Eq. (4.28) can be rewritten

as,

$$V_{out}^2 = \frac{(1+G_mR\cos\phi)^2 \cdot [1+(\tan\theta)^2] \cdot I_n^2R^2}{[1+(\tan\theta+k_0 \cdot G_mR)^2] \cdot (\tan\theta+k_0 \cdot G_mR)^2N^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{4.29}$$

Now let us consider the noise mixing effect. The nonlinearity in the circuit due to large voltage swing and switching of the differential pair causes noise to be multiplied by the carrier. This mixing effect folds all the noise components below ω_0 to the region above ω_0 and vice versa, effectively doubling the noise power predicted by Eq. (4.29). Thus we have output noise due to the driving transistors and loading resistors as

$$V_{out}^2 = \frac{2(1+G_mR\cos\phi)^2 \cdot [1+(\tan\theta)^2] \cdot I_n^2R^2}{[1+(\tan\theta+k_0 \cdot G_mR)^2] \cdot (\tan\theta+k_0 \cdot G_mR)^2N^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{4.30}$$

Taking a 4 stage sub-feedback loops based differential ring oscillator as example, if only thermal noise is considered, we have noise current $I_n^2 = 4kT(\gamma g_m + 1/R + \gamma G_m)$ for a single differential delay stage as shown in Fig. 4.13. Then the total output noise power density is

$$\begin{aligned} V_{out}^2 &= \frac{I_n^2R^2}{2[1+(1+G_mR)^2](1+G_mR)^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \\ &= \frac{2kTR(\gamma\sqrt{2}+1+\gamma G_mR)}{[1+(1+G_mR)^2](1+G_mR)^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \end{aligned} \tag{4.31}$$

which improves with the increase of G_m at the cost of higher power consumption.

Closed loop noise transfer function given by Eq. (4.28) can be compared with a closed loop transfer function expression of Leeson's model for a LC tank based oscillator (about the center frequency ω_0),

$$V_{out}^2 = V_{in}^2 \frac{1}{4Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{4.32}$$

We obtain an equivalent open loop Q for a ring oscillator, Q_r,

$$Q_r = \frac{N\omega_0 RC}{2g_m R} = \frac{N[\tan\theta + k_0 \cdot G_m R]}{2(1 + G_m R\cos\phi)\sqrt{1 + (\tan\theta)^2}} \tag{4.33}$$

where $k_0 = \sin\phi + \tan\theta \cdot \cos\phi$ as defined in (3.6).

Eq. (4.33) can be also obtained by directly applying the expression for Q as introduced by [Raz961],

$$Q_r = \frac{\omega_0}{2}\left|\frac{dT}{d\omega}\right| = \frac{\omega_0}{2}\sqrt{\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\Phi}{d\omega}\right)^2} \tag{4.34}$$

For a 4 stage ring oscillator with sub-feedback loops ($i = 2$, $\theta = 5\pi/4$), we have

$$Q_r = \sqrt{2}(1 + G_m R) \tag{4.35}$$

which increases linearly with $G_m R$. For 7 stage ring oscillators with sub-feedback loops, equivalent Q_r as function of $G_m R$ are illustrated in Fig. 4.16 for i=2 and 4. It is observed that the topology based on 5 stage sub-feedback loops (i=4) has a higher Q_r value than that based on 3 stage sub-feedback loops (i=2). This stronger frequency selectivity in signal path thus produces more sinusoidal like time domain waveform at the output as illustrated in Fig. 4.17. Considering the fact that two circuits have close operating frequency, the same number and magnitude of noise sources, the 5 stage sub-feedback loop based circuit (i=4) is expected to have better noise performance compared to that of 3 stage sub-feedback loops based circuits (i=2). Similar analysis can be applied to other stage number of ring oscillators, e.g., for 9 stage ring oscillators, the equivalent Q_r as function of $G_m R$ are illustrated in Fig. 4.18 for i=2, 4 and 6. The circuit based on i=6 generates more sinusoidal

like time domain waveforms at the output [Fig. 3.9] due to the stronger frequency selectivity in the signal path.

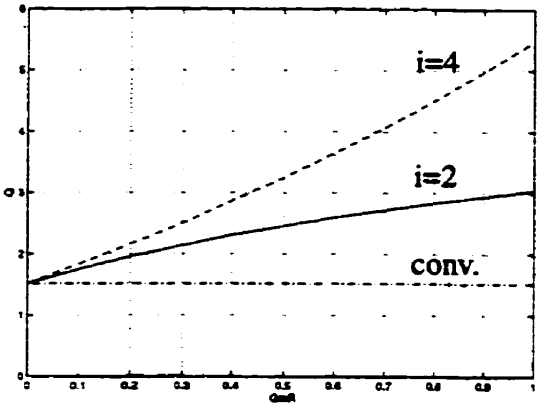


Fig. 4.16. Equivalent Q_r as function of $G_m R$ for 7 stage sub-feedback loop based ring oscillators (feedback index i=2 and 4, respectively)

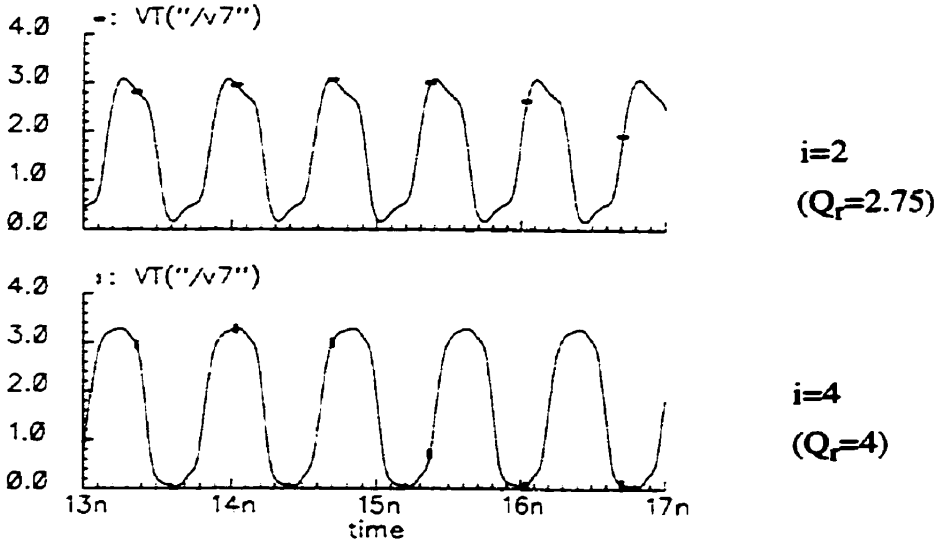


Fig. 4.17. Comparison of time-domain waveforms for feedback index *i*=2 and 4 topology (7 stages ring)

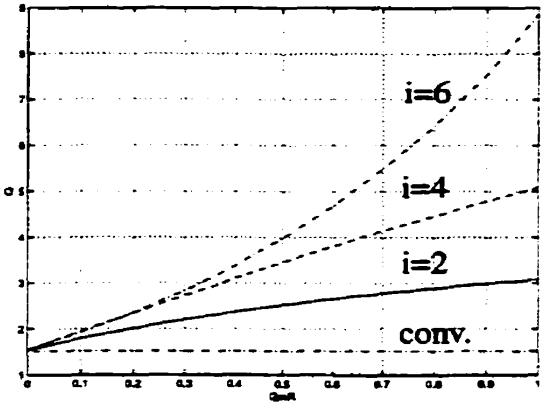


Fig. 4.18. Equivalent Q_r as function of G_mR for 9 stage sub-feedback loop based ring oscillators (feedback index i=2, 4, 6, respectively)

4.4.2 Tail Current Noise

The current controlled oscillator (ICO) or the VCO with voltage to current converter embedded for frequency control unavoidably suffers from the input noise modulation. The low frequency noise components at the oscillator input modulate the oscillator operating frequency, therefore, contributing to the close-in phase noise (Fig. 4.19). The effect is similar to frequency modulation (FM) [McN94] [Raz961]. It is also called the varactor modulation phase noise for LC oscillator [Rhe95].

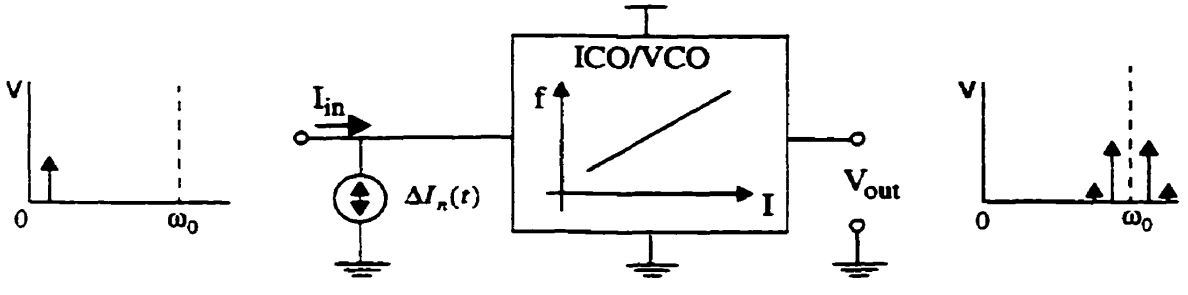


Fig. 4.19. Noise modulation at VCO input

For the differential circuit shown in Fig. 4.20, the modulation signal comes from the tail current noise. Assuming there is a small sinusoidal perturbation, $\Delta I_n(t) = I_m \cos\omega_m t$, superimposed on the tail current source, then the output signal of the oscillator is

$$\begin{aligned} V(t) &= A_0 \cos(\omega_0 t + 2\pi K_{ICO} \int I_m \cos\omega_m t \cdot dt) \\ &= A_0 \cos(\omega_0 t) + \frac{A_o I_m K_{ICO}}{2 f_m} [\cos(\omega_0 + \omega_m)t - \cos(\omega_0 - \omega_m)t] \end{aligned} \tag{4.36}$$

where $K_{ICO} = (df)/(dI_{ss})$ is frequency to current sensitivity. It can be easily obtained with measurement or simulations.

Thus, the total output noise power density due to the tail current noise for N stage ring oscillator is

$$V_{out}^2 = N\left(\frac{A_o I_m K_{ICO}}{2\sqrt{2} \cdot f_m}\right)^2 \tag{4.37}$$

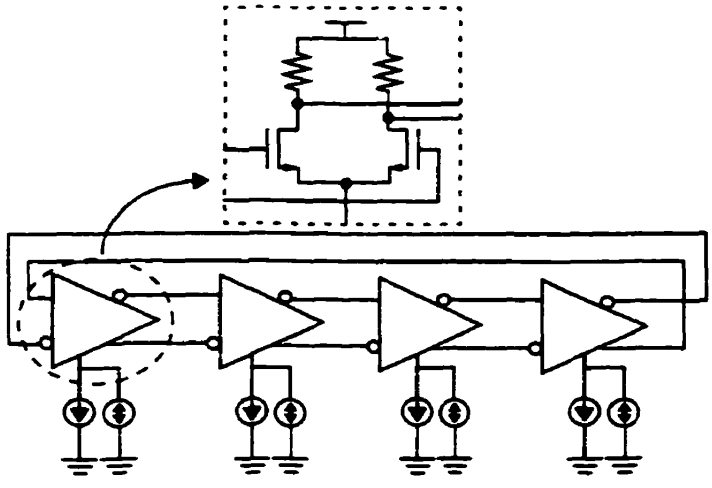


Fig. 4.20. Low frequency modulation due to tail current noise

For sub-feedback loop based ring oscillators (Fig. 4.21), there are two tail current sources in each stage. Thus Eq. (4.37) should be modified as

$$V_{out}^2 = N\left(\frac{A_o}{2\sqrt{2}\cdot f_m}\right)^2 [(I_{m1}K_{ICO1})^2 + (I_{m2}K_{ICO2})^2] \tag{4.38}$$

where I_{m1} and I_{m2} represent the noise current appear in the two tail, respectively (Fig. 4.21).

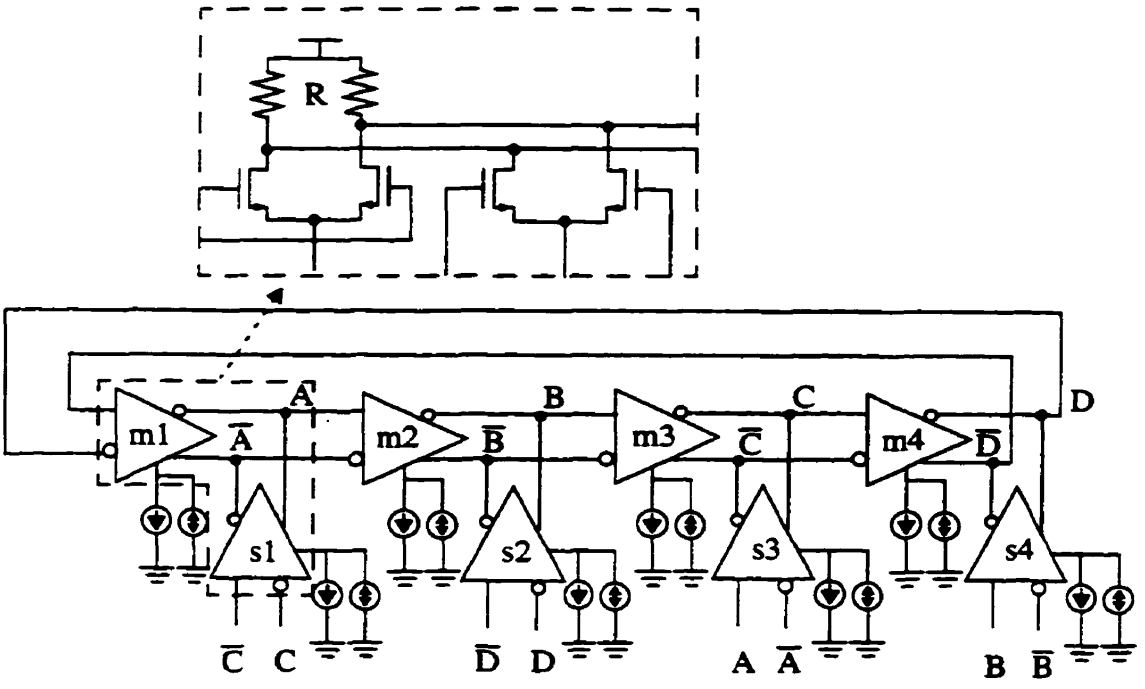


Fig. 4.21. Tail current modulation for the sub-feedback loop based ring oscillator

Eq. (4.37) illustrates that oscillators that have a large gain can also be tuned easily by noise. Oscillators that resist to be tuned also resist the influence of noise. Increasing the oscillator power level does not result in a direct reduction in oscillator phase noise as it does for the driving transistor and loading resistor noise sources. The modulation effect due to tail current noise is significant for sub-feedback loops based oscillators since the topology increases K_{ICO} for high speed and wide tuning range. To lower the phase noise at a given power dissipation, it is desirable to reduce the value of frequency sensitivity K_{ICO}.

4.4.3 Power Supply and Substrate Noise

The basic reason for preferring differential circuits is that they can be made to reject external interference better. However, even for a differential circuit, rejection occurs only partially due to the following mechanism:

(1) If resistor loads are realized with MOS devices (Fig. 4.22), they can not maintain linearity for a large range of V_{DS} voltage. The resistance is dependent on common-mode voltage that carries the supply noise. Nonlinear load resistance cause common-mode noise conversion into differential-mode noise. Even though resistors are made with poly-silicon, the unavoidable mismatching degrades the symmetry of the circuit.

(2) The drain junction capacitance of each transistor is a function of V_{DD} and V_{sub}, modulating the delay of each stage as noise appears in either voltage [HeRa98].

(3) Total capacitance at the common source of the differential pair and the capacitance associated with tail current converts the substrate noise to current, thereby modulating the delay of the gain stage [Raz961].

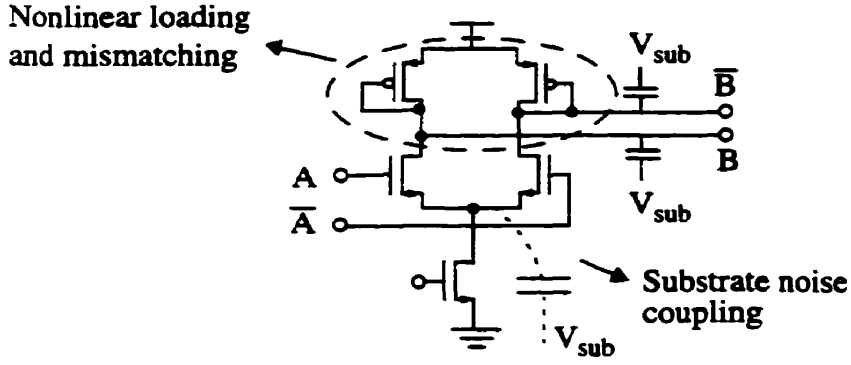


Fig. 4.22. Phase noise due to supply and substrate noise

We can analyze the phase noise due to the power supply or substrate noise using a method similar to the tail current noise method. We define the frequency sensitivity to supply voltage as $K_v = df/(dV_{DD})$ which can be also obtained with measurement or simulation. Assuming there is a small sinusoidal perturbation voltage, $\Delta V_{DD}(t) = V_m \cos\omega_m t$ is superimposed on the power supply. Then the output signal of the oscillator is

$$\begin{aligned} V(t) &= A_0 \cos(\omega_0 t + 2\pi K_v \int V_m \cos\omega_m t \cdot dt) \\ &= A_0 \cos(\omega_0 t) + \frac{A_o V_m K_v}{2 f_m}[\cos(\omega_0 + \omega_m)t - \cos(\omega_0 - \omega_m)t] \end{aligned} \tag{4.39}$$

Thus, the total output noise power due to the power supply noise is

$$V_{out}^2 = \left(\frac{A_o V_m K_v}{2\sqrt{2} \cdot f_m}\right)^2 \tag{4.40}$$

Phase noise due to the supply and substrate noise is significant when oscillators are integrated with digital systems. Wide band noise due to current spikes produced by digital circuit may couple into the oscillator circuit through shared power supply and substrate.

4.4.4 Summary of Phase Noise Analysis and Experimental Results

The formula to be used for the single sided spectral phase noise is

$$L(f_m) = 10 \cdot \log \frac{\int_{(f_0 + f_m - 1/2)}^{(f_0 + f_m + 1/2)} dV_{tot}^2}{A_0^2/2} \tag{4.41}$$

where V_{tot}^2 is the summation of the noise power contributed by all types of noise sources with the assumption that these noise sources are noncoherent. A_0 is carrier amplitude (voltage swing).

Eq. (4.41) exhibits that a large output signal swing is critical for reducing phase noise.

However, voltage swing is often limited by the supply voltage, gain cell structure and operating frequency.

Taking the 4 stage ring oscillator VCO3 circuit in Chapter 3 as an example, the associated parameters used for VCO3 phase noise calculation at 1.25 GHz are listed in Table 4.2. Only thermal noise is considered. Using Eq. (4.31), phase noise due to driving transistors and loading resistors is found equal to -104 dBc/Hz at 5 MHz offset frequency. With Eq. (4.38) phase noise due to tail current noise is -115.7 dBc/Hz. Obviously, the driving transistor and loading resistor noise is the dominant noise source for this oscillator. The total phase noise due to these two group noise sources is -103.5 dBc/Hz. The measured phase noise is -103 dBc/Hz at 5 MHz offset frequency [Fig 3.34]. There is an error of only 0.5 dB between theoretical and experimental results. We have ignored the supply and substrate noise since only the oscillator circuit is operating on the chip.

Table 4.2 Parameters used for VCO3 (0.5μm CMOS) phase noise calculation at 1.25 GHz

f_m	5 MHz
kT	0.41×10^{-20} JK^{-1}
γ	1.0
I_{m1}^2	0.23×10^{-23} A^2
I_{m2}^2	0.164×10^{-23} A^2
K_{ICO1}	2.66×10^{12} Hz/A
K_{ICO2}	5.56×10^{12} Hz/A
G_m	40×10^{-6} 1/ohm
R	20.36×10^{3} ohm
A_0	340 mV

4.5 Summary

In this chapter the phase noise in single-ended ring oscillators and sub-feedback loop based differential ring oscillators has been analysed. For single-ended ring oscillator, the analysis is based on a time domain noise model. The relationship between design parameter and timing jitter is derived for internal noise sources. The cycle-to-cycle jitter was shown to be inversely proportional to supply voltage and power consumption. For a fixed operation frequency, jitter is independent of stage number and can be reduced by increasing the ratio of W/L. The analysis of timing jitter in a single-ended ring oscillator also demonstrate its strong sensitivity to external interference signals, such as supply and substrate noise. The basic reason for exploring differential circuit implementations is that they can be made to reject external interference better. However, even for a differential circuit, rejection can only partially occur due to the nonlinear loading, drain junction capacitor and mismatching of devices.

Phase noise in sub-feedback loop based ring oscillators has been analyzed in the frequency domain. Compared to time domain analysis, frequency domain analysis provides insight into the time domain waveform shapes and into the noise filtering introduced by the sub-feedback loops based architecture. Noise sources affecting the total output phase noise are classified into three groups according to their different mechanisms. The introduced sub-feedback loop based ring topology improves equivalent open loop Q factor and noise shaping function for the noise from the driving transistors and loading resistors which are connected directly to the signal path. The Q value is a function of gain of the feedback inverter and feedback index i. By choosing the optimum feedback index i, phase noise performance can be improved for the sub-feedback loop based ring oscillators (e.g., for 7 stage ring oscillator with sub-feedback loops, the circuit based on i=4 is expected to have better noise performance compared to the circuit based on i=2).

CHAPTER 5

Design and Analysis of GHz Monolithic CMOS Phase - Locked Loop Clock Generator

5.1 Introduction

With the expanding volume of data traffic, demand for a higher LANs data rate keeps growing. This chapter presents the design and analysis of a GHz CMOS monolithic phase-locked loop clock generator for high speed data communications [SuKw992]. In Section 5.2, the building blocks for the PLL are explored. The current controlled ring oscillator developed in Chapter 3 combined with a frequency control and stabilizing scheme is proposed to achieve not only a large and linear tuning range but also to reduce temperature and supply voltage sensitivity. The achieved linear frequency transfer characteristic is important for maintaining a constant loop gain in the PLL over its lock range. Section 5.3 presents the loop stability analysis and acquisition simulation for the 1.25 GHz PLL. Since one of the most demanding PLL specifications is phase noise, an analysis of phase noise associated with each component is presented in Section 5.4. The monolithic implementation and measurement results are summarized in Section 5.5.

5.2 PLL Building Blocks

Fig. 5.1 shows the functional block diagram of a clock generator for data communications. The PLL includes a phase and frequency detector (PFD), charge pump, on-chip loop filter (LPF), VCO and prescaler/divider. The output clock frequency is 1244.16 MHz [ANST][BCR]. The clock is synthesized from a 77.76 MHz or 19.44 MHz reference with corresponding divider's division ratios of 16 and 64, respectively. The design considerations of the PLL block include low voltage operation (3.3 V for this design), low power consumption, monolithic integration, low timing jitter and good supply and substrate noise rejection. In the following subsections, the design of each building block will be discussed with the major focus on VCO design for this monolithic PLL application.

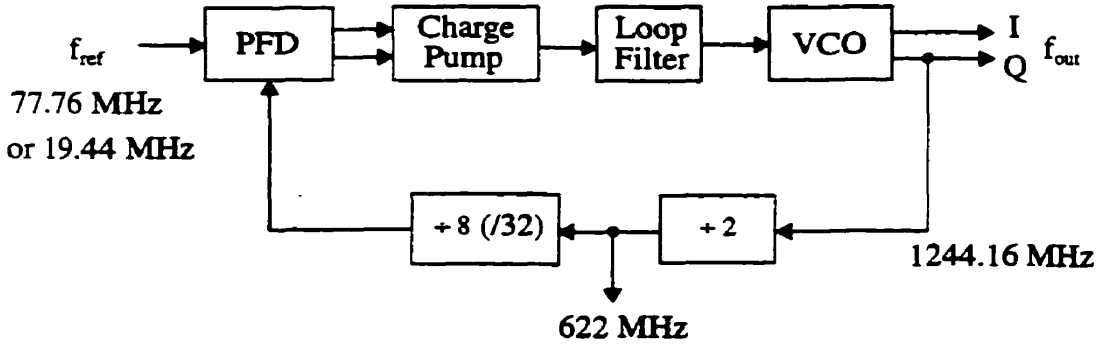


Fig. 5.1. Functional block diagram

5.2.1 The VCO and its Biasing Circuitry

The voltage controlled oscillator (VCO) is a critical building block in phase-locked loops. The design of a VCO for practical applications needs to accommodate process, supply voltage and temperature variations. The integrated VCO block diagram is shown in Fig. 5.2. It consists of four parts: current controlled ring oscillator core circuitry; biasing reference; control voltage to control current converter; output buffer circuit. The four stage

differential ring oscillator based on 3 stage sub-feedback loops [Fig. 3.17 and Fig. 3.25] is utilized as the ICO core circuit. It provides a large and linear tuning range, high-speed operation and a pair of quadrature phase output signals. The two separate tail current sources associated with each stage of the ring oscillator are connected to temperature compensated biasing and to a V-to-I converter, respectively [Fig. 5.3]. Cascode circuits are used in tail current sources to achieve high impedance, thus improved static supply noise rejection. The biasing reference is used to reduce the supply and temperature sensitivity of the oscillator. The buffer circuit consists of differential to single-end converter and amplifier.

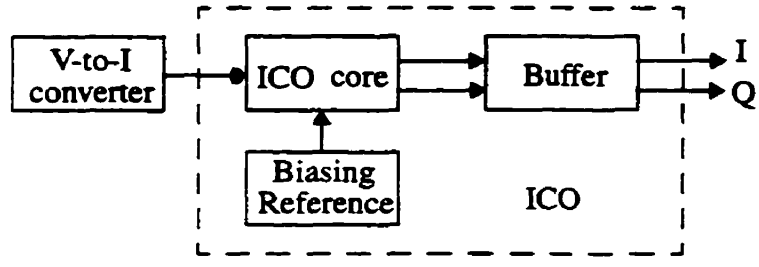


Fig. 5.2. Integrated VCO block diagram

5.2.1.1 Temperature Compensated Biasing

A Proportional to Absolute Temperature Bandgap Reference (PTAT) is designed to provide biasing current to VCO as shown in Fig. 5.3. The output current from the PTAT circuit changes proportionally with the absolute temperature. This increased current is used to compensate for the transistor mobility degradation at high temperatures. The oscillating frequency thus remains constant without control voltage adjustments.

From the analysis in Chapter 3, the oscillation frequency of the four stage ring oscillator is

$$\omega_o = 1/(RC) + G_m/C \tag{5.1}$$

For active loading using a diode connected transistor (with size W_p), we have load resistance

$$R = 1/\left(\sqrt{\mu_p C_{ox}\left(\frac{W_p}{L}\right)I_{b1}}\right) \tag{5.2}$$

I_{b1} is the tail current in the major loop. In Eq. (5.1), R is inversely proportional to the square-root of the mobility μ_p. As the temperature rises, μ_p decreases, thus oscillating frequency decreases. In order to maintain the oscillation frequency when temperature increases, R should be kept constant. Thus, I_{b1} should be increased such that it is inversely proportional to mobility, μ_p. The left side of Fig. 5.3 shows the biasing circuit which provides a biasing current that is inversely proportional to mobility. The circuit can be called a PTAT circuit without using bipolar transistor. Since $(W/L)_{M5}=(W/L)_{M6}$, $(W/L)_{M7}=(W/L)_{M8}$, the equality results in both sides of the circuit having the same current ($I_1=I_2=I$) due to the current-mirror pair (M_5, M_7) and (M_6, M_8). Now, around the loop consisting of (M_1, M_3), (M_2, M_4) and R_b, we have

$$V_{gs1} = V_{gs2} + IR_b \tag{5.3}$$

and recalling that $V_{eff} = V_{gs} - V_t$, we can subtract the threshold voltage, V_t, from both sides, resulting in $V_{eff1} = V_{eff2} + I_2R$. Eq. (5.3) can be written as

$$\sqrt{\frac{2I}{\mu_p C_{ox}(W/L)_1}} = \sqrt{\frac{2I}{\mu_p C_{ox}(W/L)_2}} + IR_b \tag{5.4}$$

Rearranging, we obtain the output current

$$I = \frac{2}{\mu_p C_{ox} R_b^2}\left(\sqrt{\frac{L_1}{W_1}} - \sqrt{\frac{L_2}{W_2}}\right)^2 \tag{5.5}$$

Substituting Eq. (5.5) into Eq. (5.2), we have

$$R = R_b\left[\frac{1}{\sqrt{2}\cdot\sqrt{W_p/L}\cdot(\sqrt{L_1/W_1}-\sqrt{L_2/W_2})}\right] \tag{5.6}$$

Thus, the R is determined by geometric ratios only, first-order independent of temperature, process parameters, and power-supply voltage. Post layout simulation was performed using 0.35 μm CMOS TSMC model. The results are shown in Fig. 5.4 (with I_{b1} = 180μA and R_b = 290Ω). The current control characteristic (f versus I_{b2}) has a good linearity and indicate a gain of 2.98 GHz/mA. The temperature sensitivity is only -200 ppm/°C. For comparison, Fig. 5.5 shows the simulation results using a uncompensated biasing (constant current source) and reveals a sensitivity to temperature of -485 ppm/°C.

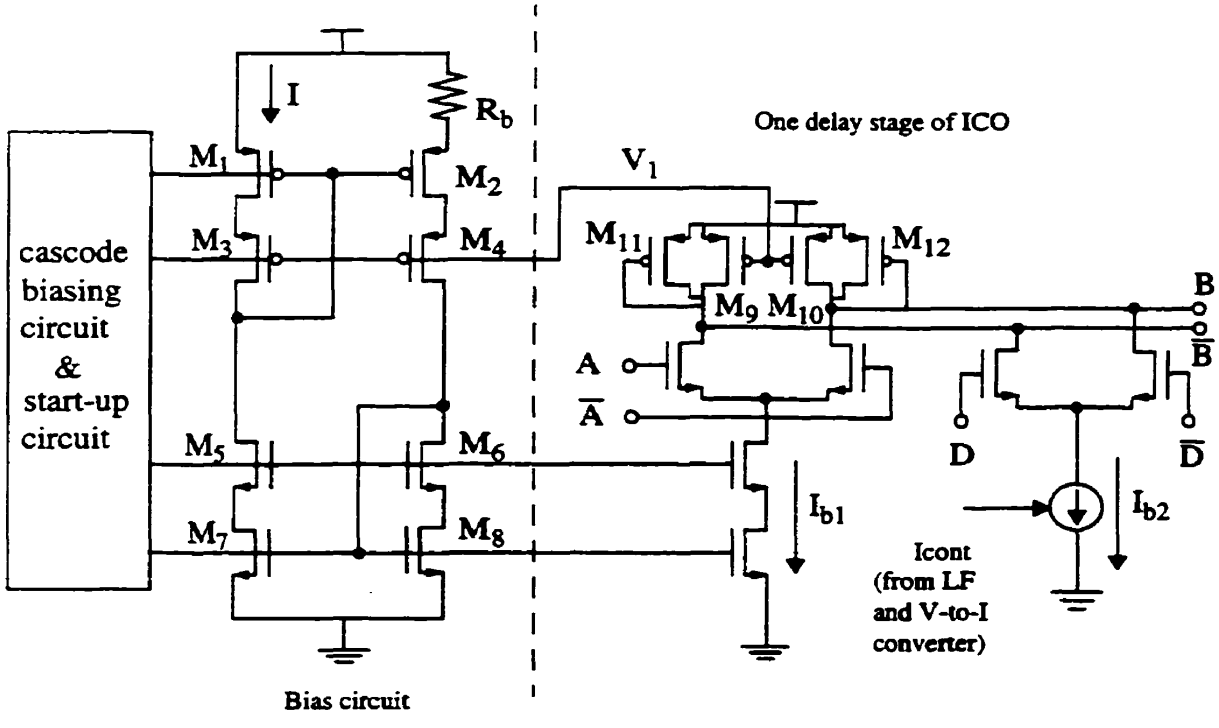


Fig. 5.3. Biasing scheme for temperature compensation and frequency control

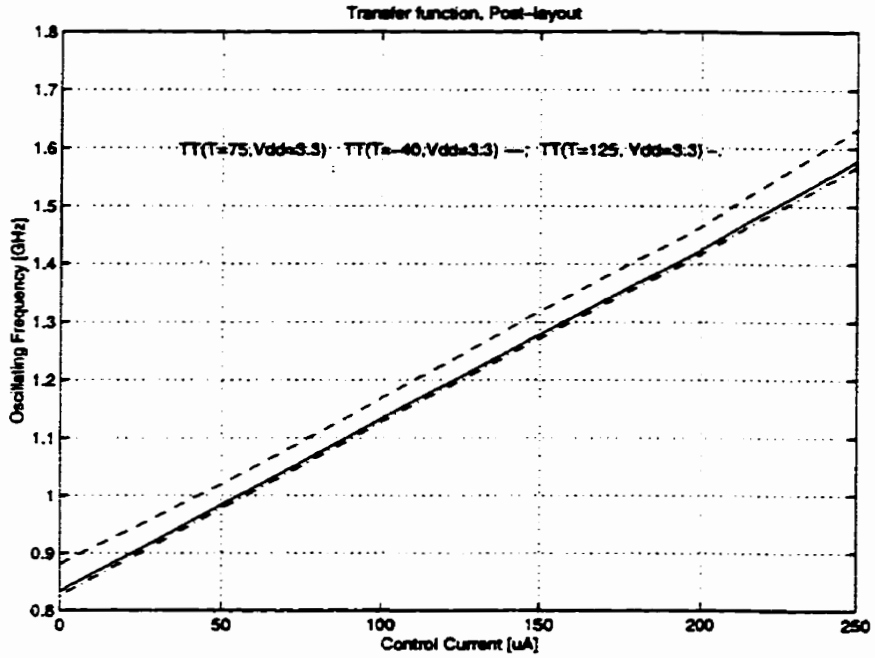


Fig. 5.4. Oscillation frequency as function of control current with temperature as parameter using temperature compensation biasing circuit (post layout simulation results)

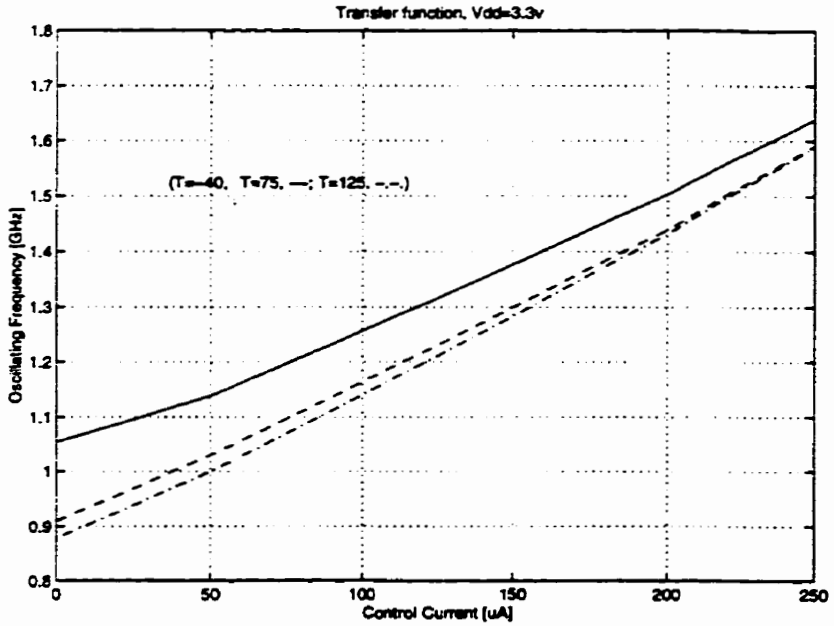


Fig. 5.5. Oscillation frequency as function of control current (without temperature compensation)

5.2.1.2 Reducing the Sensitivity to Supply Noise

Nonlinear load resistances in differential delay circuits can convert common-mode noise in the power supply into differential-mode noise, thus degrading the VCO jitter performance. By connecting a diode-connected PMOS device in shunt with an equal size biased PMOS device, the linearity of loading can be improved [MZN90][Mane96].

The voltage V_I from the bias circuit is used to bias triode PMOS devices in order to reduce the effect of the power supply variation (Fig. 5.3). An increase in power supply voltage V_{DD} will cause V_I to increase correspondingly (Fig. 5.6). However, the effective voltage (V_{eff}) across the triode PMOS loading transistors remains unchanged. Thus, the loading resistance also remains constant. Fig. 5.7 shows the simulated post layout oscillation frequency as a function of the control current with power supply voltage as parameter. The changes on V_{DD} have little effect on the oscillation frequency. The ICO's sensitivity to power supply variation ($(\Delta f/f)/\Delta V_{dd}$) is only 6%/V at the center frequency of 1.25 GHz. For comparison, the oscillation frequency for conventional constant voltage biasing is shown in Fig. 5.8, which indicates a sensitivity to the power supply variation of 56%/V.

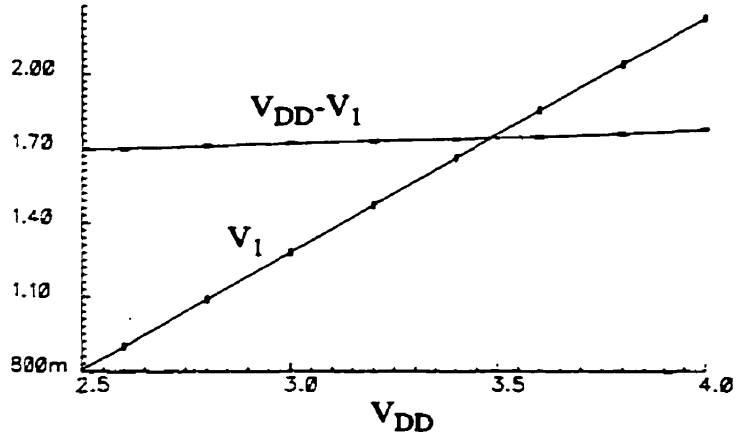


Fig. 5.6. Bias voltage versus supply variation

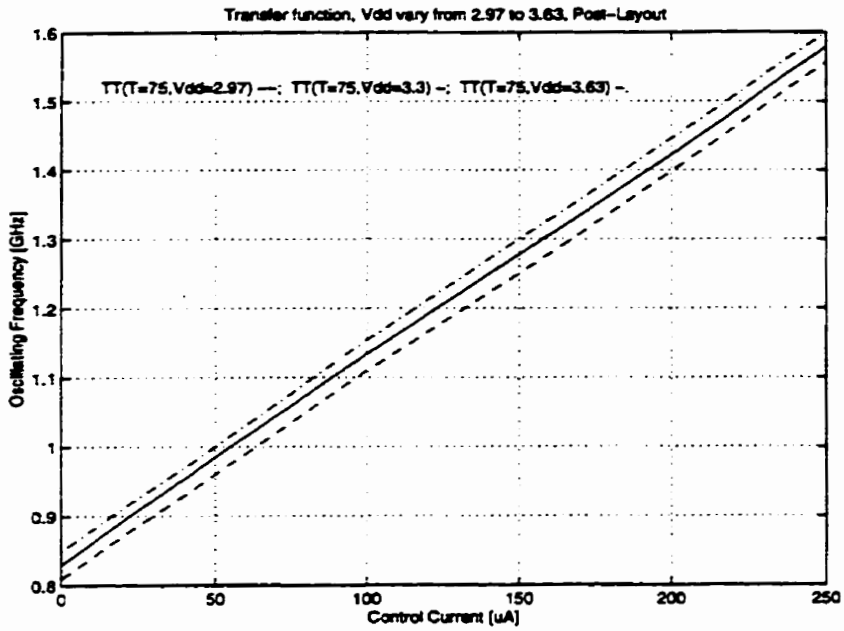


Fig. 5.7. Oscillation frequency as function of control current with power supply voltage as parameter (with compensation)

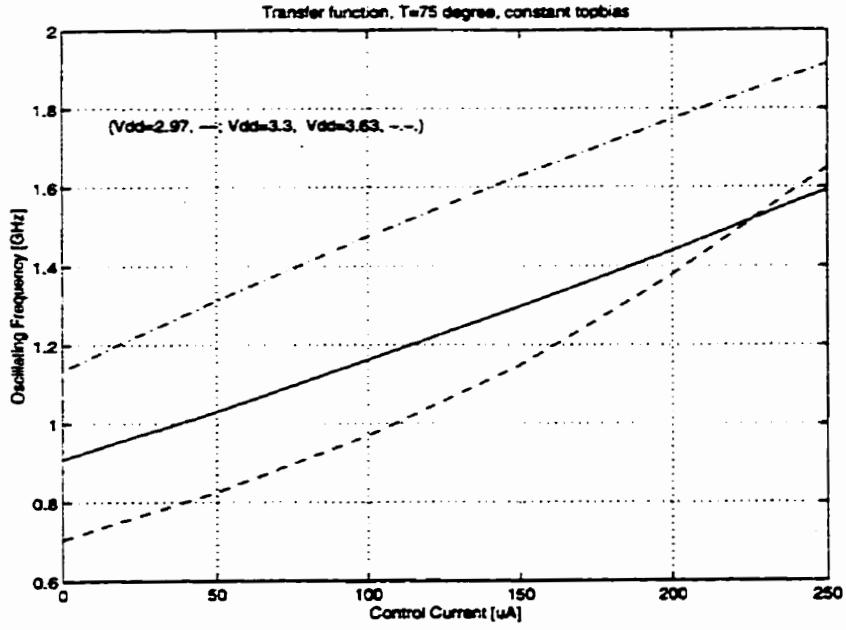


Fig. 5.8. Oscillation frequency as function of control current with power supply voltage as parameter (constant voltage biasing without compensation)

5.2.1.3 Output Buffer

The output buffer is shown in Fig. 5.9. It consists of a differential pair preamplifer and a differential to single-ended converter. Two inverter stages consisting of M_1-M_4 are added to provide sufficient driving capability. The circuit results in a rail-to-rail voltage swing which is expected by the following frequency dividers.

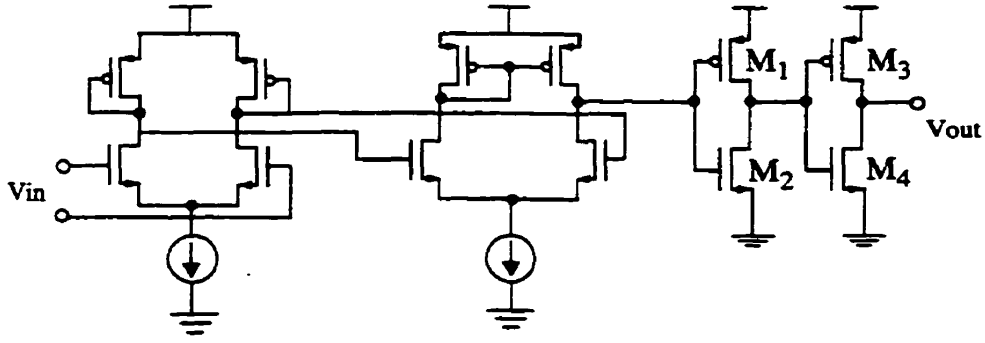


Fig. 5.9. Output buffer

5.2.1.4 Voltage to Current Converter

Voltage to the current converter is used to convert the output voltage on the loop filter into a current that is used to tune the ring oscillator (ICO) [YGW92][JoMa97]. The simplified voltage to current converter is shown in Fig. 5.10. The high gain of the opamp guarantees that its differential input voltage is very small, and, therefore, the voltage across the resistor R is very closely equal to V_{cont}. Thus, the current through R is $I_R = V_{cont}/R$. This current is mirrored by the transistor M_2. The dynamic range of output from the charge pump and loop filter is from 0.5 V to 2.7 V. This voltage needs to be transferred to the ICO input control current from 0 to 250 μA to achieve a large tuning range (800 MHz to 1.6 GHz) with a centre frequency at 1.25 GHz. The R value (5 kΩ) combined with the ICO gain

(K_{ICO} in unit of MHz/mA) results in the sensitivity of the VCO (K_{VCO} in units of MHz/V). If transistors M_1 and M_2 have different sizes, we have

$$K_{VCO} = \frac{K_{ICO}}{R}\left(\frac{W_2}{W_1}\right) \tag{5.7}$$

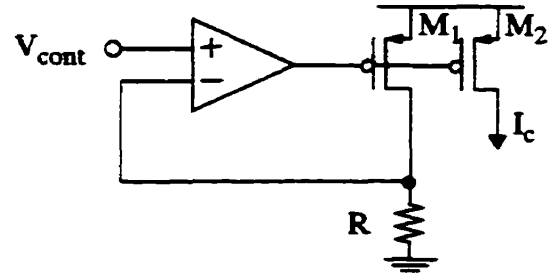


Fig. 5.10. Simplified voltage to current converter

5.2.2 Phase and Frequency Detectors

Selection of the type of phase/frequency detector is an important step in a PLL design. PLL frequency synthesizers and clock generators require phase detectors to have wide phase detection range, good linearity, low power dissipation and small size for integration. An ideal phase detector produces an output signal, whose dc value is linearly proportional to the difference in the phases of two input signals,

$$\overline{V_{out}} = K_d(\theta_1 - \theta_2) \tag{5.8}$$

This particular ideal transfer function is difficult to implement in practice, and a variety of circuit architectures have been developed to approximate it, such as the Gilbert multiplier, exclusive OR (*XOR*) phase detector, two-state phase detector, three-state phase detector, Z-state phase detector and sample-and-hold phase detector [Wol91].

The Gilbert multiplier can not be used as a frequency detector since the average output is zero for $\omega_1 \neq \omega_2$. As well, K_d is a function of input signal amplitudes, an undesirable attribute because a PLL employing such a phase detector exhibits amplitude-dependent static and dynamic behavior. If the input signal amplitudes are large enough that all three differential pairs experience full switching, then the circuit operates as an *exclusive OR (XOR)* gate. Since the output of the *XOR* PD is averaged, noise injected into the data stream (a false bit) can be rejected. Thus, the *XOR* PD can be used in the clock recovery circuit. The disadvantage of using the *XOR* PD is that the PLL can lock on harmonics of the data (the average of the PD output amplitude for $2f_i$ and $0.5f_i$ components is essentially same). So the VCO operating frequency range should be limited to frequencies much less than $2f_i$ and much greater than $0.5f_i$, where f_i is the nominal clock frequency for proper lock with a *XOR* PD. Furthermore, the average output of the *XOR* PD depends on the duty cycle of the input.

Two-state PD and three-state PD belong to so-called *edge-triggered sequential phase detectors* [Wol91]. Since the circuits change state only on one edge of the inputs, their characteristics differ from those of an XOR; their average output does not depend on the input duty cycle, and the outputs remain low when the loop is locked, eliminating ripple on the output of the loop filter. However, one disadvantage of two-state PD and three-state PD is that the output high frequency component is at f_i rather than at $2f_i$ for the XOR PD. Thus, narrower loop bandwidth is required to suppress the clock frequency feed through and spurious modulation. Another disadvantage is that they are more sensitive to noise than the XOR PD. This is because the flip-flops remember an error due to noise, while the XOR is memoryless. A three-state PD can be used only with strictly periodic signals (e.g., in frequency synthesizers and clock generators). If there are any missing pulses, as in clock recovery applications or high-noise applications, then the three-state PD will not operate properly.

The three-state PD can be used as both a phase and frequency detector (PFD) which proves extremely useful because it significantly increases the acquisition range, lock speed of PLLs and is free from false locking to the second or third harmonics. The implementation of the PFD is shown in Fig. 5.11. The circuit consists of two edge-triggered, resettable D flipflops (DFF) with their D inputs connected to logical "1". The reference signal "Ref" and local oscillator signal "Osc" act as clock inputs of DFFa and DFFb, respectively. If the rising edge of the "Ref" leads the "Osc" rising edge, the "UP" output of the PFD has a width corresponding to the time difference between two leading edges, while the "DN" output remains low. This causes the oscillator frequency to increase, having the effect of moving the edges closer together. In lock, both the "UP" and "DN" pulse are coincident and have a designed minimum width given by the total delay through the AND gate and the reset path of the DFFs. Fig. 5.12 shows the ideal input-output transfer characteristic of the PFD.

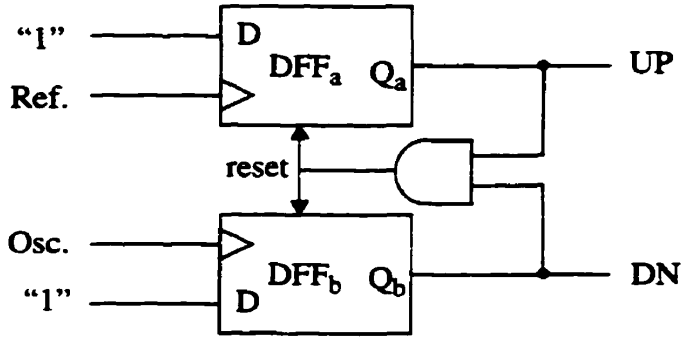


Fig. 5.11. The three-state PD used as *PFD*

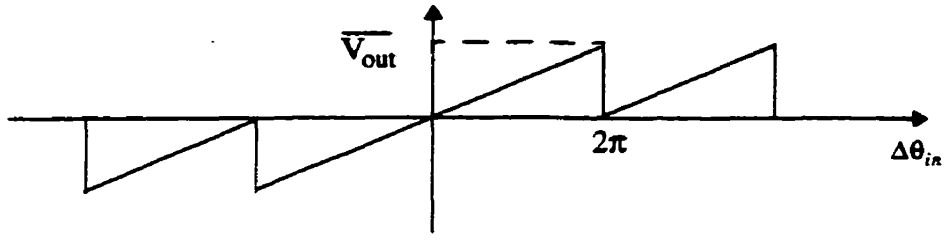


Fig. 5.12. PFD transfer characteristic

The transfer characteristics of a PFD practical implementation can potentially suffer from "dead zone". The dead zone is a region where the magnitude of the PFD DC output sticks at a fixed value or gain (K_d) drops from its regular value. If the input phase difference is within the dead zone, the DC output does not change sufficiently to correct the resulting error and a peak-to-peak jitter approximately equal to the width of the dead zone can arise in the VCO output. The dead zone occurs when Q_a and Q_b do not have a sufficient length of time to be simultaneously high (Fig. 5.11). In order to eliminate the dead zone associated with the three-state PFD, an extra delay can be inserted in the reset path with the use of an inverter chain. This creates minimum width of UP/DN pulses when the input signals are in phase. The net charge added to the loop filter by the charge pump is zero due to the equal width of the pulses. In practical implementation, the pulse width of "UP" and "DN" should be short to minimize the perturbation of the loop filter voltage due to mismatch of current magnitude while long enough to eliminate dead-zero. To achieve high speed and low power consumption DFFs can be implemented using dynamic circuits.

5.2.3 Charge Pumps

Charge pumps and loop filters are utilized to convert the timed output logic levels from digital style PDs or PFDs into analog quantities for controlling the VCO [Gard80]. The combination of a PFD and a charge pump offers two important advantages over the XOR/

LF approach: 1) the capture range is only limited by the VCO output frequency range; 2) the static phase error is zero if mismatches and offsets are negligible.

The simplified charge pump circuit diagram is shown in Fig. 5.13. The digital signals UP, DN and their complements switch current sources I_{up} and I_{dn} onto node V_{cont}, thus delivering a charge to move Vcont up or down. I_{up} and I_{dn} need to be equal. The minimum charge pump current is limited by the switching speed requirement. When nodes A and B are not switched to V_{cont} they are biased by the unity-gain amplifier [YGW92]. This suppresses any charge sharing from the parasitic capacitance on A or B that can cause mismatch between the two current sources. Once the loop is locked, the charge pump will only need to deliver extremely narrow output current pulses to correct for voltage drop in the loop filter due to leakage.

The proper design of the charge-pump is a key to obtaining low jitter with an on-chip filter. Output glitch energy needs to be minimized. Current sources I_{up} and I_{dn} need to be well matched and controlled over supply, temperature and process variations since they determine the loop transfer and noise characteristic. Current sources and switch turn-on time mismatch results in residual energy at f_{ref} and harmonics. It also generates a static phase error. All the transistors in the current sources are usually chosen relatively wide for better matching and have long channels to minimize short channel effects and maximize output impedance. High output impedance allows the transistors in the current mirrors to operate as ideal current sources when biased in the saturation region.

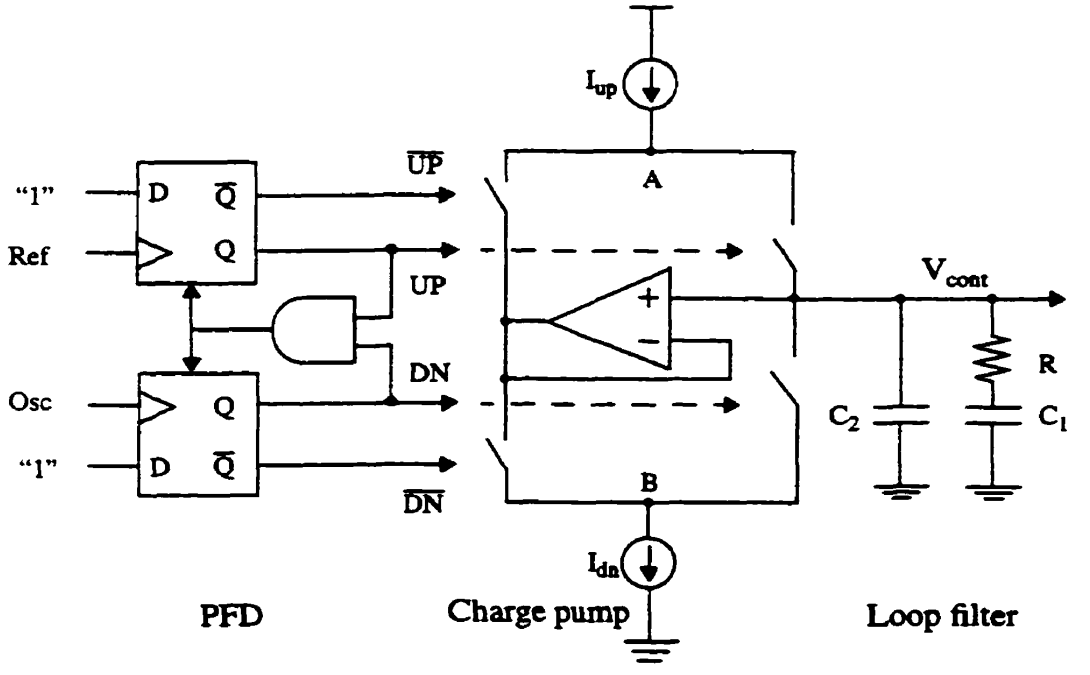


Fig. 5.13. Simplified charge pump circuit connected with PFD and loop filter

5.2.4 The Loop Filter

The loop filters differ from simple first order passive RC networks to complex high order structures. Design considerations include close-loop bandwidth, dynamic response, stability, frequency acquisition range and spurious modulation suppression. The existence of ripple at the VCO input places limits on the application of the simple first-order filter. A higher order loop filter improves for AC filtering, but it increases the circuit design complexity and can possibly cause instability of the PLL. A second order charge pump loop filter is shown in Fig. 5.13 which is a passive phase-lead filter driven by a charge pump. The resistor, R, has been included to realize a zero in the low-pass filter's transfer function. Capacitor C_2 is used to filter out high frequency spikes from the charge pump.

The transfer function of the loop filter in Fig. 5.13 can be represented as

$$F(s) = \frac{V_{LF}}{I_{ch}} = K_h \cdot \frac{(s + \omega_z)}{s(s/\omega_p + 1)} \tag{5.9}$$

where $K_h = R$, $\omega_z = \frac{1}{RC_1}$ and $\omega_p = \frac{1}{RC_2}$

By increasing the loop bandwidth of the PLL, the loop will be able to track the reference clock faster and correct VCO phase noise more significantly. To increase the bandwidth, minimizing C_2 is required. However C_2 can not be eliminated completely because some of the C_2 capacitance is due to parasitic capacitance from metal wiring and resistor R.

5.2.5 Frequency Prescaler/Dividers

The prescaler/dividers are used to divide the VCO output frequency by an integer N (16/64) for this clock generator. Dividers are generally designed as digital counters which are classified as sequential circuits. Fig. 5.14 shows the block diagram of a synchronous divider (Johnson counter with division ratio $2N$) and an asynchronous divider (ripple counter with division ratio 2^N). For the asynchronous divider, each DFF of this divider has its inverted output connected back to the input, forming a divide-by-2 circuit (Toggle flip-flop). The non-inverting output is used as clock input of the next flip-flop. These asynchronous dividers can reach very high frequencies because only one element, the first flip-flop in the chain, operates at maximum frequency and no external logic circuit is required for such a divide by two operation.

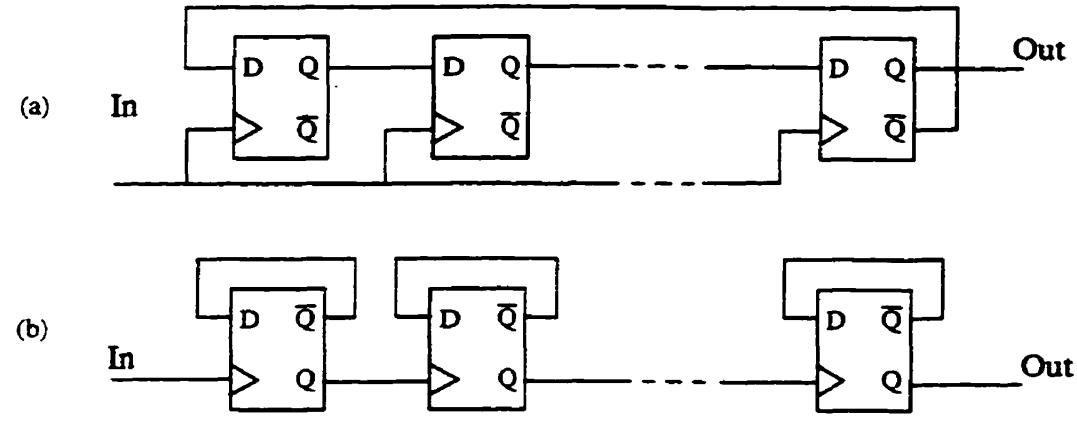


Fig. 5.14. Circuit diagram of (a) a synchronous divider and (b) an asynchronous divider

The DFF circuits can be constructed either with static or dynamic circuits. Static circuits are more robust and provide broadband operation but can not operate at a very high frequency. In contrast, dynamic circuits can operate at higher speed but work only in a limited range of frequencies. Many types of dynamic flip-flops have been proposed [YKS87] [YuSv89] [RFHF93] [RHP94] [FoKw95]. The True Single Phase Clock (TSPC) DFF was used as the prescaler for this clock generator application (Fig. 5.15). Since it operates at high VCO output frequency, its design is quite critical. The transistor sizes have been optimized to achieve high speed. Table 5.1 lists the post-layout simulation results with sinusoidal input in a 0.35 μm CMOS technology. The frequency operating range of the prescaler is from 400 MHz to 3 GHz with power consumption of 6.6 mW at maximum frequency. The minimum operating frequency depends on process leakage specification. The divide by 8/32 divider utilizes dynamic flip-flops which are connected as a ripple counter. Since at lower frequencies the precharged nodes tend to lose their charge due to leakage current, a feedback transistor can be used to keep the output node high while another transistor is added to eliminate glitches normally occurring in this circuit (Fig. 5.16) [RHP94].

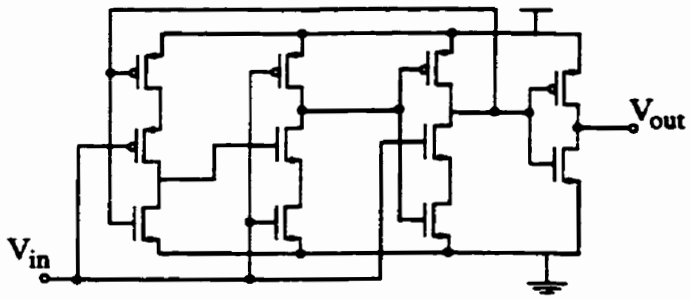


Fig. 5.15. TSPC frequency prescaler (divided by 2)

Table 5.1 Post-layout simulation results of the prescaler (0.35 μm CMOS)

Input frequency	Power consumption
3 GHz (max)	6.6 mW
1250 MHz	3 mW
400 MHz (min.)	1.86 mW

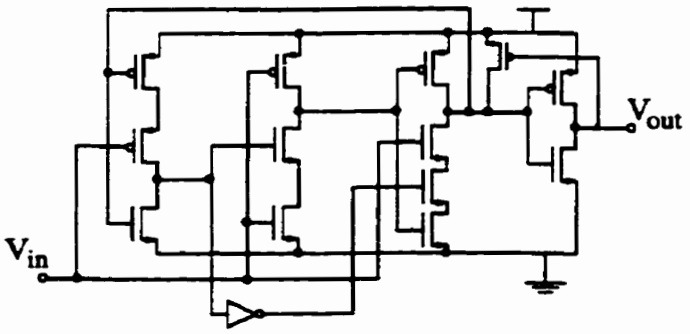


Fig. 5.16. Dynamic Flip-Flop with improved low frequency behaviour

5.3 Analysis of Phase-Locked Loops

Because of its switching operation, the charge-pump PLL is a discrete-time system. Simple transfer function analysis is not directly applicable to a nonlinear, time-varying system. However, when loop bandwidth is small compared to the input frequency, the state of the PLL changes by only a very small amount on each cycle of the input frequency. We are not concerned about the detailed behaviour within a single cycle but more interested in average behaviour over many cycles. By applying an average analysis, the time-varying operation can be simplified to time-invariant and the powerful tool of transfer functions can be used [Gard79].

5.3.1 PLL Frequency Response

In order to analyse PLL approximately with a linearized time-invariant system, the following assumptions are made: (a) same average charge flowing into the low-pass filter for both linear and non-linear systems; (b) the phase of the input and VCO output frequency changes little in any period; (c) loop bandwidth is smaller than one tenth of any digital activity within the loop. With these assumptions, a linearized continuous-time, small-signal model for PLL is given in Fig. 5.17.

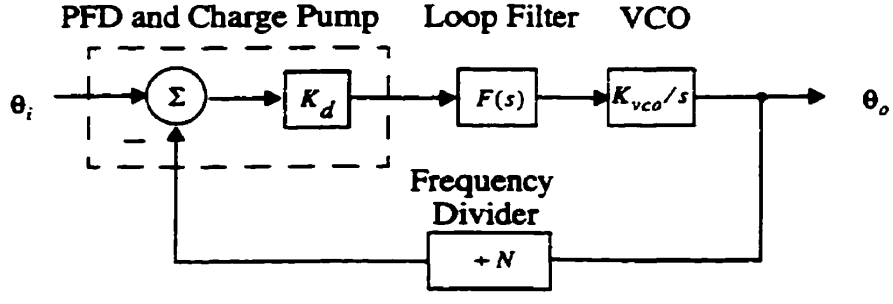


Fig. 5.17. Linearized continuous-time, small phase error model of PLL

With the closed-loop phase transfer function (θ_o/θ_i) represented by $H(s)$, we have,

$$H(s) = \frac{K_d K_{vco} F(s)/s}{1 + K_d K_{vco} F(s)/(Ns)} = \frac{NG(s)}{1 + G(s)} \tag{5.10}$$

where $G(s)$ is the open loop transfer function from the phase detector input to the frequency divider output,

$$G(s) = \frac{K_d K_{vco} F(s)}{Ns} \tag{5.11}$$

K_{vco} is the VCO sensitivity (or gain) with unit of rad/sec/volt, and N is the divider ratio. The combined transfer function (K_d) of the PFD and charge pump can be represented as

$$K_d = \frac{I_{avg}}{\Delta\theta_{in}} = \frac{I_{ch}}{2\pi} \tag{5.12}$$

where I_{avg} is the corresponding average error current for input error phase $\Delta\theta_{in}$, and I_{ch} is the charging/discharging current from the charge pump. Substituting Eq. (5.9) and Eq. (5.12) into Eq. (5.10) and Eq. (5.11), respectively, we have the open-loop transfer function,

$$G(s) = \frac{K(s + \omega_z)}{s^2(s/\omega_p + 1)} \tag{5.13}$$

and the close-loop transfer function,

$$H(s) = \frac{NK(s + \omega_z)}{s^3/\omega_p + s^2 + Ks + K\omega_z} \tag{5.14}$$

where

$$K = \frac{I_{ch} K_{vco} K_h}{2\pi N} \tag{5.15}$$

Since the close loop transfer function has a denominator of the third order and there

are two poles at the origin for the open-loop transfer function, The PLL is usually referred to as a type II third-order system [Gard79]. However, since $C_2 \ll C_1$, the pole ω_p has only high frequency effects on the PLL. Low frequency properties should be essentially the same as for the second-order loop. The PLL bandwidth (BW) can be found from $|G(s)| = 1$ as

$$BW \approx K = \frac{I_{ch} K_{vco} K_h}{2\pi N} \tag{5.16}$$

Stability requires that all the closed-loop poles be located in the left half of the s plane. The easiest way to analyze loop stability is to plot the magnitude and phase of the open-loop transfer function versus frequency [SeSm91][Smi86]. The phase margin is

$$\begin{aligned} \phi_M &= 180^o + \arg G(j\omega_c) \\ &= \arg\left[\frac{K(j\omega_c + \omega_z)}{\omega_c^2 (j\omega_c/\omega_p + 1)}\right] \end{aligned} \tag{5.17}$$

where ω_c ($=2\pi K$) is the open-loop crossover frequency at which the open-loop gain is unity.

The greater the phase margin, the more stable the system and the more phase lag from parasitic effects can be tolerated. Additional phase lag is due to neglected parasitic poles or from the time delay arising in the phase detector.

From Eq. (5.17), we know that a smaller ω_z makes the system more stable. However, this requires a large capacitance value of C_1. A large capacitor value also takes large chip area and longer time to charge/discharge during lock acquisition. If peaking in frequency response (overshooting in the time domain) is not critical for the application, a good compromise is to make $\omega_z = K/4$ (when $\omega_z < K/4$, the PLL is overdamped; when $\omega_z > K/4$, the PLL is underdamped [Wol91]). This assures fast acquisition. If peaking is more of concern, a smaller ω_z should be selected to limit the peaking to some small value.

The choice of ω_p needs to consider the stability of the PLL as well as high frequency component suppression. The jitter due to high frequency spurious modulation can be reduced by making ω_p as small as possible. However, the pole at ω_p adds excess phase lag, which reduces the loop phase margin, and possibly causes ringing in the transient response. Thus, for stability reasons, a large ω_p needs to be chosen. A good compromise is to keep $\omega_p \geq 4K$ [Gard79].

PLL loop bandwidth influences the stability, pull-in time and the suppression of noise from the VCO and high frequency spurious modulation. In order to suppress the VCO noise, the loop was designed to have a large bandwidth (2 MHz). I_{ch} was chosen to be 20μA based on practical considerations of power consumption and speed. The gain of VCO is 272 MHz/V. The chosen loop filter parameters are K_h of 40 kΩ, C_1 of 242 pF. In order to have a large ω_p, C_2 is minimized with the use of distributed capacitance of the resistor (R), parasitic capacitance of metal wiring and gate capacitance. It has a total value of 686 fF. The zero and pole frequencies of the loop filter are located at 16.4 kHz and 5.8 MHz, respectively. The simulated responses of $|G(j\omega)|$, $|H(j\omega)|$ and $\arg G(j\omega)$ are plotted in Fig. 5.18 and Fig. 5.19 using extracted post layout parameters for N=16 and 64, respectively. Table 5.2 summaries the simulated loop performance. For N=16, the loop bandwidth is 2037 MHz with transfer function peaking of 0.06 dB. The phase margin (PM) is 70 degrees indicating good stability condition. It should be noted the nonlinearites and parasitic poles (e.g., input capacitance of VCO) would cause some degradation of the phase margin.

Table 5.2 Simulated loop performance

N	BW (kHz)	PM (deg)	Peaking (dB)
16	2037.2	70.2	0.06
64	537.58	83.0	0.22

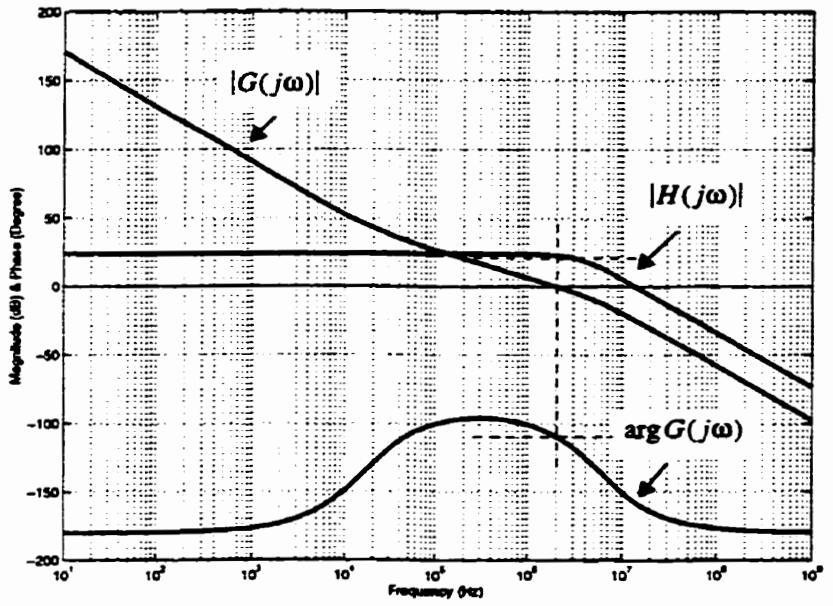


Fig. 5.18. Closed and open loop response for N=16

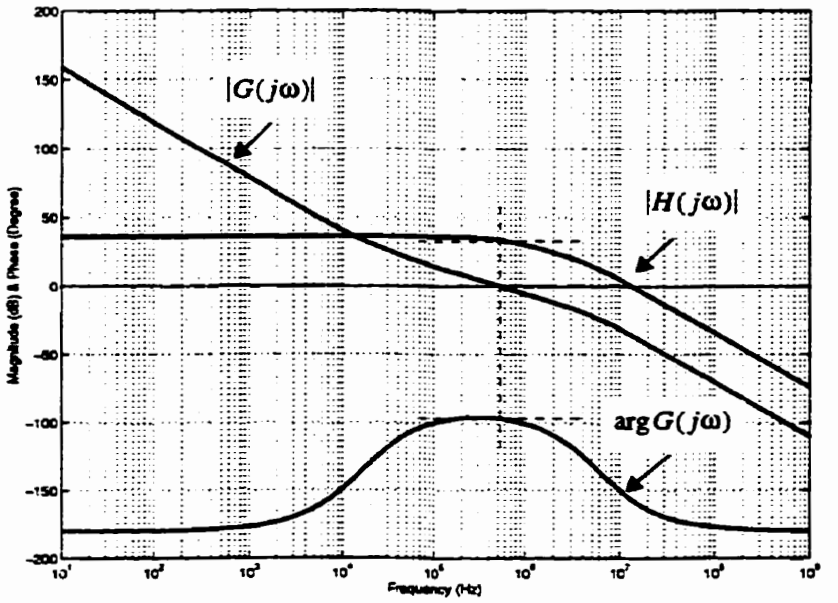


Fig. 5.19. Closed and open loop response for N=64

5.3.2 Lock Acquisition

The small-signal assumption and linearized system model fail for large phase errors which occur during the acquisition of lock. Thus, transistor level time domain analysis was performed for loop capture behaviour analysis. The simulation time steps are chosen to be less than the smallest time constant of the VCO (10 ps). The total length of simulation time must be greater than largest time constant of the low-pass filter (10 μs). The simulation was run on an ULTRA1 Spar Sun-station with HSPICE for about 3 days. Fig. 5.20 illustrates the simulated acquisition behaviour of the 1.25 GHz PLL. The upper curve corresponds to the control voltage of the VCO as a function of time. The lower curve is the voltage on the loop capacitor C_1. Loop locking is achieved if two curves approach to each other at a designed static control voltage.

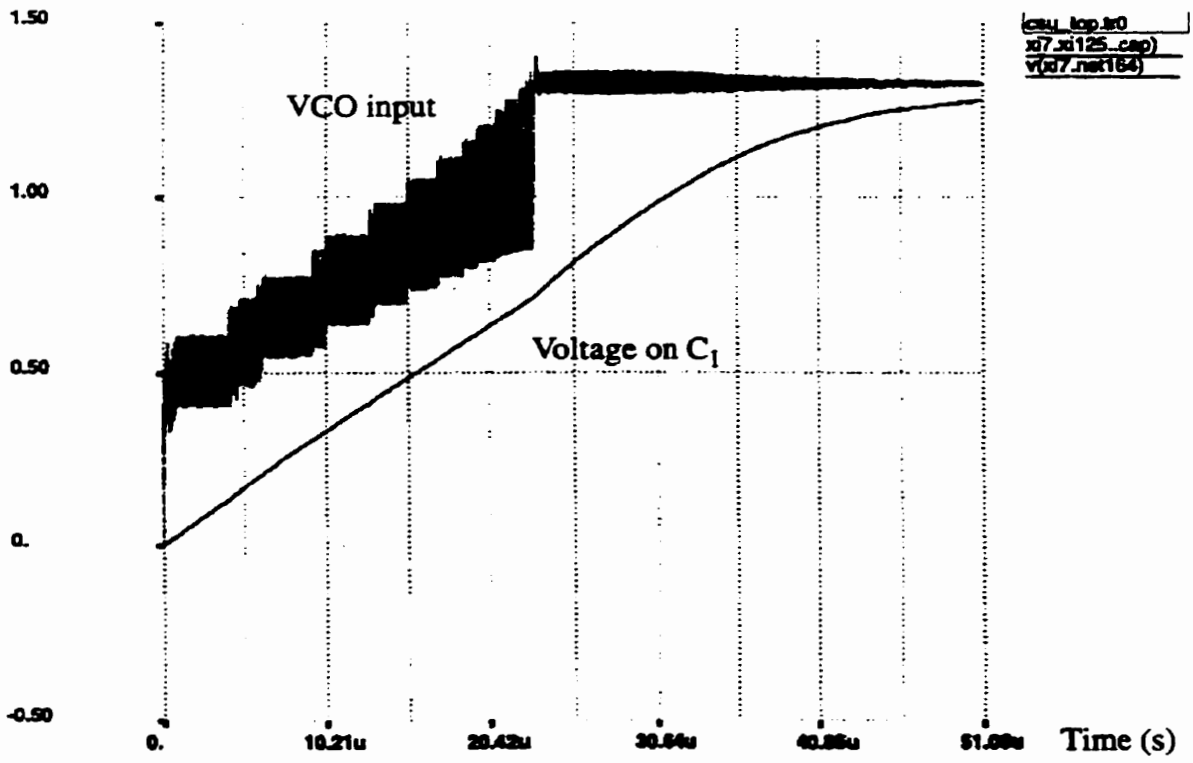


Fig. 5.20. Simulated PLL acquisition behaviour.

For a 3-state PFD PLL, the pull-in time can be found as [Wol91]

$$T_p = \frac{\omega_{eo}/K - 2\pi N}{\pi N \omega_z} \tag{5.18}$$

where ω_{eo} is the initial frequency error of the VCO.

For a 450 MHz initial frequency error, the calculated pull-in time is 23 μs which is close to the time domain simulation results (26 μs) for this 1.25 GHz clock generator.

5.4 Noise in Phase-Locked Loops

5.4.1 PLL Phase Noise due to the Additive Noise

In a practical PLL, all the loop components contribute noise to the output. Digital phase detectors that were evaluated in the frequency range of 0.1 to 1.0 MHz exhibit a phase noise floor of $S_\varphi(f) = 10^{-10.6 \pm 0.3}/f$ [Krou82]. ECL and CMOS logic families were found to exhibit better phase noise performance by up to 22 dB in the flicker noise region. In a passive loop filter, noise is contributed by its components: capacitors and resistors. Since depletion and diffusion type capacitors depend on fluctuation of applied voltage or current respectively, the pn junction structure should be avoided for low phase noise. Resistors produce thermal noise proportional to their value, $4kTR$. (e.g. for R=40 kΩ, we have $S_R(f) = 6.6 \cdot 10^{-16}$ (V^2/Hz) at 27°C). Thus large value resistor should be avoided.

The phase noise of a monolithic CMOS ring oscillator was discussed in Chapter 4. Since VCO requires a buffering circuit to drive a large load and avoid frequency pulling, this buffer amplifier introduces additional phase noise to the VCO in the PLL. The noise performance of a high frequency buffer can be characterized by its Noise Figure (NF). A high noise figure in the buffer increases the noise floor of the VCO in the PLL. Phase noise

levels at the input to an ideal digital divider of ratio N are reduced by $20 \cdot \log N$ at the divider output. For a large division ratio, the phase noise floor of the last divider determines the overall divider performance.

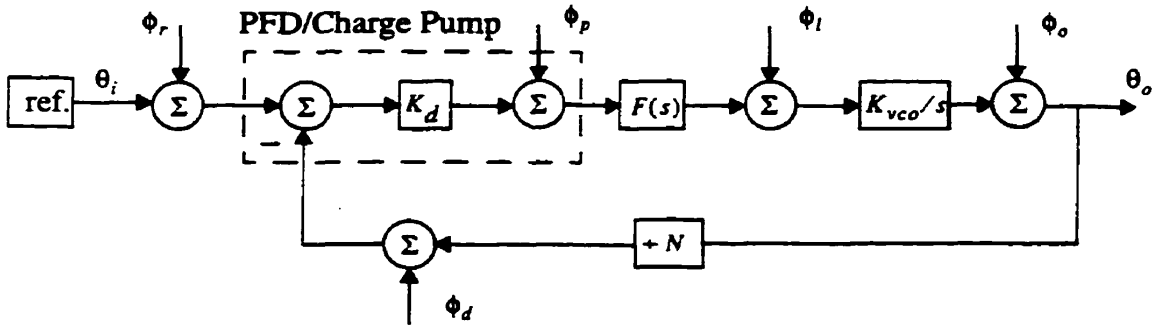


Fig. 5.21. A PLL including five additive noise sources

Fig. 5.21 shows a linearized model of a PLL with five additive noise sources. ϕ_r represents the noise on the reference signal; ϕ_p is the noise created in the phase detector and charge pump; ϕ_d is the noise due to frequency divider; ϕ_l is the noise from loop filter; ϕ_o is the noise from VCO. Since all noise sources are non-coherent and random, the total noise of the closed-loop system at the VCO output is given by adding respective spectral densities,

$$\begin{aligned} S_{\phi_T} &= \left|\frac{NG(s)}{1+G(s)}\right|^2 \cdot (S_{\phi_r} + S_{\phi_d}) + \left|\frac{K_{vco}F(s)/s}{1+G(s)}\right|^2 \cdot S_{\phi_p} + \left|\frac{K_{vco}/s}{1+G(s)}\right|^2 \cdot S_{\phi_l} + \left|\frac{1}{1+G(s)}\right|^2 \cdot S_{\phi_o} \\ &= \left|\frac{NG(s)}{1+G(s)}\right|^2 \cdot \left(S_{\phi_r} + S_{\phi_d} + \frac{1}{K_d^2} \cdot S_{\phi_p} + \frac{1}{|K_d F(s)|^2} \cdot S_{\phi_l}\right) + \left|\frac{1}{1+G(s)}\right|^2 \cdot S_{\phi_o} \end{aligned} \tag{5.19}$$

where $G(s)$ is the open loop gain as defined in Eq. (5.11).

From Eq. (5.19), we know that the noise power of all terms is amplified by the factor N^2 within the loop bandwidth. e.g., corresponding to N=16 and 64, the input reference's phase noise is increased by $(20 \cdot \log N)$ 24 dB and 36 dB, respectively. Thus in order to re-

duce phase noise, a large division ratio should be avoided. Since noise from the PFD, charge pump and loop filter is divided by phase detector/charge pump gain K_d, the output phase noise can be reduced by increasing K_d, while preserving the desired loop forward gain.

Eq. (5.19) also indicates that the PLL functions as a low-pass filter for phase noise arising on the reference signal, phase detector, divider and loop filter. In order to minimize these noises, the loop bandwidth must be as small as possible, although it slows down locking, limits the capture range, and degrades the stability. The PLL functions as a high-pass filter for phase noise originating in the VCO. The output signal from the VCO is mixed by the phase detector to the baseband when the PLL is in-lock. The phase noise components which lie close to the loop center frequency will fall within the loop filter bandwidth and the resulting error signal at the filter output will act to suppress these noise components. Phase noise components in the oscillator output which are at a frequency sufficiently far away from the center frequency will lie outside the loop filter bandwidth. No error signal will correct for these fluctuations in frequency. Therefore, phase noise in the oscillator output which lies outside the loop bandwidth is unaffected by the operation of the PLL.

In monolithic CMOS implementations, the phase noise of the VCO is typically much more significant than that of other loop component. If only noise from the VCO is considered, the output phase noise within the loop bandwidth ($f < K$) is

$$S_{\phi_r} \approx \frac{1}{|G(s)|^2} \cdot S_{\phi_o} = \left| \frac{Ns}{K_d K_{vco} F(s)} \right|^2 \cdot S_{\phi_o} \tag{5.20}$$

Substituting (5.9) into Eq. (5.20), we have

$$S_{\phi_T} = \left|\frac{s^2(s/\omega_p + 1)}{K(s+\omega_z)}\right|^2 \cdot S_{\phi_o} = \begin{cases} \frac{s^4}{(K\omega_z)^2} \cdot S_{\phi_o} & f < f_z \\ \frac{s^2}{K^2} \cdot S_{\phi_o} & f_z < f < K \end{cases} \quad (5.21)$$

The output noise due to the VCO is minimized by having the loop bandwidth as wide as possible, a requirement in conflict with the case where the PLL input, phase detector and divider create noise. In frequency/clock synthesizer applications where the reference is derived from a crystal oscillator, the loop bandwidth can be increased to reduce both the VCO phase noise and lock time. However, stability considerations limit the loop bandwidth to approximate $f_{ref}/10$ [Gard79].

The VCO noise transfer function (S_{ϕ_T}/S_{ϕ_o}) within the loop bandwidth is approximately equal to $-20 \cdot \log|G(s)|$ dB, shown in Fig. 5.18 and Fig. 5.19 (with the opposite sign) for N=16 and 64, respectively. If the phase noise of the free running oscillator is -100 dBc/Hz at 1MHz offset frequency, the PLL output phase noise due to VCO is -106 dBc/Hz for N=16.

5.4.2 PLL Jitter due to the Spurious Signal Modulation

The proper design of the charge-pump is critical to obtaining low jitter with an on-chip loop filter. Output glitch from the charge-pump and PFD output high frequency harmonics can generate periodic disturbance on the VCO control line. This effect is similar to frequency modulation as we analysed in Section 4.4.2. The period disturbance at the VCO input creates sidebands at an offset equal to $\pm f_{ref}$, requiring further limitation of the loop-filter bandwidth so that the magnitude of these sidebands is sufficiently small.

Assuming this ripple is a small sinusoidal perturbation $\Delta V_r(t) = V_m \cos\omega_m t$, the frequency deviation at the VCO output is,

$$\Delta f_0(t) = K_{VCO} \cdot \Delta V_r(t) = K_{VCO} \cdot V_m \cos\omega_m t \tag{5.22}$$

The deviation of the period from the center frequency is

$$\Delta T(t) = \frac{\Delta f_0(t)}{f_0^2} = \frac{K_{VCO} V_m}{f_0^2} \cos\omega_m t \tag{5.23}$$

The timing jitter rms value due to the single frequency modulation can be found [HeRa98] as

$$\sigma = \frac{K_{VCO} V_m \omega_m}{\sqrt{2} \cdot f_0^3} \tag{5.24}$$

Assuming that $K_{VCO} = 272MHz/V$, $f_0 = 1.25GHz$, $f_m = 77.76MHz$, and the rms jitter value $\sigma = 9.6ps$, from Eq. (5.24) the perturbation amplitude (V_m) can be calculated as 200 mV.

In order to reduce the timing jitter due to the spurious modulation, the gain (or sensitivity) of VCO can be purposely made low. However, the resulting reduction of the loop bandwidth and frequency control range usually requires additional circuitry for compensation (such as, a coarse control of the center frequency).

5.5 Implementation and Measurement Results

The PLL clock generator was implemented monolithically in a 0.35 μm single poly, three metal CMOS technology. The layout was divided into four separated blocks: (1) ICO/ prescaler and output interface; (2) PFD and dividers; (3) charge pump; (4) loop filter and V-to-I converter. The second and third blocks were provided by PMC-Sierra, Inc. The first block uses two pairs of supply and ground pins for its digital and analog circuits, respectively. Each of the other three blocks uses a pair of supply and ground pins. Separation of

each functional block makes it easy to debug and characterize the performance of each building block. The design also incorporates a dual bi-directional analog test bus to probe critical nodes inside the PLL for testing purposes. All building blocks are separated by both p+ and n well guarding rings to reduce inter-block interference. The core ICO layout was made as compact as possible. Devices with a large width are divided into the connection of parallel smaller MOSFETs. To compensate for the edge effects, dummy elements are added to a common-centroid layout to ensure that the matched transistors see the same adjacent structures. Substrate contacts are placed close to the critical devices in the high frequency path.

Fig. 5.22 shows the die photo of PLL clock generator. By varying the input reference frequency, the ICO (in PLL) locking range and transfer characteristic were measured (Fig. 5.23). The gain of the ICO is exceptionally linear and slightly higher than predicted. The measured output spectrum and jitter histogram of PLL at 1.25 GHz is illustrated in Fig. 5.24 and Fig. 5.25, respectively. Table 5.3 summarizes the measurement results.

Table 5.3 Summary of measured PLL clock generator performance

Locking range	880-1648 MHz
Output jitter	11 ps (rms), 80 ps (P-P)
Operating voltage	2.96 to 3.63 V
Power consumption	109 mW
Chip active area	1 mm by 1 mm

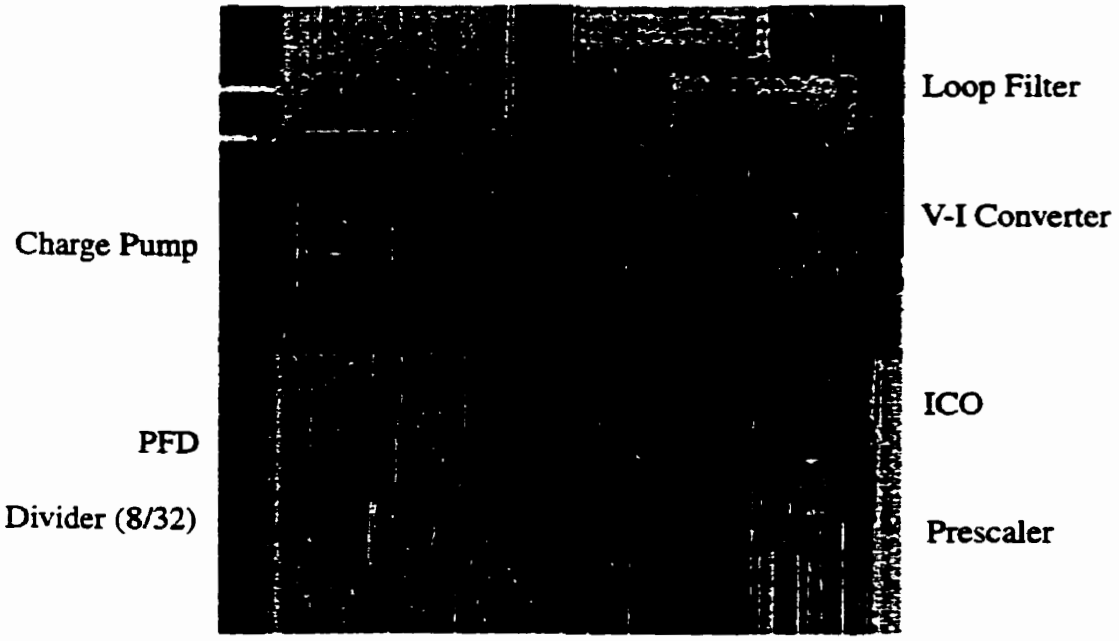


Fig. 5.22. Die photograph of the PLL clock generator

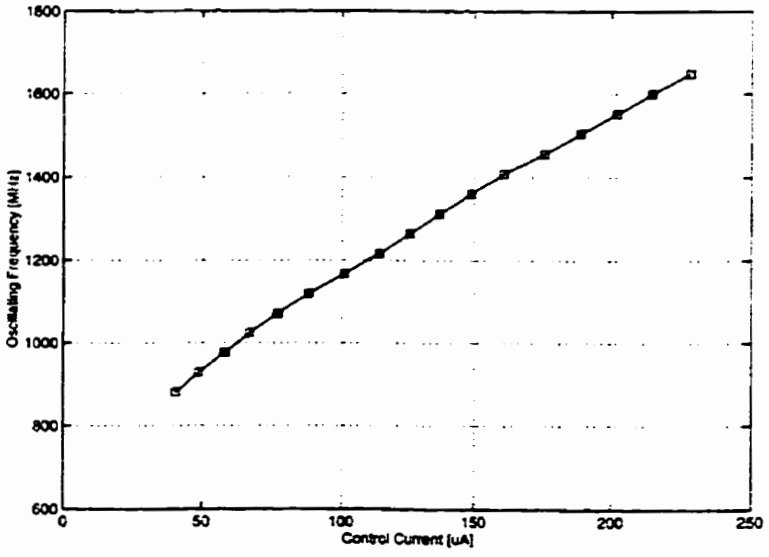


Fig. 5.23. Measured results of the ICO (in PLL) transfer characteristic

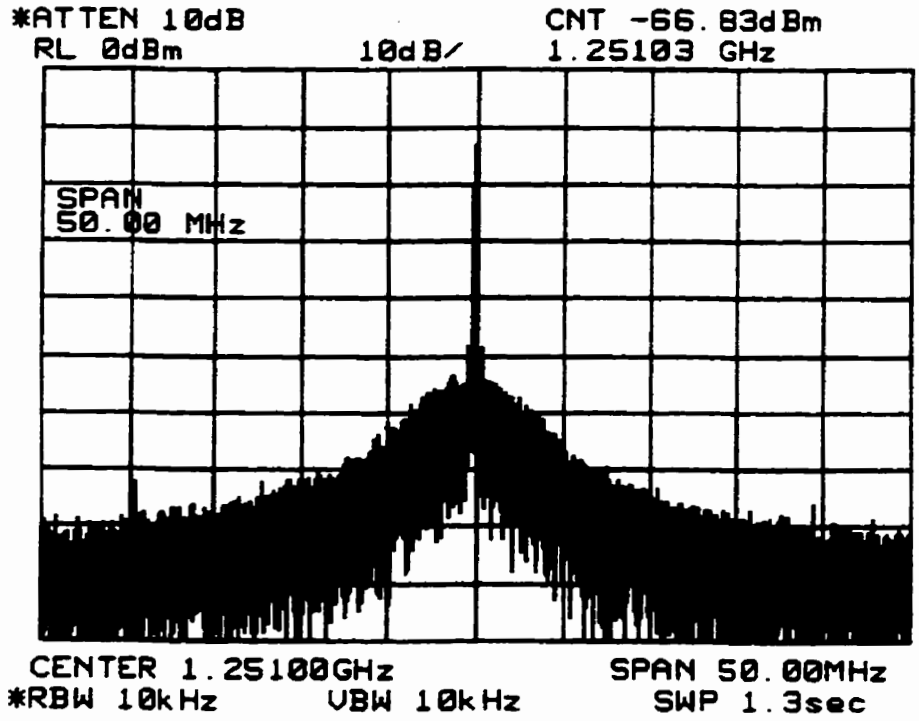


Fig. 5.24. Measured output spectrum of the PLL at 1.25 GHz

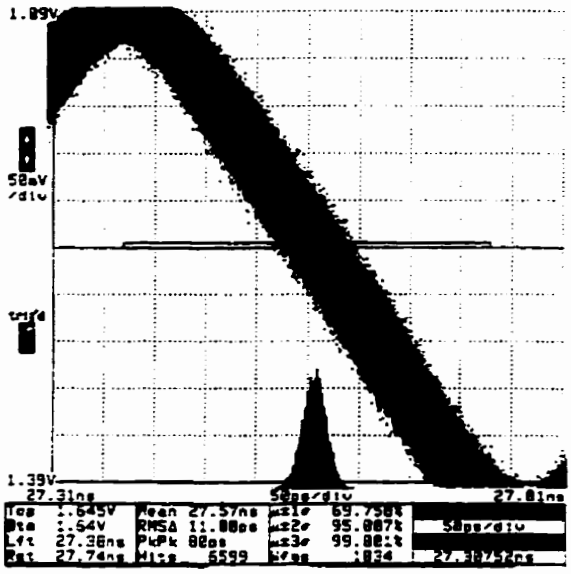


Fig. 5.25. PLL jitter histogram

5.6 Summary

A 1.25GHz monolithic CMOS PLL clock generator unit was designed for data communications. The monolithic PLL consists of a ring oscillator, divider, phase/frequency detector, charge pump and on-chip loop filter. The design accommodates process, supply voltage and temperature variations. The voltage controlled oscillator incorporates a quadrature output ring structure with sub-feedback loops embedded to speed up and tune the circuit (developed in Chapter 3). The two separated tail current sources associated with each stage of the ring oscillator are connected to temperature compensated biasing and loop filter/V-to-I converter, respectively. An on-chip biasing reference circuit was developed to reduce the VCO's sensitivity to both supply and temperature variation without the use of a bipolar transistor as in the conventional design. The VCO is exceptionally linear and has wide tuning range. The achieved highly linear frequency transfer characteristics are important for maintaining a constant loop gain in the PLL over its lock range and modulation applications. Because the applications using this PLL require low phase noise. Emphasis is also placed on the analysis of the noise sources and their contributions to the overall noise performance of the PLL. The reference feed-through and the output glitch from the charge pump can generate periodic disturbance on the VCO control line. This effect is similar to high frequency modulation and is the dominant noise source to the output timing jitter. The fully integrated PLL was fabricated in a 0.35 μm CMOS process, occupies an active area of 1 mm^2, and consumes about 100 mW operating from a 3.3V supply. A rms timing jitter of 11 ps was measured.

CHAPTER 6

Conclusions

6.1 Summary

The focus of this thesis was the development of high speed monolithic CMOS ring oscillators. A general oscillator circuit topology capable of achieving high speed operation and multiple phase output was proposed. The topology used controlled sub-feedback inverters to construct fast loops for long chain, multiphase output ring oscillators to achieve higher speed. A linearized model was developed and led to the discovery of a relationship between speed and feedback index i. This speed-feedback index relation is important for fast loop construction and was confirmed by time domain HSPICE simulations. The operating frequency of the ring oscillator increases linearly with the transconductance (G_m) of sub-feedback inverters. G_m can be controlled with an external voltage. Thus, the sub-feedback loops based topology also provides an alternative to conventional capacitive or resistive tuning, which can be also understood as changing the effective number of delay stages

(N_{eff}) within the range of ($i+1$) and N. Both single-ended and differential inverter stages and control voltage can be used in the topology.

Detailed implementation of the proposed topology for both single-ended and differential circuits has been proposed and analyzed. For a sub-feedback loop based ring oscillator, the dc gain of inverters in the major loop should be kept greater than the minimum value for oscillation to occur. However, large values should be avoided to achieve low phase noise. The design was fabricated in 0.5 μm CMOS technology. VCO1 is a single-ended five stage ring oscillator with sub-feedback loops. It demonstrates a 62% increase in frequency with power consumption of only 6 mW. VCO3 is a four stage quadrature output ring oscillator with three stage sub-feedback loops. Compared with VCO2, which is a conventional four stage differential ring oscillator of the same transistor sizes, doubling of speed has been achieved. The linearity of the VCO frequency control transfer characteristics also improved.

For communications applications, one of the most critical VCO specification is phase noise. In Chapter 4, phase noise in single-ended ring oscillators and sub-feedback loop based differential ring oscillators was analyzed. For a single-ended ring oscillator, the analysis is based on a time domain noise model. The relationship between design parameters and timing jitter is derived for internal noise sources. The cycle-to-cycle jitter was shown to be inversely proportional to supply voltage and power consumption. For a fixed operation frequency, jitter is independent of stage number and can be reduced by increasing the ratio of W/L. The analysis of timing jitter in a single-ended ring oscillator also demonstrates its strong sensitivity to external interference signals, such as supply and substrate noise. On chip regulator can only be used to reduce the low frequency supply noise sensitivity at the cost of decreased effective supply voltage and output swing. The basic reason differential circuits were used is that they provide higher external interference re-

jection. However, the rejection is limited due to the nonlinear loading, nonlinear drain junction capacitor and mismatch of devices.

Phase noise in sub-feedback loop based ring oscillators has been analyzed in the frequency domain. Compared to time domain analysis, frequency domain analysis provides both an explanation for time domain waveform shaping and more insight into the noise filtering introduced by the sub-feedback loop architecture. Noise sources are classified into three groups according to their contribution to the total output phase noise. The proposed sub-feedback loop based ring topology improves the equivalent Q factor. The noise shaping function for the noise from the driving transistors and loading resistors which are connected directly to the signal path is also improved. The Q value is a function of gain of the sub-feedback inverter and feedback index i. By choosing the optimum feedback index i, phase noise performance can be improved for the sub-feedback loop based ring oscillators (e.g., for 7 stage ring oscillator with sub-feedback loops, the circuit based on i=4 is expected to have better noise performance compared to the circuit based on i=2).

In addition to considerable effort into the development of high speed ring oscillators, an inductor based oscillator was also explored for low noise design [Appendix A]. The LC oscillator was fabricated in a 0.35 μm triple-metal, double-poly CMOS process, occupies an active area of 0.5 mm^2, and consumes 20 mW power at 3.3 V. The measured phase noise performance at 1.8 GHz is -98.3 dBc/Hz at 500 kHz offset frequency.

A 1.25 GHz monolithic CMOS PLL clock generator unit was designed for data communications. The monolithic PLL consists of a ring oscillator, divider, phase/frequency detector, charge pump and on-chip loop filter. The design accommodates process, supply voltage and temperature variations. The voltage controlled oscillator incorporates a quadrature output ring structure with sub-feedback loops embedded to speed up and tune

the circuit. The two separated tail current sources associated with each stage of the ring oscillator are connected to a temperature compensated biasing and loop filter/V-to-I converter, respectively. An on-chip biasing reference circuit was developed to reduce the VCO's sensitivity to both supply and temperature variation without the use of a bipolar transistor as in the conventional design. The VCO is exceptionally linear and has a wide tuning range. Because the applications using this PLL require low phase noise, emphasis is also placed on analysis of the noise sources and their contributions to the overall noise performance of the PLL. The PLL was fabricated in a 0.35 μm CMOS process, occupies an active area of 1 mm^2, and consumes approximately 100 mW operating from a 3.3 V supply. A rms timing jitter of 11 ps was measured. The measurement results confirm the suitability of the VCO and the PLL for applications such as clock generation/recovery systems, high speed multiphase data sampling and microprocessor clock synchronization.

6.2 Future Work

The research work described in this thesis can be pursued further in a number of areas: (1) Accurate prediction of phase noise in oscillators remains a challenging area. The analysis needs to take into consideration the dynamic and nonlinear nature of the circuits and should lead to intuitive guidelines for circuit designers. (2) For an LC oscillator, the characterization and improvement of quality factors (Q) for both the inductor and varactor in the commercial CMOS process can be further investigated. (3) Because of its switching operation, the charge-pump PLL can not be analysed as a linear system in certain circumstances. An exact analysis taking into account the discrete and nonlinear characteristic of the circuits can be explored. (4) Reducing the timing jitter in monolithic PLLs continues to be a challenge for architecture and circuits designs. Since power supply and substrate noise are two of the major noise sources, it is suggested that fully differential PLL building blocks are developed for future low jitter applications. (5) In mobile cellular applica-

tions, the noise shaping $\Delta\Sigma$ modulus controller is also an area whose properties merit further study. High order architecture with single bit output and good stability can be investigated to reduce the complexity of the multi-modulus divider (MMD) and phase noise of the frequency synthesizer. (6) Monolithic integration of a PLL with a digital Delta-Sigma modulator in a deep submicron CMOS process to form a complete fractional-N frequency synthesizer would be of commercial interest. (7) The ring oscillators and PLL developed in this thesis can be implemented in 0.25 μm or 0.18 μm CMOS process with minor modification to operate at 2.5 GHz for OC-48 SONET transceivers.

Appendix A:

Design and Implementation of a 1.8 GHz 0.35 μm CMOS Monolithic LC Oscillator

A monolithic CMOS LC tank oscillator was designed and fabricated for digital mobile communications. The LC VCO circuit schematic is shown in Fig. A-1. NMOS transistors M1 and M2 are coupled in positive feedback to provide a negative resistance to cancel losses in the resonator. M3, M4 provide biasing current. Buffer circuits are used to drive the off-chip loads. According to Leeson's noise model, to minimize the phase noise of an oscillator, the oscillator has to use a high Q LC tank, an active circuit with low noise factor, active devices with low flicker noise, and high signal swing at the resonator.

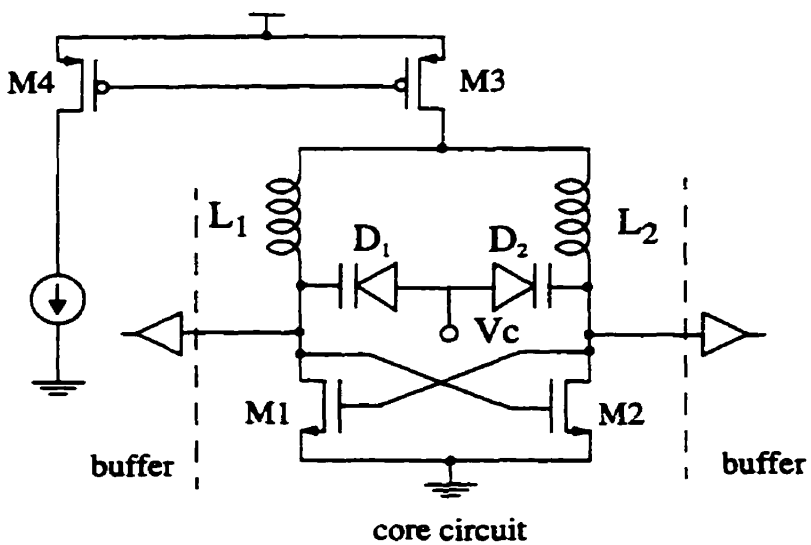


Fig. A-1. LC oscillator

(a) Oscillator Design

It is desirable to maximize the value of the spiral inductor to increase voltage swings and hence decrease phase noise. However, the maximum value of the inductor is determined by a self-resonant frequency and tuning range. The chosen spiral inductors have a value of 6.3 nH at 2.0 GHz. The total capacitance is 1 pF. Inductors L_1, L_2 are implemented by metal 3 as shown in Fig. A-2. An appropriate equivalent circuit of a microstrip line on silicon process is shown in Fig. A-3, where L is the total inductance of the line and r is the series resistance due to conductor losses and dissipation arising from current flowing in the silicon substrate. The shunt parasitics result from a combination of capacitances, due to an insulating layer of silicon dioxide (C_{ox}) and the underlying substrate (C_{si}), and substrate dissipation (R_{si}) [LoCo97].

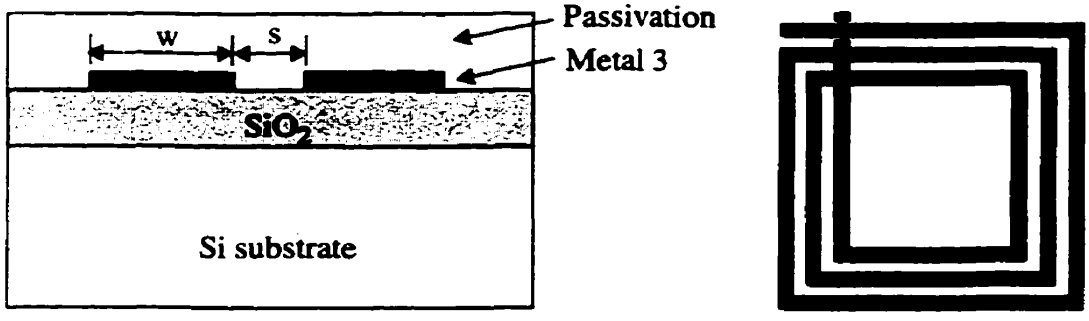


Fig. A-2. Cross-sectional view of the inductor

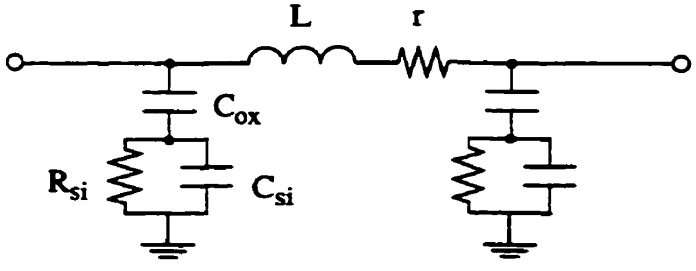


Fig. A-3. Microstrip line equivalent circuit

For the spiral inductor, additional components are required to represent mutual magnetic and electric coupling between adjacent lines.

The substrate and metal properties for the 0.35 μm CMOS fabrication process are listed in Table A-1. The designed inductor has a width of 10 μm and spacing of 2 μm. The internal dimension was chosen as 100 μm to minimizes negative mutual coupling on opposite sides of the spiral. The turn number is 4.5. The simulations are based on ASITIC which is a CAD tool for inductor/transformer design and analysis [NiMe98].

Table A-1 Substrate and metal parameters of a 0.35μm CMOS process

Parameter	Value
Silicon resistivity (rho)	15 ohm-cm
Silicon thickness (t1)	400 μm
Silicon relative permittivity (eps1)	11.7
Oxide resistivity	1e10 ohm-cm
Oxide thickness below Metal 3 (M3)	4.03 μm
Oxide thickness above Metal 3 (M3)	6 μm
M3 thickness	0.92 μm
M3 sheet resistance (rsh)	40 milli-ohm/sq.

The LC-tank's effective resistance includes the parasitic resistances of the inductor and capacitors. Since the value is approximately 30 Ω, the required negative conductance provided by the transistors must be $R_s(\omega C_t)^2 = 30 \cdot (2\pi \cdot 2.0GHz \cdot 1pF)^2 = 4.7ms$. Using a safety factor of 2.5, each of the amplifying transistors must have a transconductance g_m of 12 ms. Since $g_m = \mu_n C_{ox}(W/L)V_{eff} = 2(I_D/V_{eff})$, the small value of V_{eff} corresponds to small I_D, resulting in lower power consumption. However, the transistor size becomes large and its parasitic capacitance increases, causing reduced tuning range. The V_{eff} and I_D are chosen to be 0.4 V and 4.4 mA. This yields a width of 150 μm for transistor M1, M2.

The capacitor of the LC-tank is formed by the inductor's parasitic capacitance to the substrate, the drain-bulk, gate-drain and gate-source capacitances of the NMOS transistors, the loading capacitance of the buffers and the tunable p+/n well junction capacitor (varactor). In order to achieve a large tuning range, the last contribution must be as large as possible [CrSt95][King98][PaAl99].

The varactors are implemented by a p+ diffusion in a n-well. The reverse pn junction capacitance of the varactor is controlled by an external control voltage. The layout of the varactor is important to achieve high Q capacitance. A strapping n-well structure [Raz971] was used to reduce the series resistance.

The fixed part of the varactor capacitance contributes 40% of the total tank capacitor (1 pF). The parasitics of M1, M2 (150 μm/0.35 μm) contribute about 45%. The parasitic of M5, M6 (50 μm/0.35 μm) contributes 15%. Since the junction capacitor per unit area for the 0.35 μm CMOS process is $C = 886 \cdot aF/\mu m^2$. The varactor takes an total effective area of 451 μm^2.

(b) Implementation and Measurement Results

The design was implemented in a tsmc 0.35 μm triple-metal, double-poly CMOS process and fabricated through CMC. The layout is shown in Fig. A-4. It occupies an active area of 0.5 mm^2. The differential output signal is available from the bottom bonding pads (V_{out2}, V_{out4}). Biasing current is applied on the top bonding pads (V_{bias}). Power supply and tune voltage are applied on the bottom pads. Appendix C shows the top level layout of the die (ICDCULS3) which includes three other oscillator circuits, dummy inductors, and varactors for calibration purposes.

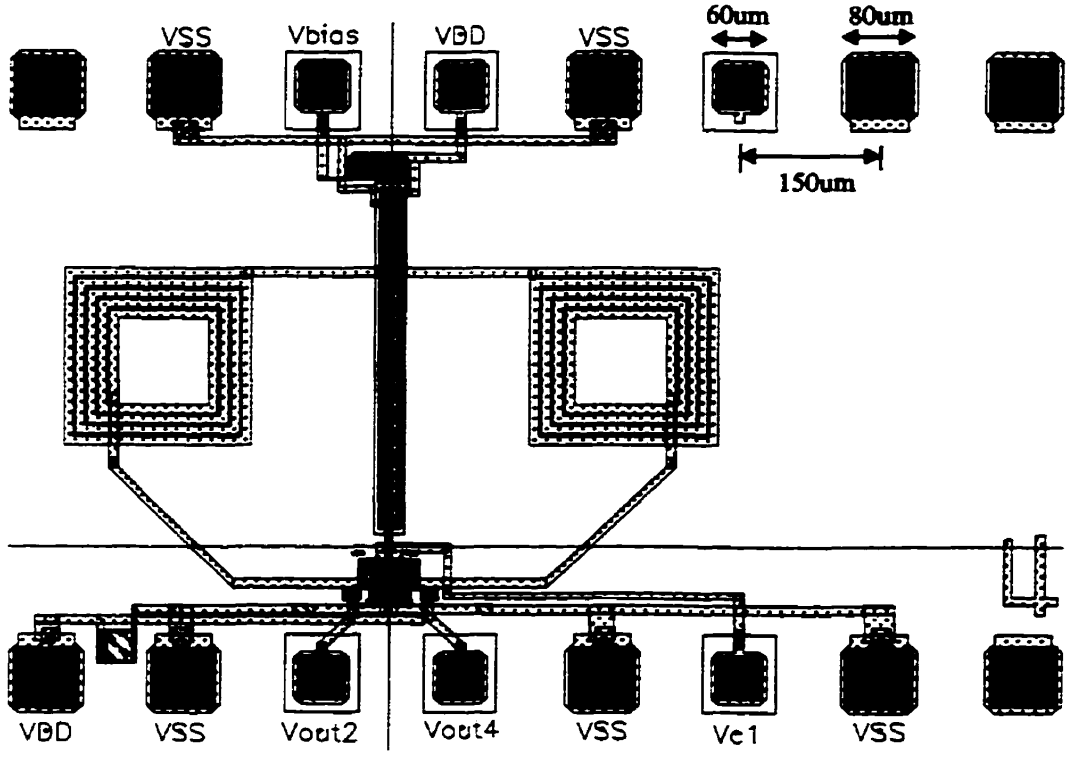


Fig. A-4. Layout of the 1.8 GHz LC oscillator (VCO4)

The circuit was tested on a wafer with multicontact RF probes from Cascade Microtech. Fig. A.5 shows the measured results of the Q factor from a dummy inductor of the same size (in the same chip). The measurement was performed using HP Network Analyzer 8720A and following the standard calibration procedure. The maximum value of Q is 3.2 around 1.8 GHz. The LC VCO output spectrum is shown in Fig. A-6. The center operating frequency is 1.77 GHz, which is slightly lower than simulation. This may be caused by the accuracy of available process parameters and the inductor model. The measured phase noise is -98.3 dBc/Hz at 500 kHz offset frequency with power consumption of 20 mW.

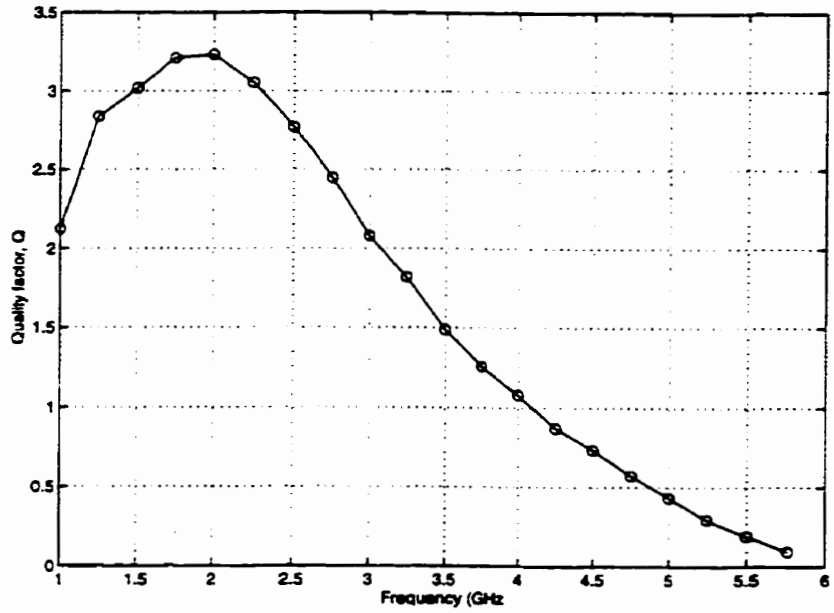


Fig. A-5. Measured Q factor

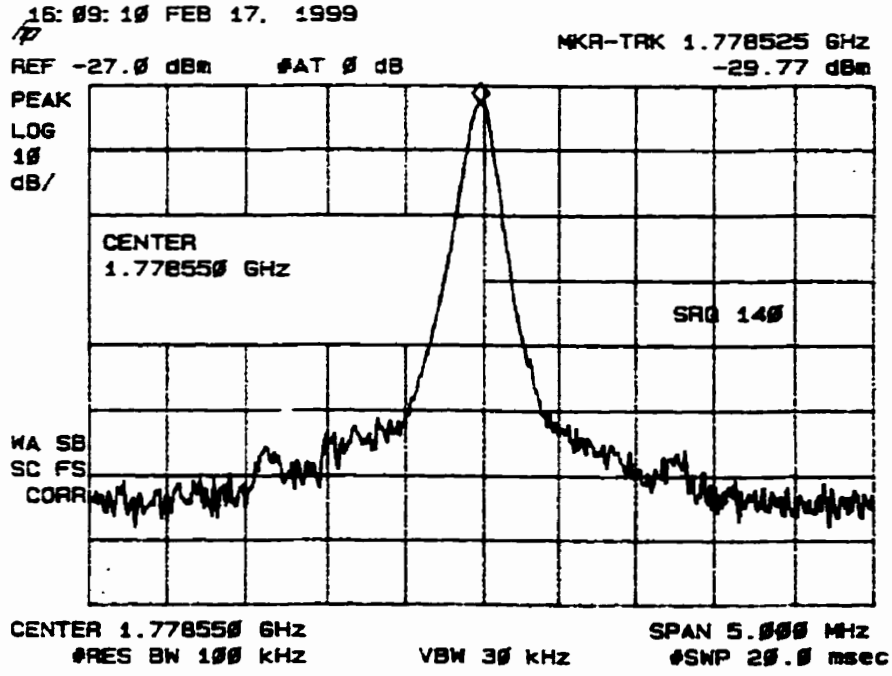
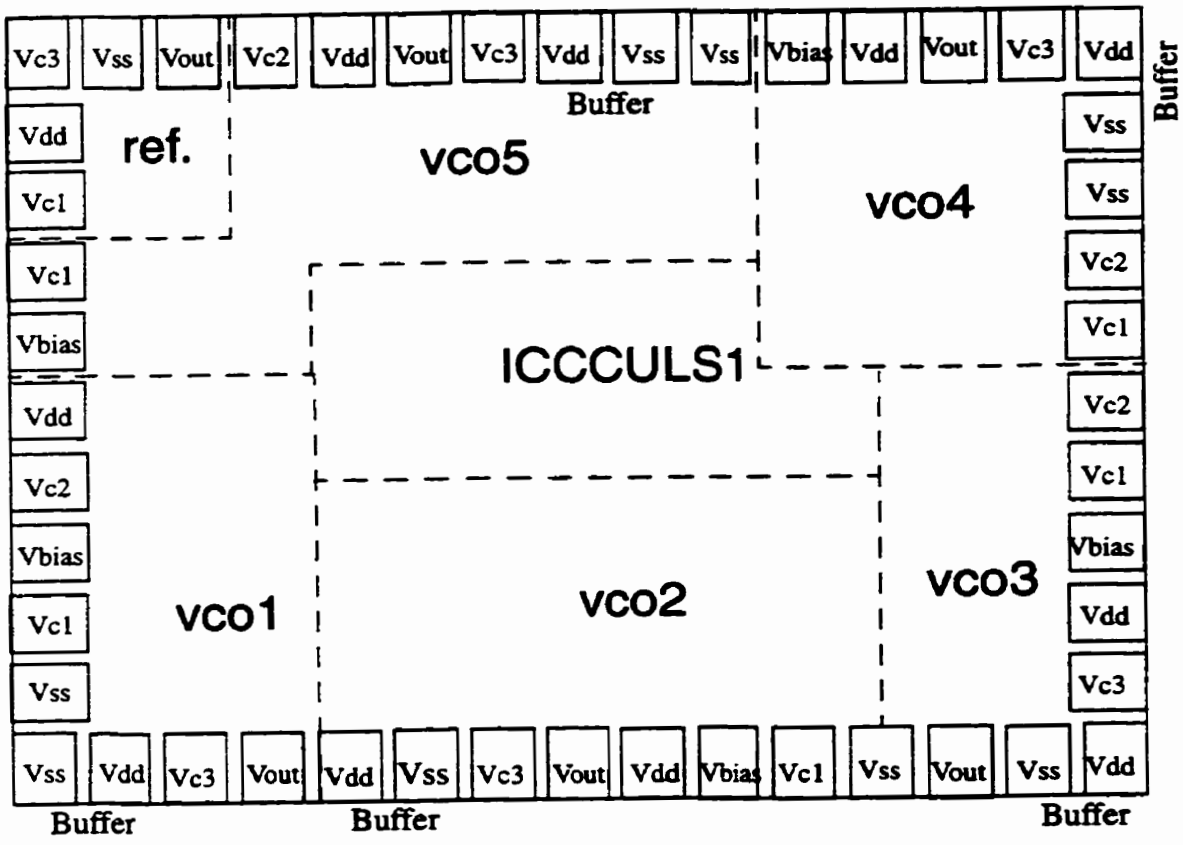


Fig. A-6. LC VCO output spectrum

Appendix B:

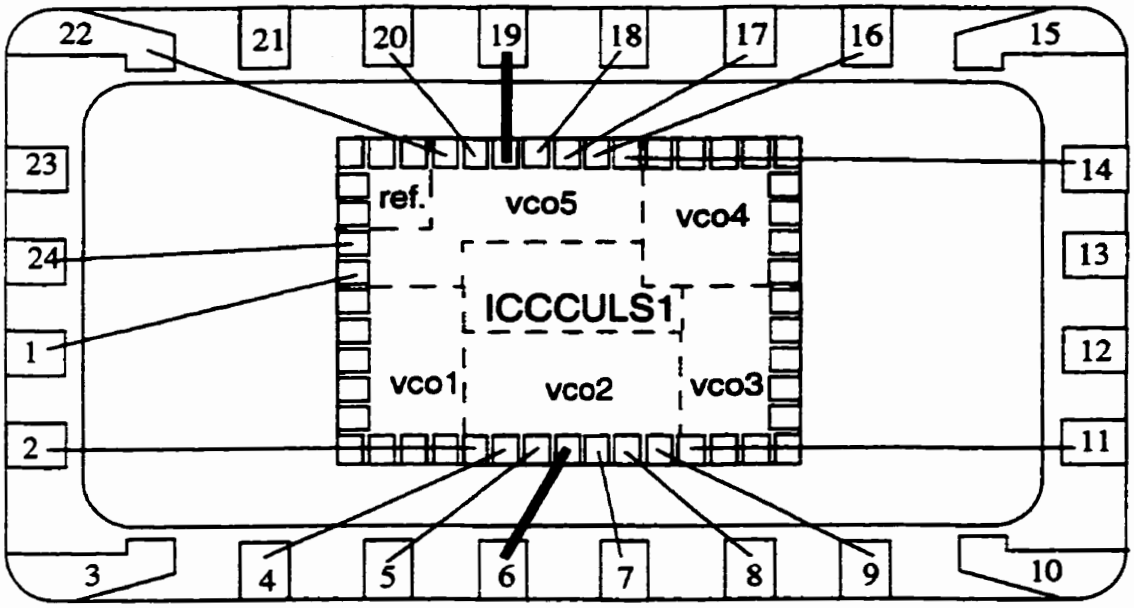
HP 0.5 μm CMOS Ring VCOs Chip (ICCCULS1)

(a) Pin Diagram



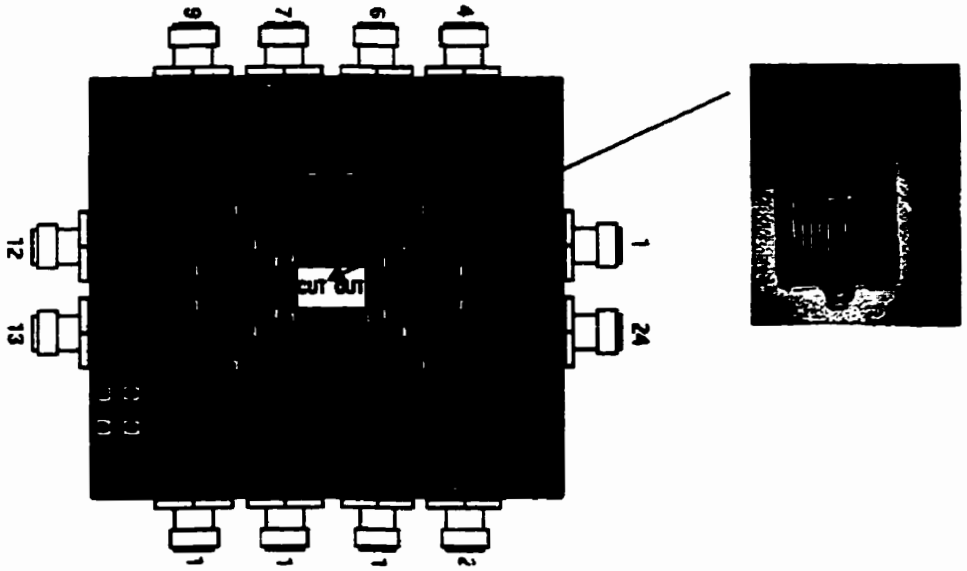
(In logo ICCCULS1, CC represents HP 0.5μm process, CU represents Carleton Univ.)

(b) Bonding diagram (set 1) with 24 pin Ceramic Flat Package (CFP)*

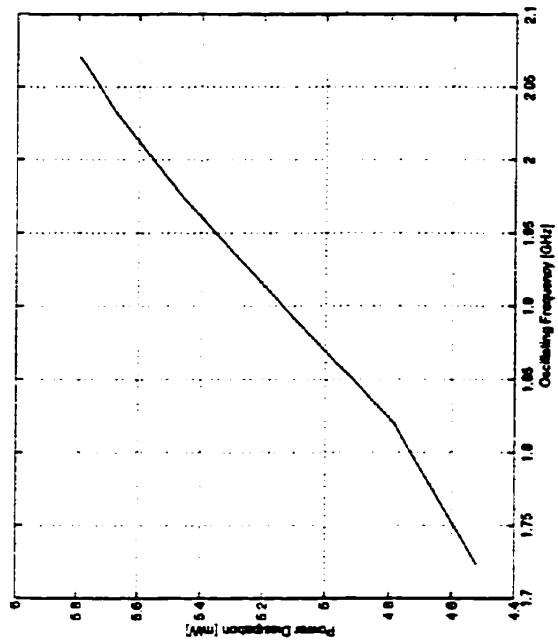


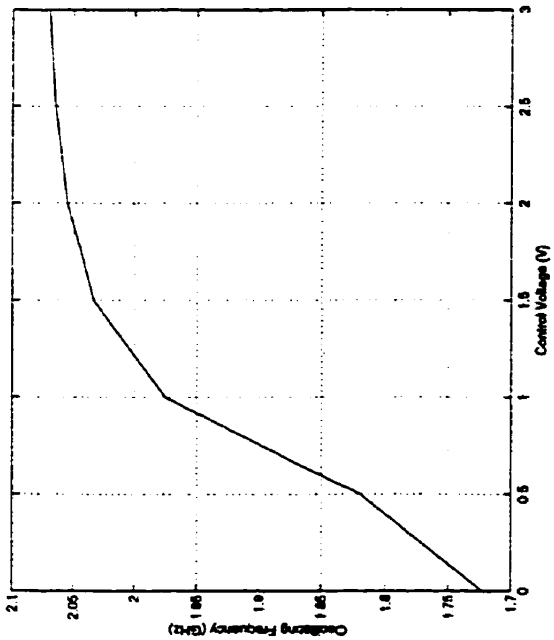
* Bonding diagram set2 and set3 are not shown here

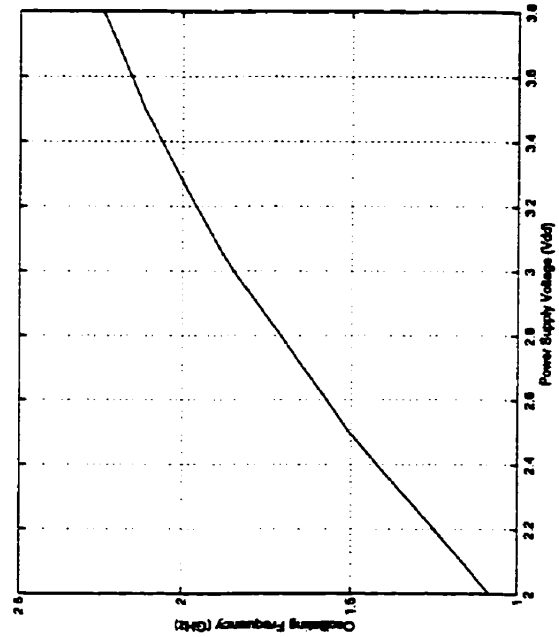
(c) Package and PCB for Testing (provided by CMC)



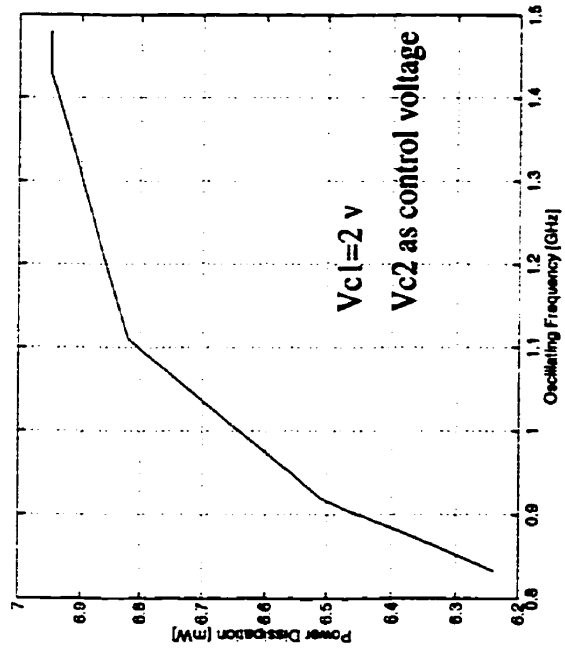
(d) Measurement Results (VCO-REF)

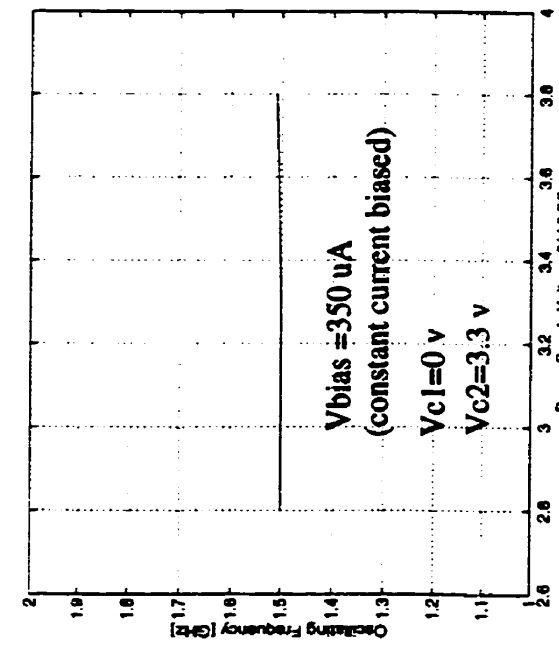


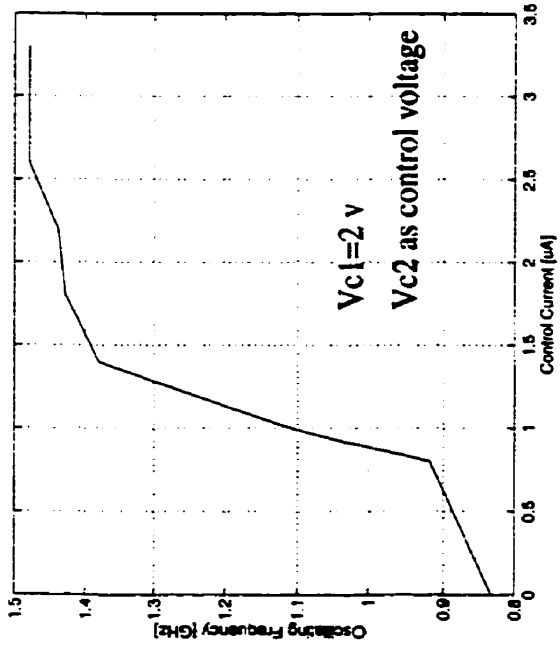


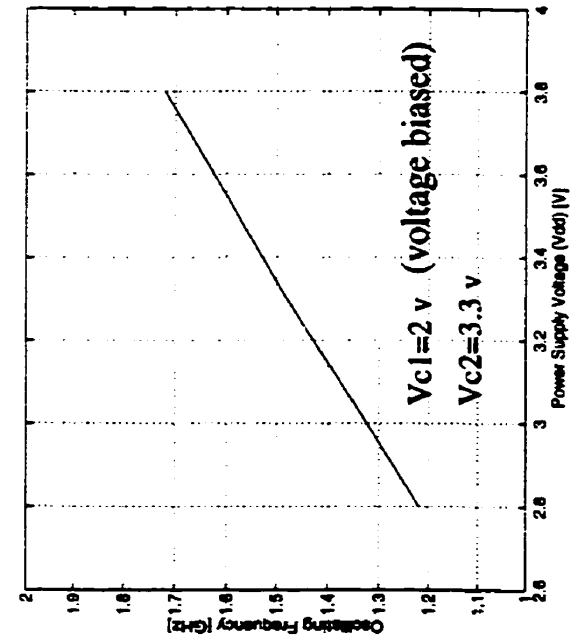


(e) Post Layout Simulation Results (VCO1)

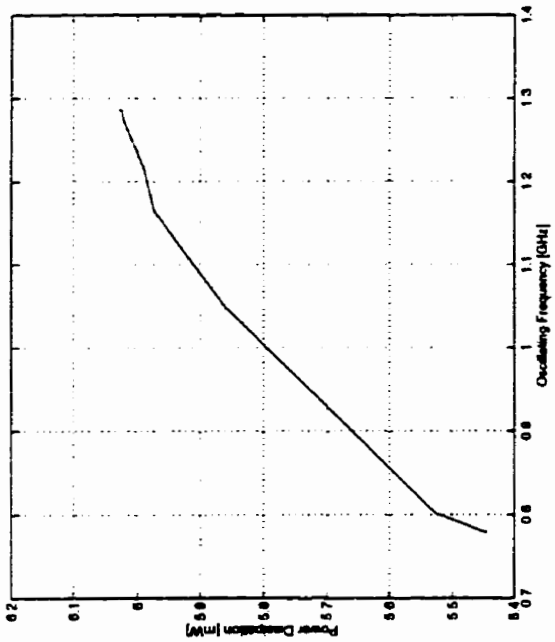


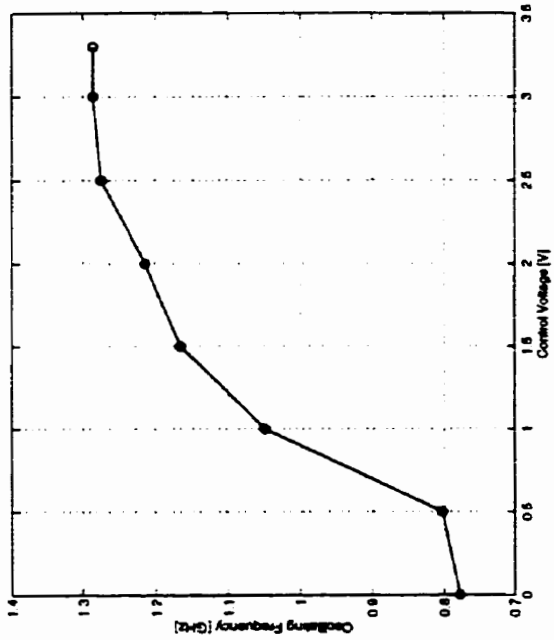


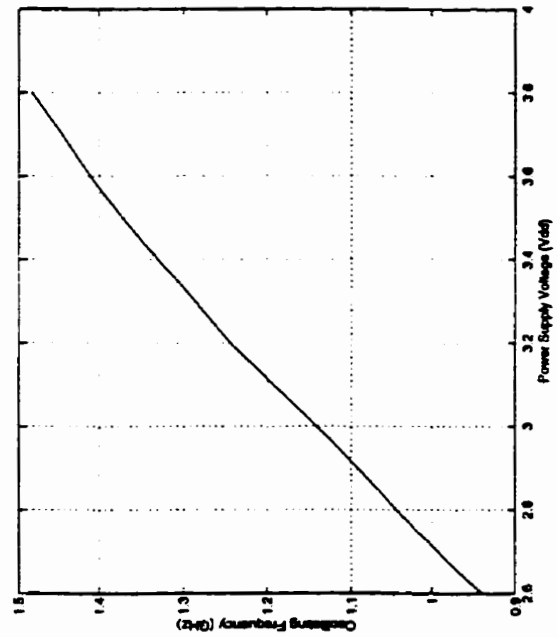




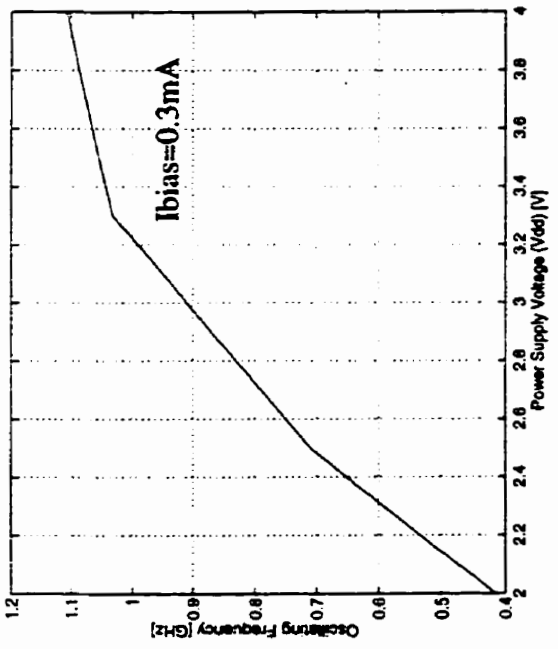
(f) Measurement Results (VCO1)

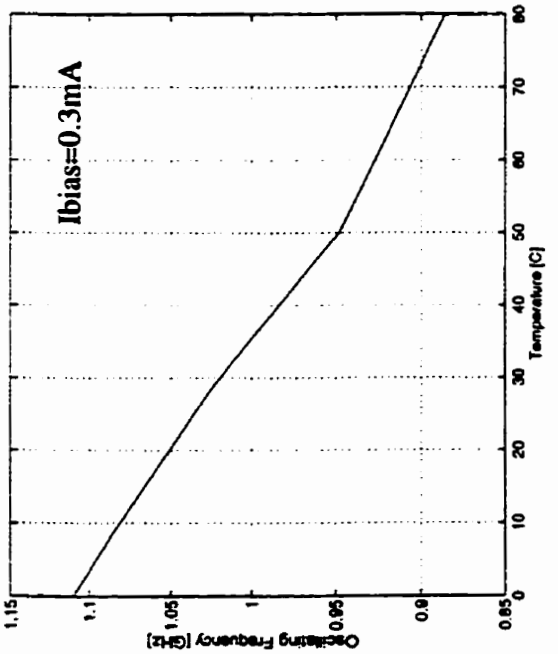


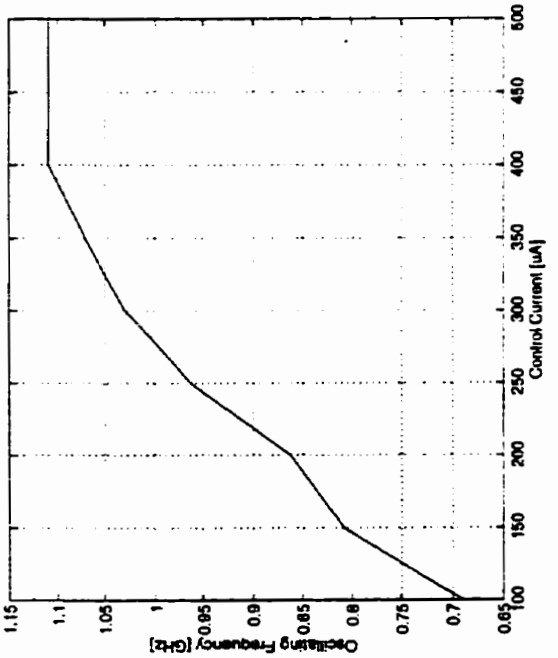


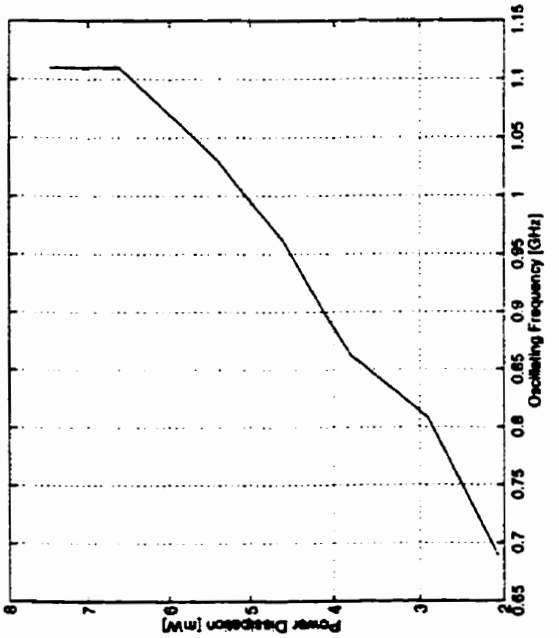


(g) Post Layout Simulation Results (VCO2)





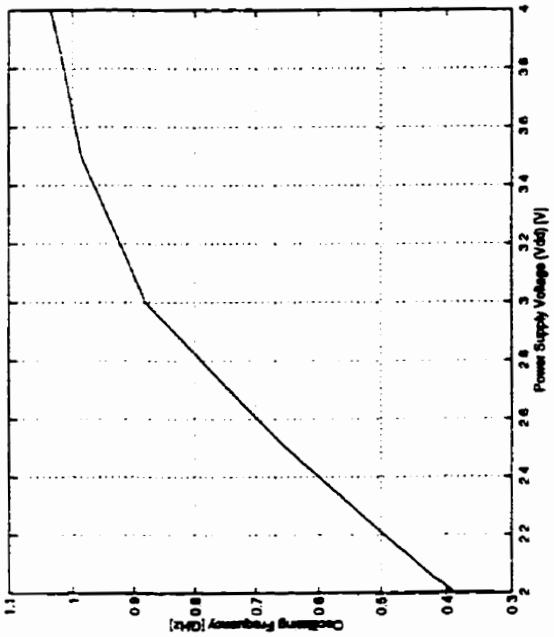


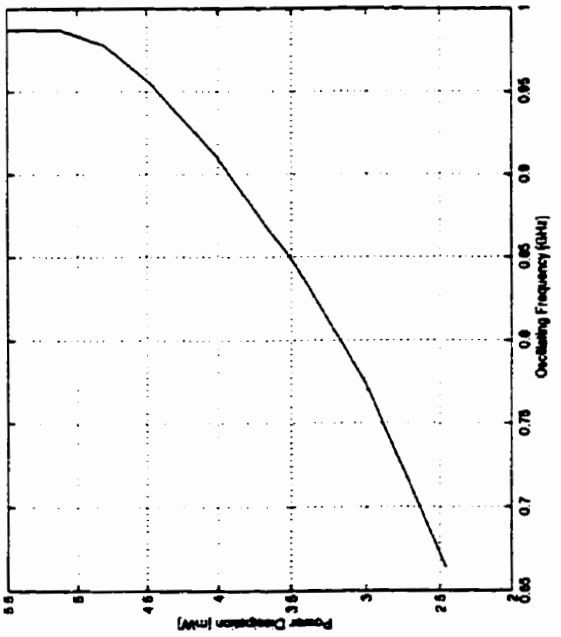


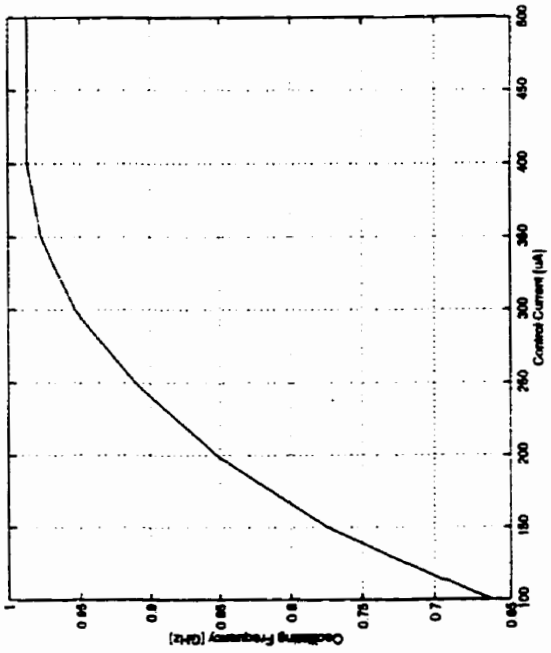
(h) Measurement Results (VCO2)

Ib=300uA

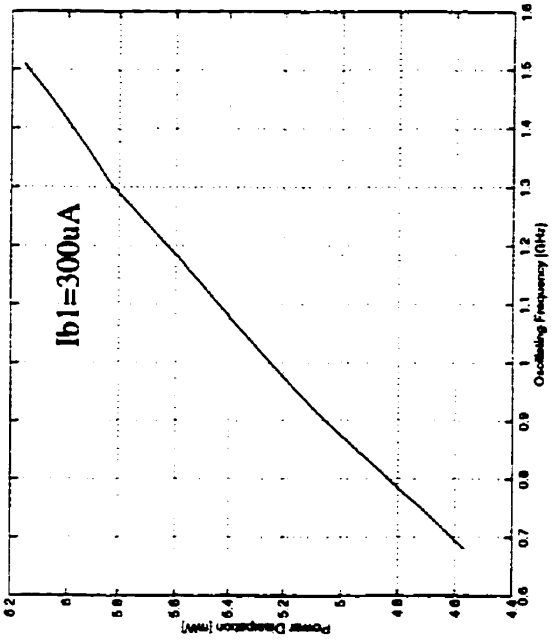
Vbias=3.3V

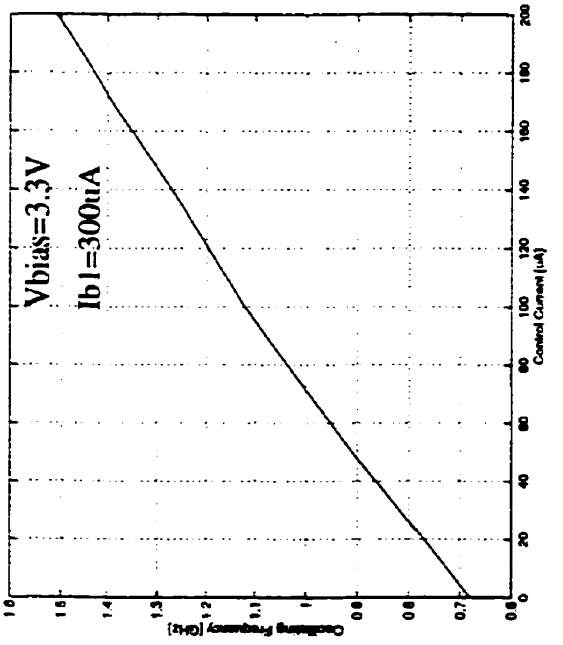


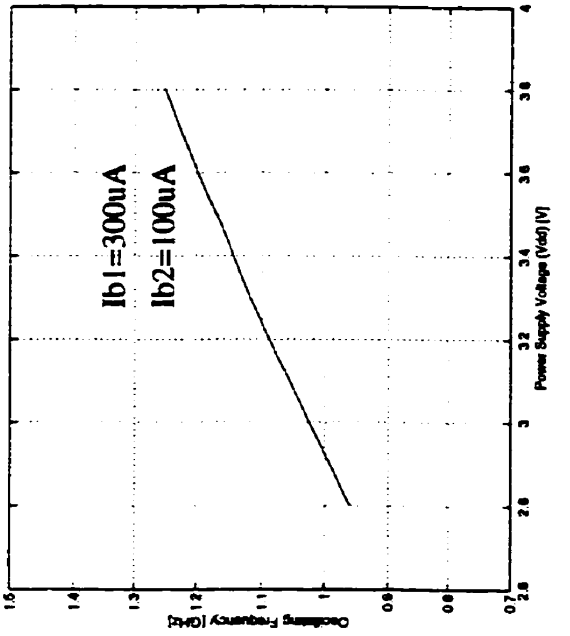




(i) Post Layout Simulation Results (VCO3)

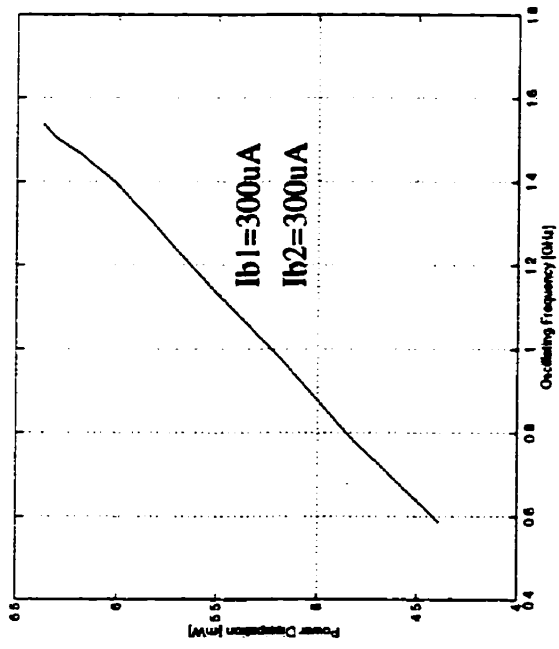


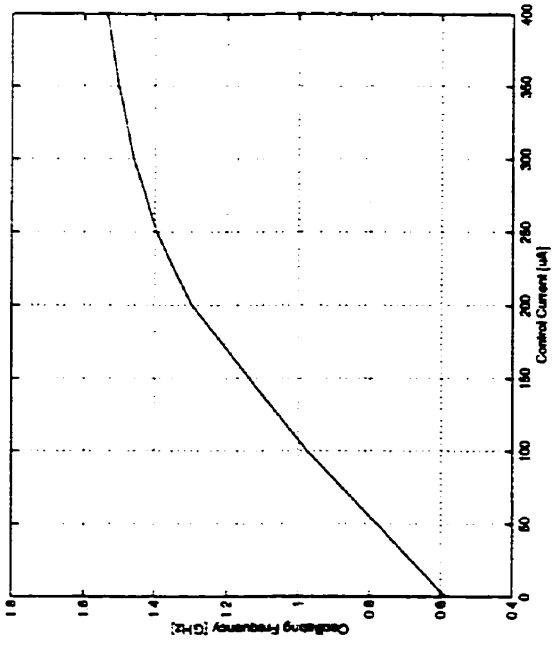


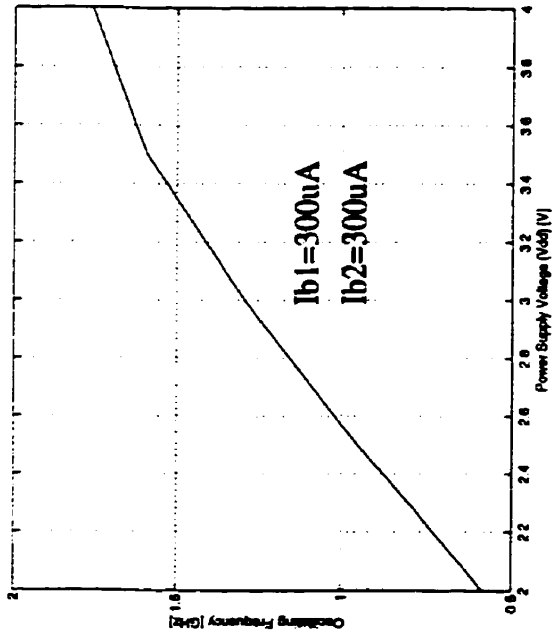


(j) Measurement Results (VCO3)

V_{bias}=3.3V
I_{b1}=300uA

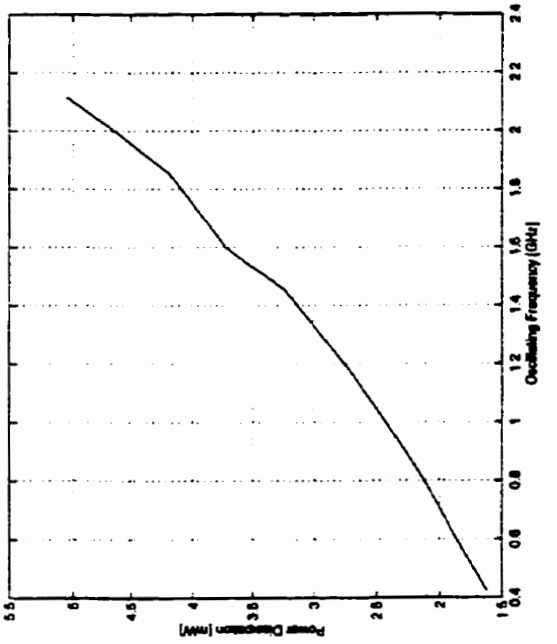


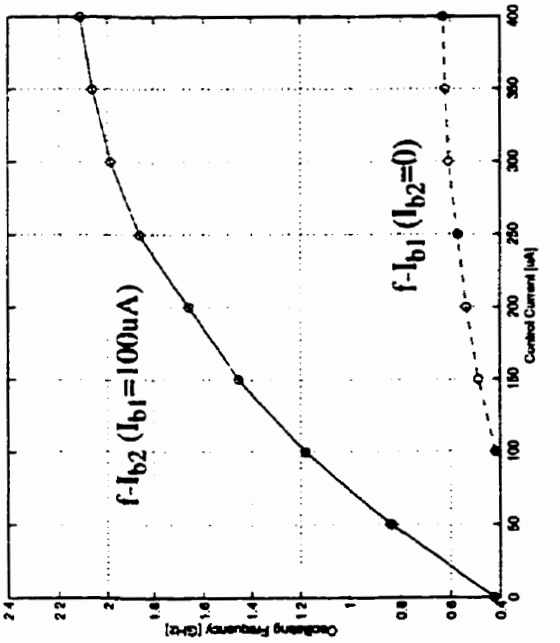


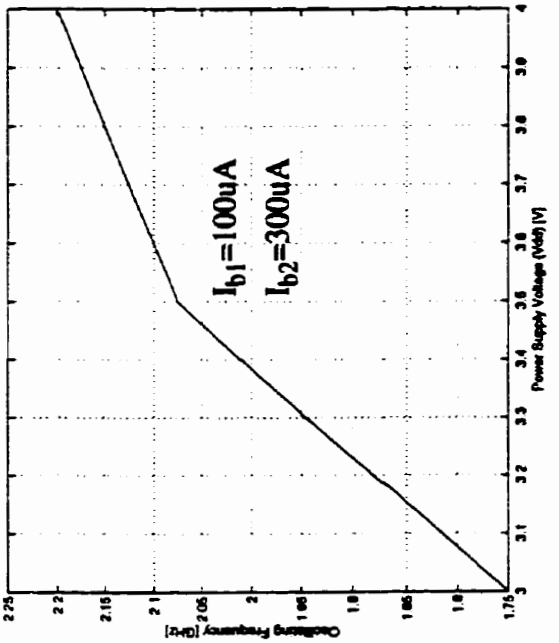


(k) Measurement Results (VCO3)

V_{bias}=3.3V
I_{b1}=100uA

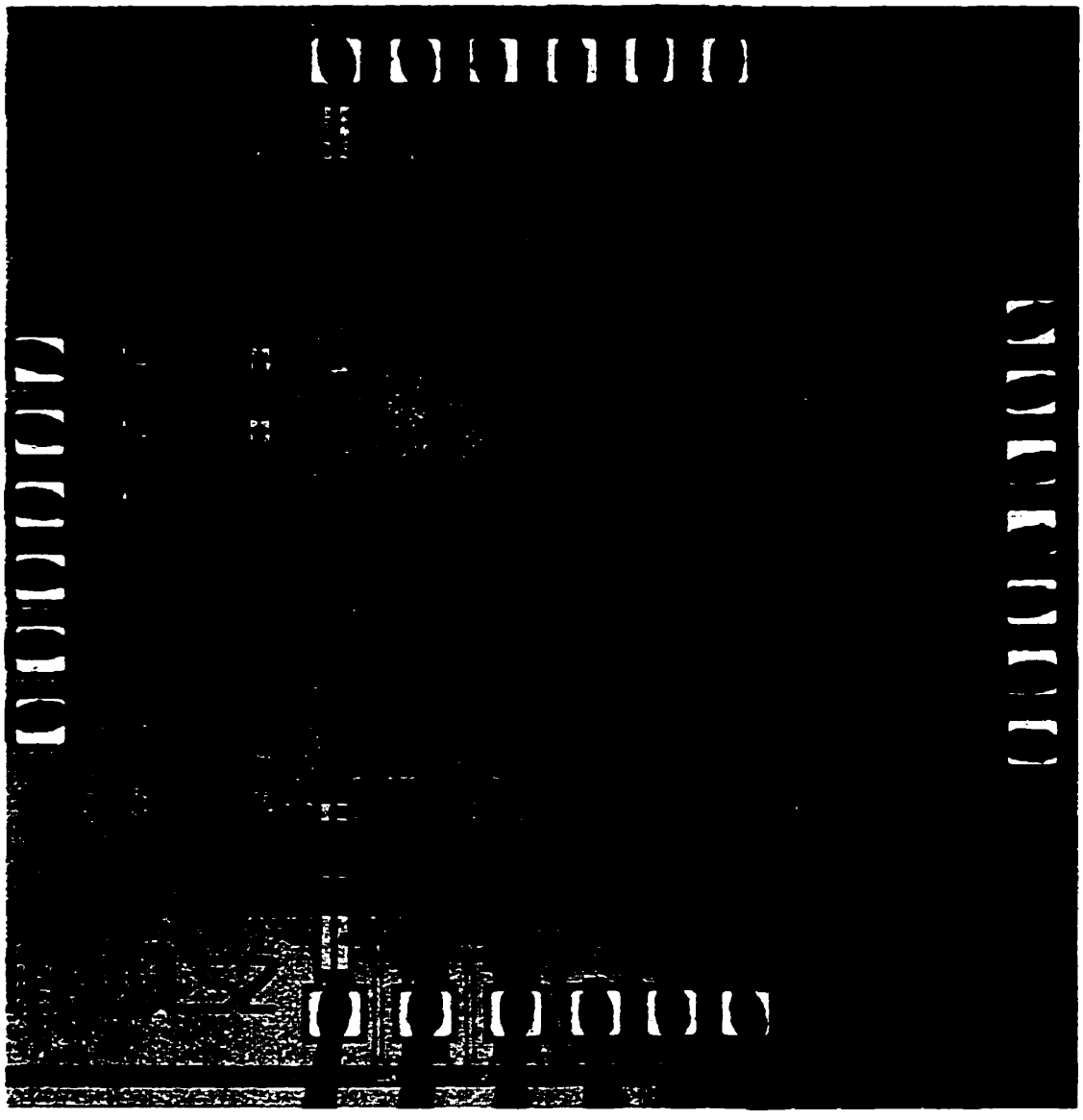






Appendix C:

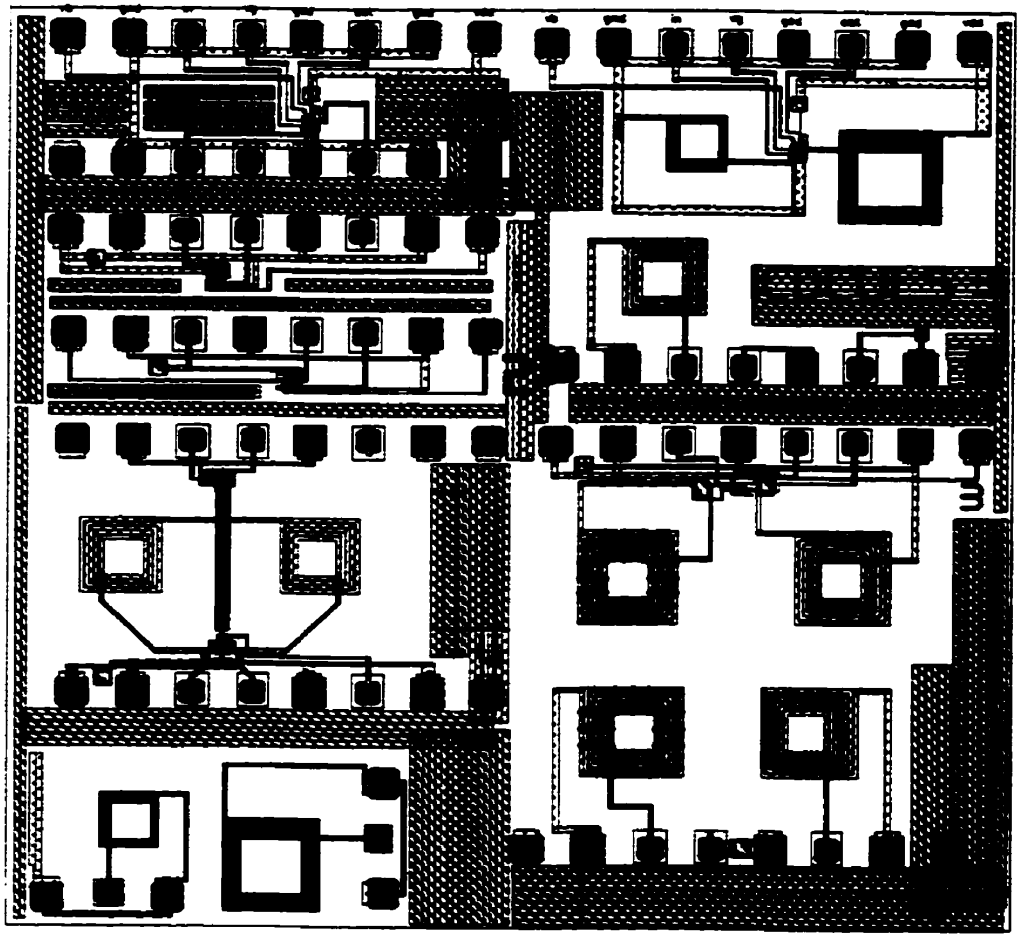
Die Photo of a Digital Delta-Sigma Modulator for Fractional-N Frequency Synthesis (IBACULS2)



Die Photo (IBACULS2, 2.3 x 2.3 mm^2, fabricated with NT 0.8 µm BiCMOS process)

Appendix D:

Layout of TSMC 0.35 μm CMOS LC Oscillators (ICDCULS3)



Top level layout

Appendix E:

Phase Noise Measurement Techniques

The phase noise of oscillators can be measured using the direct spectrum analyser method, the frequency discriminator method and the phase locked loop method [HP88][HP89][HP90]. The basic measurement setup, the equipment utilized, and the advantages and disadvantages of each will be summarized here.

(a) The Direct Spectrum Analyser

In the direct spectrum analyser method, the VCO output is directly connected to a spectrum analyser tuned to the source frequency. Since it is impractical to make measurements of noise power in a 1 Hz bandwidth, this results in measurement of the noise in a wider bandwidth which must be corrected to 1Hz by reducing the noise measured by 10 dB for every decade by which the filter is wider than 1 Hz. Furthermore, the direct spectrum analyser technique will usually require correction factors, since the detector of the analyser is ordinarily an envelope rather than a true rms detector, the log amplifiers amplify noise peaks less, and the bandpass filters may be Gaussian or trapezoidal in shape, which requires correction to a square bandpass. Hence, using the direct spectrum technique, the phase noise L(f) in dBc/Hz at any offset frequency f_m can be calculated as:

$$L(f_m) = P_M(f_m) - P_C - c_1 + c_2$$

where $P_M(f_m)$ is the measured average noise power for a given resolution bandwidth in dBm at an offset frequency f_m, and P_c is the measured carrier power in dBm. c_1 is the correction factor to calculate the measured noise power of a 1 Hz rectangular bandwidth [=

10 log(1.2 x resolution BW) dB for the HP8591 spectrum analyser [HP90]]. c_2 is the spectrum analyser effects correction factor (2.5 dB for an HP8591 spectrum analyser).

The direct spectrum measurement technique is the easiest technique for measuring oscillator noise. It provides quick, qualitative analysis of an oscillator and can be utilized for a broadband frequency range. However, it has limited resolution for close-in measurement. It can not be used to measure spectrally pure sources, nor can it measure noisier sources that have either high AM or drift. The technique is most useful when it can be determined that the noise of the oscillator being measured is worse than that of the local oscillator of the spectrum analyzer and AM noise is less than phase noise. It is perfect for measuring the phase noise on a stable (phase locked) source with relative high noise sidebands. In summary, the direct spectrum measurement technique is optimum for measuring a source with relatively high noise and low drift.

(b) The Frequency Discriminator Method

In the frequency discriminator method, the frequency fluctuations of the source are translated to baseband voltage fluctuations by the frequency discriminator which can then be measured by a baseband analyser.

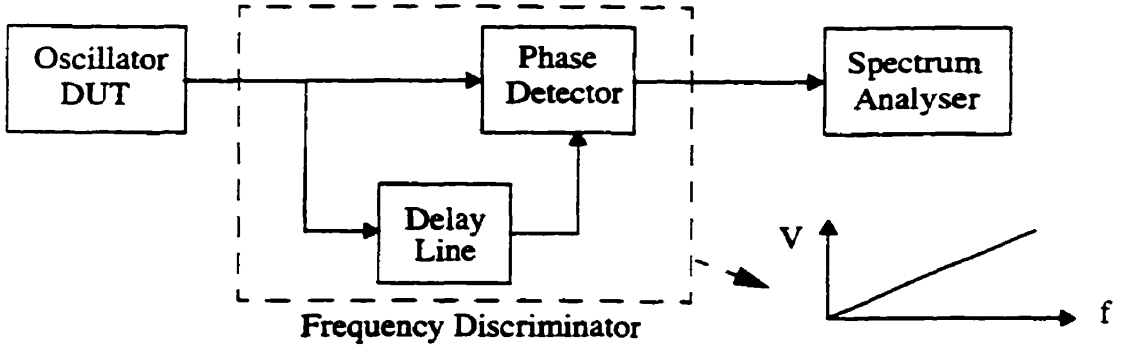


Fig. E-1. The frequency discriminator phase noise measurement technique

There are various implementations of frequency discriminator, one of which is the delay line/phase detector implementation which is employed in the HP3048A phase noise measurement system [HP89]. In that implementation of frequency discriminators, the signal from the tested frequency source is split into two channels, the signal of one path being delayed relative to the signal in the other path as shown in Fig. E-1. This unequal delay converts the frequency fluctuations of the signal into phase fluctuations. The phase detector then converts phase fluctuations to voltage fluctuations, which are read by the spectrum analyzer and are related to the phase noise of the source. Phase noise measurement using that method requires a procedure for set up, calibration and data conversion which is automated in the HP3048A phase noise measurement system.

This technique demonstrates better sensitivity than the direct spectrum analyzer technique, since the translation to baseband voltage permits the use of spectrum analyzers with a baseband analyzer or fast Fourier transform analyzers. In general, the sensitivity of this system is limited by the internal noise of the frequency discriminator. However it is difficult to implement due to loss in the delay line which makes it limited in the maximum range of offset frequencies. It also has poor close-in sensitivity (sensitivity at small offset frequencies).

(c) The Phase-Locked Loop Method

A typical block diagram is shown in Fig. E-2, where two sources at the same frequency and in phase quadrature are input to the double-balanced mixer used as a phase detector, the output of the mixer will be the sum and the difference of frequencies. The sum is filtered by the low-pass filter (LPF) to prevent it from overloading the LNA or the baseband analyser. Any phase fluctuation that is not common to both signals will be represented by a phase term in the difference frequency signal. The LNA improves the sensitivity and the noise figure of the spectrum analyser. Analog spectrum analysers are used for high offset

frequency measurements and digital spectrum analysers are useful for close-in offsets but limited in the maximum range of offset frequency. Hence, a combination of both is needed for a wide offset frequency range. This phase noise measurement technique is also implemented in the HP3048A system [HP89]. It is the most sensitive and broadband method.

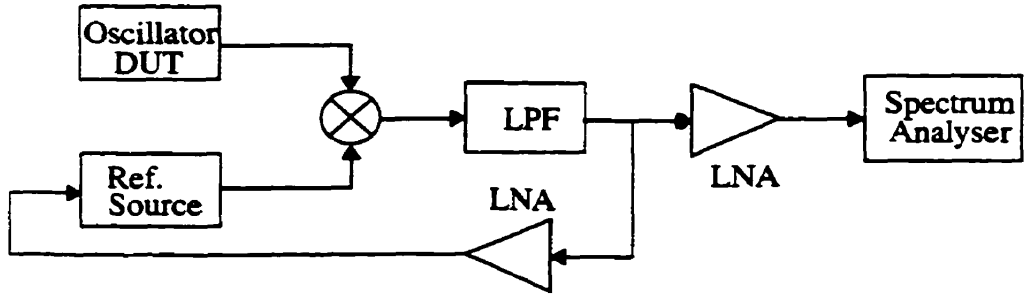


Fig. E-2. Measurement of spectral density of phase fluctuations with a phase locked loop

It is important that the phase detector input sources stay in quadrature (90° phase relationship), since it is the condition at which the system is operating near the "zero" crossing of the phase detector. The sources are held in a 90° phase relationship by the use of a second order phase locked loop (PLL) in a feedback path to one of the oscillators, the utilization of the PLL to maintain lock at the phase detector for a drifting frequency source does not contradict the fact that it is an open loop measurement. Since, however a correction factor is needed while measuring phase noise at offset frequencies less than the PLL bandwidth, care should be taken to use a PLL bandwidth less than that of any offset frequency of interest to increase the validity of the measured performance.

References

[AbMe83] A. A. Abidi and R. G. Meyer, "Noise in relaxation Oscillators", *IEEE J. Solid-State Circuits*, vol. 18, pp. 794-802, Dec. 1983.

[Abi86] A. A. Abidi, "High-frequency noise measurements on FET's with small dimensions," *IEEE Trans. Electron Devices*, vol.ED-33, pp. 1801-1805, Nov. 1986.

[Abi97] A. A. Abidi, "Low-power radio frequency ICs for portable communications," *Proc. of IEEE*, vol. 83, no. 4, pp. 544-569, 1995.

[Abou96] M. Abou-Seido, "Design and analysis of CMOS monolithic inductor-less voltage controlled oscillators," Master thesis, Carleton University, 1996.

[AlTh96] A. Ali and J.L. Tham, "A 900MHz frequency synthesizer with integrated LC voltage controlled oscillator," in *ISSCC Dig. Tech. Papers*, pp. 390-391, Feb. 1996.

[AnRu93] W. Anzill and P. Russer, "A general method to simulate noise in oscillators based on frequency domain techniques," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-41, no. 12, pp. 2256-2263, Dec. 1993.

[ANST] American National Standard for Telecommunications - Digital Hierarchy - Optical interface rates and formats specifications, ANSI T1.105-1991.

[ASGC95] J. Alvarez, H. Sanchez, G. Gerosa, and R. Countryman, "A wide-bandwidth low-voltage PLL for PowerPC^{TM} Microprocessors," *IEEE J. Solid-State Circuits*, vol. 30, pp. 383-391, April. 1995.

[Ash96] K. B. Ashby, I. A.Koullias, W. C. Finley, J. J. Bastek, and S. Moinian, "High Q inductors for wireless applications in a complementary silicon bipolar process," *IEEE J. Solid-State Circuits*, vol. 31, pp. 4-9, Jan. 1996.

[AyRa95] T. Aytur and B. Razavi, "A 2 GHz 6mW BiCMOS frequency synthesizer," in *ISSCC Dig. Tech. Papers*, pp. 264-265, Feb. 1995.

[Banu88] M. Banu, "MOS oscilltors with multi-decade tuning range and gigahertz

maximum speed," *IEEE J. Solid-State Circuits,* vol. 23, no. 12, pp. 1386-1393, Dec. 1988.

[BCR] Bell Communications Research - SONET Transport Systems: Common Generic Criteria, TR-NWT-000253, Issue 2, Dec. 1991.

[BiRe92] R. F. Bitting, W. P. Repasky, "A 30-128 MHz frequency synthesizer standard cell," *Proc. CICC*, 1992.

[BuMa91] A. W. Buchwald and K. W. Martin. "High-speed voltage-controlled oscillator with quadrature outputs," *Electron. Lett.*, vol. 27, no. 4, pp. 309-310, Feb. 1991.

[BMOK92] A. W. Buchwald and K.W. Martin, A. Oki, and K. Kobayashi. "A 6-GHz integrated phase-locked loop using AlGaAs/GaAs hetrojunction bipolar transistors," *IEEE J. Solid-State Circuits,* vol. 27, pp. 1752-1761, Dec. 1992.

[BES98] J. N. Burghartz, D. Edelstein, M. Souyer, H. Ainspan, K. Jenkins, "RF circuit design aspects of spiral inductors on silicon," in *ISSCC Dig. Tech. Papers*, pp. 246-247, 1998.

[BSJ96] J. N. Burghartz, M. Souyer, and K. A. Jenkins, "Microwave inductors and capacitors in standard multilevel interconnect silicon technology," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 100-104, Jan. 1996.

[CAG93] J. Y. C. Chang, A. A. Abidi and M. Gaitan, "Large suspended inductors on silicon and their use in a 2-um CMOS RF amplifier," *IEEE Electron Device Lett.*, vol. 14, pp. 246-248, May 1993.

[CWC92] T. S. Cheung, H. Wong and Y. C. Cheng, "250MHz NMOS relaxation oscillator with enhanced linear voltage frequency characteristic and temperature stability," *Electron. Lett.*, vol. 28, no. 20, pp. 1917-1919, Sept. 1992.

[CrSt95] J. Craninckx and M. Steyaert, "A CMOS 1.8 GHz low phase noise voltage congtrilled oscillator with prescaler," in *ISSCC Dig. Tech. Papers*, pp. 266-267, Feb. 1995.

[CrSt97] J. Craninckx and M. Steyaert, "A 1.8 GHz low phase noise CMOS VCO using optimized hollow spiral inductor," *IEEE J. Solid-State Circuits,* vol. 32, pp. 736-744, May, 1997.

[Craw94] J. A. Crawford, Frequency Synthesizer Design Handbook, Artech House

Publishers, 1994.

[DLHH98] M. Danesh, J. R. Long, R. A. Hadaway and D. L. Harame, "A Q-factor enhancement technique for MMIC inductors," *IEEE MTT-S International Microwave Symposium, Baltimore,* USA, pp. 183-186, June 1998.

[DaMo74] M. B. Das and J. M. Moore. "Measurements and interpretation of low-frequency noise in FETS," *IEEE Trans. on Electron Devices,* vol. ED-21, pp. 247-257, April 1974.

[DaCo97] L. Dauphinee, M. Copeland, P. Schvan, "A balanced 1.5GHz voltage controlled oscillator with an intefrated LC resonator," in *ISSCC Dig. Tech. Papers*, pp. 390-391, Feb. 1997.

[DeJo83] B. T. Debney and J. S. Joshi, "A theory of nosie in GaAs FET microwave oscillators and its experimental verification," *IEEE Trans. on Electron Devices,* vol. ED-30, no. 7, pp. 769-775, July 1983.

[DeSa96] A. Demir and A. L. Sangiovanni-Vincentelli, "Simulation and modelling of phase noise in open-loop oscillators," *Proc. CICC*, pp. 453-456, 1996.

[DMR88] A. Demir, A. Mehrotra and J. Roychowdhury, "Phase noise and timing jitter in oscillators," *Proc. CICC*, pp. 45-48, 1998.

[DoJe94] L. Dobos and B. Jensen, "A versatile monolithic 800KHz to 800MHz phase-startable oscillator," *IEEE Custom Integrated Circuits Conf. Proceedings, (CICC).* 1994.

[Dong92] A. X. Dong, "Incorporation of digital angle-modulation into a fractional division synthesizer," M.Eng. Thesis, Carleton University, Ottawa, Canada, 1992

[EnAb86] S. K. Enam and A. Abidi, "A gigahertz voltage controlled ring oscillator,," *Electron. Lett.*, vol. 22, pp. 677-679, June, 1986.

[EnAb92] S. K. Enam and A. Abidi, "NMOS IC's for clock and data regeneration in Gigabit per second optical-fiber receivers," *IEEE J. Solid-State Circuits,* vol. 27, no. 12, pp. 763-1774, Dec. 1992.

[EnAb90] S. K.Enam and A. Abidi, "A 300-MHz CMOS voltage controlled ring oscillator," *IEEE J. Solid-State Circuits,* vol. 25, pp. 312-315, Feb. 1990.

[EsHo81] D. J. Esdale and M. J. Howes, "A refection coefficient approach to the design of one-port negative impedance oscillators," *IEEE Trans. Microwave Theory*

Tech., MTT-29, no. 8, pp. 770-776, Aug. 1981.

[FlLi92] M. P. Flynn and S. U. Lidholm, "A 1.2mm CMOS current-controlled oscillator," *IEEE J. Solid-State Circuits,* vol. 27, no. 7, pp. 982-987, July 1992.

[FoKw95] N. Foroudi and T. A. Kwasniewski, "CMOS high-speed CMOS dual-modulus frequency divider for RF frequency synthesis," *IEEE J. Solid-State Circuits*, vol. 30, no. 2, pp. 93-100, Feb. 1995.

[Fox93] R. M. Fox, "Comments on circuit models for MOSFET thermal noise," *IEEE J. Solid-State Circuits,* vol. 28, no. 2, pp. 184-185, Feb. 1993.

[Gard79] F. M. Gardner, Phaselock Techniques, second edition, New York: Wiley & Sons, 1979.

[Gard80] F. M. Gardner, "Charge-pump phase-lock loops," *IEEE Trans. Comm.*, vol. COM-28, pp. 1849-1858, Nov. 1980.

[Gard85] F. M. Gardner, "Properties of frequency difference detectors," *IEEE Trans. Comm.*, vol. COM-33, pp. 131-138, Feb. 1980.

[GrMe93] P. R. Gray and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, John Wiley & Sons, 1993.

[GrMe95] P. R. Gray and R. G. Meyer, "Future direction in silicon ICs for RF personal communications," *Proc. CICC*, pp. 83-90, 1995.

[Gre72] A. B. Grebene, Analog Integrated Circuit Design, Van Nostrand Reinhold, New York, 1972.

[Gre84] A. B. Grebene, Bipolar and MOS Analog Integrated Circuit Design, John Wiley and Sons, New York, 1984.

[GuSh96] R. X. Gu, K. M. Sharaf and M. I. Elmasry, "High-performance digital VLSI circuit design," Kluwer Academic Publishers, 1996.

[Hafn66] E. Hafner, "The effects of noise in oscilltors", *Proc. of the IEEE*, Feb. 1966.

[HaLe98] A. Hajimiri, T.H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits,* vol.33, no.2, pp.179-194, Feb. 1998.

[Has84] R. Hassun, "The common denominators in fractional N," *Microwaves and RF*, p.107, June 1984.

[HeRa98] F. Herzel and B. Razavi, "Oscillator jitter due to supply and substrate noise," *Proc. CICC*, pp. 489-492, May 1998.

[Hil86] M. D. Hill et al., "SPUR: Multiprocessor workstation," *IEEE Computer,* vol. 19, no. 10, pp. 8-24, Nov. 1986.

[HiSu92] A. Hill and J. Surber, "The PLL dead zone and how to avoid it," *RF Design,* pp. 131-134, March 1992.

[Hog85] C. R. Hogge, "A self-correcting clock recovery circuit," *IEEE J. Lightwave Technology,* vol. LT-3, pp. 1312-1314, Dec. 1985.

[HP88] Hewlett-Packard, Seminar notes, "RF & Phase Noise Measurement Seminar," 1988.

[HP89] Hewlett-Packard, User's Manual, "HP 3048A Phase Noise Measurement System", 1989.

[HP90] Hewlett-Packard, User's Manual, "HP 8590 Series Spectrum Analyzer", 1990.

[Huij96] J. H. Huijsing et al. (eds), Analog Circuit Design, pp.65-85, Kluwer Academic Publishers 1996.

[JaNe97] B. Jansen, K. Negus, D. Lee, "Silicon bipolar VCO family for 1.1 to 2.2 GHz with fully-integraed tank and tuning circuits," in *ISSCC Dig. Tech. Papers,* pp. 392-293, Feb. 1997.

[Jaq90] I. Jaquet, "A comparison of phase noise control techniques used in high resolution high-speed freqency synthesizers for mobile radio transceivers," M.Eng. Thesis, Carleton University, Ottawa, Canada, 1990.

[JBHK87] D. K. Jeong, G. Borriello, D. A. Hodges, R. H. Katz, "Design of PLL-based clock generator circuits," *IEEE J. Solid-State Circuits,* vol. 22, no. 4, pp. 255-261, April 1987.

[JCSC97] D. Jeong, S. Chai, W. Sing, G. Cho. "CMOS current controlled oscillators using multiple feeback loop ring architectures," in *ISSCC Dig. Tech. Papers,* pp. 386-387, 1997.

[Jind86] R. P. Jindal, "Hot-electon effects on channel thermal noise in fineline NMOS field-effect transistors," *IEEE Trans. Electron Devices,* vol. ED-33, pp. 1395-1397, Sept. 1986.

[JoMa97] D. A. John, K. Martin, Analog integrated circuit design, John Wiley & Sons, Inc. 1997.

[Kato88] K. Kato, et. al, "A low-power 128 MHz VCO for monolithic PLL IC's," *IEEE J. Solid-State Circuits,* vol. 23, no. 2, pp. 474-479, April 1988.

[KAPD96] V. Kaenel, D. Aebischer, C. Piguet, E. Dijkstra, "A 320 MHz, 1.5 mW at 1.35V CMOS PLL for microprocessor clock generation," in *ISSCC Dig. Tech. Papers*, pp. 132-133, 1996.

[KHG90] K. B. Kim, D. Helman, and P. Gray, "A 30-MHz hybrid analog-digital clock recovery circuit in 2um CMOS," *IEEE J. Solid-State Circuits,* vol. 25, pp. 1385-1394, Dec. 1990.

[King98] P. Kinget, "A fully integrated 2.7V 0.35um CMOS VCO for 5GHz wireless applications," *IEEE J. Solid-State Circuits*, pp. 226-227, Feb. 1998.

[Klie92] R. Klieber, et al, "A coplanar transmission line high-Tc superconductive oscillator at 6.5 GHz on a single substrate," *IEEE Microwave and Guided Wave Letters,* vol. 2, no. 1, pp. 22-24, Jan. 1992.

[Horo93] M. Korowitz, A. Chan, J. Cobrunson, J. Gasbarro, T. Lee, W. Leung, W. Richardson, T. Thrush, Y. Fujii, "PLL design for a 500 Mb/s interface," in *ISSCC Dig. Tech. Papers*, pp. 160-161, 1993.

[Krou82] V. F. Kroupa, "Noise properties of PLL systems," *IEEE Trans. Comm.*, Oct. 1982.

[KuHo91] K. Kurita, T.Hotta, T. Nakano and N. Kitamura, "PLL-based BiCMOS on-chip clock generator for very high-speed microprocessors", *IEEE J. Solid-State Circuits,* vol. 26, no. 4, pp. 585-589, April 1991.

[Kuro69] K. Kurokawa, "Some basic characteristics of broadband negative resistance oscillator circuits," *The Bell System Technical Journal,* July-August, pp. 1937-1977, 1969.

[KwAb95] T. Kwasniewski, M. Abou-Seido, A. Bouchet, F. Gaussorgues, J. Zimmerman, "Inductorless oscillator design for personal communications devices- A 1.2 um CMOS process case study," *Proc. CICC*, May 1995.

[Lar96] L. E. Larson (Editor), RF and microwave circuit design for wireless communication, Artech House Publishers, 1996.

[Lar97] L. E. Larson, "Integrated circuit technology options for RFIC's -present status and future directions," *Proc. CICC*, pp. 169-176, 1997.

[LaCa96] L. E. Larson, M. Case, S. Rosenbaum, D. Rensch, et. al., "Si/SiGe HBT technology for low-cost monolithic microwave integrated circuits," in *ISSCC Dig. Tech. Papers*, pp. 80-81, 1996.

[LeBu92] T. H. Lee, J.F. Bulzacchelli, "A 155MHz clock recovery delay and phase locked loop," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1736-1746, Dec. 1992

[Lee66] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proc. of IEEE*, vol. 54, pp. 329-330, Feb. 1966.

[LoCo97] J. R. Long, M.A. Copeland, "The modelling, characteriization, and design of monolithic inductors for silicon RF ICs," *IEEE J. Solid-State Circuits*, vol. 32, pp. 357-369, March 1997.

[Magu95] M. K. Maguire, "The design of a high-frequency voltage-controlled oscillator in BiCMOS using on-chip inductors," M.Eng. Thesis, Carleton University, Ottawa, Canada, 1995.

[Mali95] L. Maliniak, "RF simulator overcomes speed, capacity obstacles," *Electronic Design*, April. 1995.

[Mana76] V. Manassewitch, Frequency Synthesizer Theory and Design, New York: Wiley &Sons, 1976.

[MaHo93] J. G. Maneatis, M. A. Horowitz, "Precise delay generation using coupled oscillators," *IEEE J. Solid-State Circuits*, vol. 28, no. 12 pp. 1273-1282, dec 1993.

[Mane96] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1723-1732, Nov. 1996.

[Mart92] L. Martin, "Program optimizes PLL phase noise performance," *Microwaves & RF*, pp. 78-91, April 1992.

[McN94] J. McNeil, "Jitter in ring oscillators," *Proc. IEEE Int. Symp. Circuits and Syst. (ISCAS)*, 1994.

[MZN90] G. Moon, M. Zaghloul and R. Newcomb, "An enhancement-mode voltage-controlled linear resistor with large dynamic range," IEEE Trans. Circuit Syst., vol. 37, p.1287, Oct. 1990.

[Neg94] K. Negus, et. al., "A highly integrated transmitter IC with monolithic narrow-

band tuning for digital cellular handsets," in *ISSCC Dig. Tech. Papers*. 1993.

[NiMe98] A. M. Niknejad and R. G. Meyer, "Analysis, design and optimization of spiral inductors and transformers for Si RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1470-1481, Oct. 1998.

[Novo95] I. Novof, J. Austin, R. Kelkar, D. Strayer, and S. Wyatt, "Fully integrated CMOS phase-locked loop with 15 to 240 MHz locking range and +/-50 ps jitter," in *ISSCC Dig. Tech. Papers*, pp. 112-113, Feb. 1995.

[NyMe92] N. M. Nyuyen and R. G. Meyer, "A 1.8GHz monolithic LC voltage-controlled oscillator," *IEEE J. Solid-State Circuits*, vol. 27, pp. 444-450, March 1992.

[PaAl99] B. H. Park, P. E. Allen, "Low-power, low-phase-noise CMOS voltage-controlled oscillator with integrated LC resonator," *Proc. IEEE Int. Symp. Circuits and Syst. (ISCAS)*, 1998.

[Parz88] B. Parzen, "Classification and a generalized restatement of Lesson's oscillator noise model," *42nd Annual Frequency Control Symposium*, 1988.

[RaSu94] B. Razavi and J. J. Sung, "A 6 GHz 60mW BiCMOS phase-locked loop," *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1560-1565, Dec. 1994.

[RaSu95] B. Razavi and J. J. Sung, "A 2.5 Gb/s 15mW BiCMOS clock recovery circuits," *Symposium on VLSI Circ*, Dig. of Tech. Papers, pp. 83-44, 1995.

[Raz961] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, pp. 331-343, March 1996.

[Raz962] B. Razavi (Editor), "Monolithic phase-locked loops and clock recovery circuits, Theory and design," IEEE Press 1996.

[Raz971] B. Razavi, "A 1.8GHz CMOS voltage-controlled oscillator," in *ISSCC Dig. Tech. Papers*, pp. 388-389, Feb. 1997.

[Raz972] B. Razavi, "Challenges in the design of freuency synthesizers for wireless applications," *Proc. CICC*, pp. 395-402, May 1997.

[Raz98] B. Razavi, "CMOS technology characterization for analog and RF design," *Proc. CICC*, pp. 23-30, May 1998.

[Reyn94] D. Reynolds, "A 320-MHz CMOS triple 8-bit DAC with on-chip PLL and hardware cursor," *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1545-

1551, Dec. 1994.

[Rhe95] R. W. Rhea, Oscillator Design and Computer Simulation, Noble Publishing, 1995.

[Rho83] W. L. Rhode, Digital PLL Frequency Synthesizers, Theory and Design, Prentice-Hall, 1983.

[RCK93] T. A. D. Riley, M. A. Copeland and T. A. Kwsniewskiy, "Sigma-Delta modulation in fractional-N frequency synthesis," *IEEE J. Solid-State Circuits*, vol. 28, pp. 553-559, May 1993.

[Rob95] I. D. Robertson (Editor), MMIC design, IEE Press, 1995.

[Robi91] W. P. Robins, Phase Noise in Signal Sources, IEE Press, 1991.

[Rofo96] A. Rofougaran, J. Rael, M. Rogougaran, and A. A. Abidil, "A 900 MHz CMOS LC oscillator with quadrature outputs," in *ISSCC Dig. Tech. Papers*, pp. 390-392, Feb. 1996.

[RFHF93] R. Rogenmoser, N. Felber, Q. Huang and W. Fichtner, "1.16 GHz dual-modulus 1.2um CMOS prescalers," *Proc. CICC*, May 1993.

[RHP94] R. Rogenmoser, Q. Huang and E. Piazza, "1.57 GHz asynchronous 1.4 GHz dual-modulus 1.2um CMOS prescalers", *Proc. CICC*, May 1994.

[Rut78] J. Rutman, "Characterization of phase and frequency instabilities in precision frequency sources, Fifteen years of progress," *Proc. of IEEE*, vol. 66, pp. 1048-1174, Sept. 1978.

[Sauv77] G. Sauvage, "Phase noise in oscillators: A mathematical analysis of Lesson's model," *IEEE Trans. Instrumen. Measurement*, vol. IM-26, no. 4, pp. 408-410, Dec. 1977.

[SeSm91] A. S. Sedra, K. C. Smith, Microelectronic Circuits, Third Edition, Oxford University Press, 1991.

[ShKw97] K. M. Sheikh and T. A. Kwasniewski, "CMOS low-power microwave frequency prescalers for wireless applications," *IEEE Canadian Conference* May, 1997, Newfoundland

[Smi86] J. Smith, Modern Communication Circuits, McGraw-Hill Inc., 1986.

[SnVe90] J. G. Sneep and C. J. M. Verhoeven, "A new low-noise 100MHz balanced relaxation oscillator," *IEEE J. Solid-State Circuits*, vol. SC-25, no. 3, pp.

692-698, 1990.

[Snel] W. M. Snelgrove, "VLSI Circuits," course note

[SoMe89] M. Soyuer and R. G. Meyer, "High-frequency phase-locked loops in monolithic bipolar technology," *IEEE J. Solid-State Circuits,* vol. 24, pp. 787-795, June 1989.

[SoWa92] M. Soyuer and J. D. Warnock, "Multigigahertz voltage-controlled oscillators in advanced silicon bipolar technology," *IEEE J. Solid-State Circuits,* vol. 27, pp. 668-670, April 1992.

[Soyu96] M. Soyuer, et al, "A 2.4 GHz silicon bipolar oscillator with integrated resonator," *IEEE J. Solid-State Circuit,* vol. 31, no. 12, pp. 268-270, Feb. 1996.

[SoJe95] M. Soyuer, K. A. Jenkins, J. N. Burghartz and M.D. Hulvey, "A 3V 4GHz nMOS voltage-controlled oscillator with integrated resonator," *IEEE J. Solid-State Circuits,* vol. 31, pp. 2042-2045, Dec. 1996.

[Stra70] L. Strauss, Wave Generation and Shaping, 2nd ed,, McGraw-Hill, New York, 1970, Chap. 16.

[Sun97] L. Sun, "Research proposal for Ph.D. Dissertation in high speed monolithic frequency synthesizers" Carleton Univeristy, May 1997.

[SuKw97] L. Sun, T. Kwasniewski, "Current monolithic VCO implementations for wireless applications," Wireless'97, July Calgary

[SKI99] L. Sun, T. Kwasniewski and K. Iniewski, "A Quadrature Output Voltage Controlled Ring Oscillator Based on Three-Stage Sub-feedback Loops," *Proc. IEEE Int. Symp. Circuits and Syst. (ISCAS),* June 1999.

[SuKw991] L. Sun, T. Lepley, F. Nozahic, A. Bellissant, T. Kwasniewski and B. Heim, "Reduced Complexity, High Performance Digital Delta-Sigma Modulator for Fractional-N Frequency Synthesis," *Proc. IEEE Int. Symp. Circuits and Syst. (ISCAS),* June 1999.

[SuKw992] L. Sun, T. Kwasniewski, "A 1.25GHz 0.35um monolithic CMOS PLL clock generator for data communications," *Proc. CICC,* May 1999.

[SuYi90] L. Sun, P. Yip, "Optical homodyne receiver based on an improved balance phase-locked loop with the data-to-phaselock crosstalk suppression," *IEEE Photon. Tech. Lett.* vol. 2, no. 9, pp. 678-679, Sept. 1990.

[SuYi91] L. Sun, P. Yip, "Optical phase locked-loop homodyne receiver using an eight-port 90° optical hybrid," *Optical and Quantum Electronics,* vol. 23, pp. 461-467, 1991.

[SuBo92] L. Sun, J. Bornemann, "Envelope detection of vestigial sideband TV signal with carrier reinsertion," *IEEE Trans. Consum. Electron.*, vol. 38, no. 1, pp. 1-4, 1992.

[TSW94] S. Tedja, J. Van der Spiegel, and H. H. Williams, "Analytical and experimental studies of thermal noise in MOSFET's," *IEEE Trans. Electron Devices,* vol. ED-41, pp. 2067-2075, Nov. 1994.

[Tham93] M. Thamsirianunt, "The design and implementation of CMOS components for gigahertz frequency synthesizer," M.Eng. Thesis, Carleton University, Ottawa, Canada, 1993.

[ThKw951] M. Thamsirisanunt and T. A. Kwasniewski, "CMOS VCOs for PLL frequency synthesis in GHz digital mobile radio communications," *Proc. CICC,* 1995.

[ThKw952] M. Thamsirisanunt and T. A. Kwasniewski, "A 1.2 um CMOS impremention of a low power 900 MHz mobile radio frequency synthesizer," *Proc. CICC,* 1995.

[Tsiv87] Y. P. Tsividis, Operation and Modeling of MOS Transistor, New York: McGraw_Hill, 1987.

[Van86] A. van der Ziel, Noise in Solid State Devices and Circuits. New York: Wiley, 1986.

[VePa90] G. D. Vendelin, A. M. Pavio, U. L. Rohde, Microwave Circuit Design Using Linear and Nonlinear Techniques, John Wiley & Sons, 1990.

[Ver92] C. J. M. Verhoeven, "A high-frequency electronically tunable quadrature oscillator," *IEEE J. Solid-State Circuits,* vol. 27, no. 7, pp. 1097-1100, July 1992.

[VeSt96] C. J. M. Verhoeven, A. van Staveren, J. R. Westra, A. H. M. van Roermund, "Low-noise oscillators," J.H. Huijsing et al. (eds), Analog Circuit Design, pp. 65-85, Kluwer Academic Publishers 1996.

[WaAb87] M. H. Wakayama and A. A. Abidi, "A 30-MHz low-jitter high-linearity

CMOS voltage-controlled oscillator", *IEEE J. Solid-State Circuit,* vol. 22, pp. 1074-1081, Dec. 1987.

[WHS92] B. Wang, J. R. Hellums and C. G. Sodini, "MOSFET thermal noise modeling for analog integrated circuits," *IEEE J. Solid-State Circuits,* vol. 27, pp. 1444-1447, Oct. 1992.

[Wan98] C. Wann, L. Su, K. Jenkins, R. Chang, D. Frank, Y. Taur, "RF perspective of sub-tenth micron CMOS," in *ISSCC Dig. Tech. Papers*, pp. 254-255, 1998.

[WLS89] K. Ware, H. Lee and C. Sodini, "A 200MHz CMOS PLL with dual phase detectors," *IEEE J. Solid-State Circuits,* vol. 24 , pp. 1560-1568, Dec. 1989.

[WKG94] T. C. Weigandt, B. Kim and P. R. Gray, "Analysis of timing jitter in CMOS ring oscillators," *Proc. IEEE Int. Symp. Circuits and Syst. (ISCAS),* 1994.

[WeEs93] N. H. E. Weste, K. Eshraghian, Principle of CMOS VLSI Design, second edition, Addison Wesley, 1993.

[Whea83] C. E. Wheatley, "Digital frequency synthesizer with random jittering for reducing descrete spetral spurs," US patent 4,410,954, Oct, 1983.

[Wol91] D. H. Wolaver, Phase-Locked Loop Circuit Design, Prentice Hall 1991.

[Yama92] Y. Yamauchi et al., "A 15-GHz monolithic low-phase-noise VCO Using AlGaAs/GaAs HBT technology," *IEEE J. Solid-State Circuits,* vol. 27, no. 9, pp. 1444-1447, Oct. 1992.

[YGW92] I. A. Young, J. K. Greason and K. L. Wong, "A PLL clock generator with 5 to 110MHz of lock range for microprocessors," *IEEE J. Solid-State Circuits,* vol. 27, pp. 1599-1607, Nov. 1992.

[YKS87] J. Yuan, I. Karlsson and C. Svensson, "A true single phase-clock dynamic CMOS circuit technique," *IEEE J. Solid-State Circuits,* vol. 22, pp. 899-901, Oct. 1987.

[YLC97] H. Yang, L. Lee, and R. Co, "A low jitter 0.3-165 MHz CMOS PLL frequency synthesizer for 3 V/5 V operation," *IEEE J. Solid-State Circuits,* vol. 32, pp. 582-586, April. 1997.

[YuSv89] J. Yuan, C. Svensson, "High-speed CMOS circuit technique," *IEEE J. Solid-State Circuits,* vol. 24, pp. 62-70, Feb. 1989.

[YuWo97] P. Yue and S. Wong, "On-chip spiral inductors with patterned ground shields

for Si-based RFIC's," *VLSI Circuits Symposium Digest of Technical Papers*, June 1997.

[ZDL96] Z. Zhang, H. Du, M. Lee, "A 360 MHz 3 V CMOS PLL with 1V peak-to peak power supply noise tolerence," in *ISSCC Dig. Tech. Papers*, pp. 134-135, 1996.