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Threshold Voltage Control By Backgating In Fully Depleted SOI CMOS

by

Yanbin Wang, M.Sc., McGill

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Ottawa-Carleton Institute for Electrical Engineering,
Department of Electronics,
Carleton University,
Ottawa, Ontario, Canada

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Abstract

Fully-depleted SOI MOSFETs with junction-isolated backgate electrodes formed by implanting boron through the silicon film and buried oxide into lightly-doped n-type SIMOX substrates have been studied experimentally and through numerical device simulation. By biasing the backgate electrode, it is possible to adjust the MOSFET threshold voltage V_{th}. The useful range of V_{th} adjustment is shown to be approximately $\pm$ 200 mV for typical structures, irrespective of silicon film or buried oxide thickness, and is limited primarily by accumulation or inversion of the back surface of the silicon film for extreme values of backgate bias. A secondary limitation on V_{th} adjustment range results from enhancement of short-channel effects when the silicon film back surface begins to weakly invert. A complete dynamic V_{th} control system using charge pumping to supply bias to the back-gate electrode has been designed and laid out. SOISPICE simulation of the extracted layout predicts that the system can return V_{th} for n-channel MOSFETs to a nominal value of 200 mV even if V_{th} initially deviates by up to $\pm$300 mV from this target. Similar results apply to p-channel devices. The layouts have been submitted for processing in Carleton's Microelectronics Fabrication Facility.

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CHAPTER 1

Introduction

Low voltage CMOS has found wide application in the microelectronics industry. The new technology of Fully-Depleted Silicon On Insulator (FD-SOI) MOSFET is shown in many respects to be ideal for 1 Volt power supply operation. Firstly, in this technology the source-drain junction leakage current in SOI-MOSFETs is eliminated. Secondly, since the capacitance between the source and drain junctions and the substrate is greatly reduced, the energy dissipated during switching is substantially decreased. Finally, FD-SOI MOSFETs have subthreshold swing (S) close to the theoretical minimum of 60 mV/decade at room temperature, Thus the threshold voltage (V_{th}) can be reduced without introducing excessive channel leakage.

The threshold voltage V_{th} of a SOI-MOSFET is critical to the performance of the device. However, due to variations in temperature or process parameters, the threshold voltage V_{th} may fluctuate by as much as $\pm$300 mV from its desired value, which is ~ 200 mV in a low voltage FD-SOI integrated circuit. Dynamic control of the threshold voltage is thus highly desirable.

Dynamical control of V_{th} has been used for many years in bulk CMOS. Burr *et al.* [1] proposed a novel approach to low-power bulk CMOS in which threshold voltages are controlled dynamically by applying a back-gate bias to the wells in which the MOSFETs are built. Yang *et al.* [2][3] extended this technique to fully-depleted SOI CMOS by placing an oxide-isolated back-gate electrode beneath the channel. However, this structure is based on complex wafer bonding and etch-back techniques and appears to be difficult to manufacture. Chang *et al.* [4] used epitaxial lateral over-

growth (ELO) onto SOI islands to fabricate fully depleted dual-gated (DG) thin film SOI-MOSFETs. This allows independent operation of both top-gate and back-gate electrodes, and leaves the back-gate buried and totally isolated from all other devices. This also provides a method to control the threshold voltage of the MOSFET with a bias on the backgate ($V_{G,back}$) for fully depleted devices. Recently, it has been shown that by constructing a junction-isolated implanted back-gate electrode under the buried oxide, the threshold voltage V_{th} can also be dynamically controlled [5][6]. The implanted back-gate structure is far simpler to manufacture than the alternatives mentioned above.

This thesis describes SUPREM3 simulation and measurements on experimental devices fabricated in earlier work to investigate the range of threshold voltage control which can be achieved with the implanted back-gate structure. The scalability of the structure from the 1 μm technology generation to the 0.25 μm generation is also considered using numerical simulations. The thesis goes on to describe the design and simulation of a dynamic threshold voltage control system for FD-SOI MOSFETs using the implanted back-gate structure. The system includes a decision circuit which determines whether the threshold voltage lies within an acceptable range, and charge pump circuits which supply positive or negative bias to the back-gate for restoration of V_{th} to the desired value. The charge pumps can produce voltages much larger than the supply voltage, an important feature if the control system is to operate from 1 V supplies. The control system operation is studied through SOISPICE simulation, and complete layouts for n- and p-channel MOSFETs are given. These layouts have been submitted to Carleton's Microelectronics Fabrication Facility for processing.

The thesis is organized as follows. Chapter 2 reviews the background of low power CMOS and SOI-MOSFET, its threshold voltage and usefulness in low voltage circuits. Chapter 3 discussed the device simulating results. The circuit description and simulation results are presented in Chapter 4 where the choice of the charge pump circuit is discussed. Also in Chapter 4 the device layout and fabrication is briefly discussed. Chapter 5 presents the device electrical characterization results follow by the discussion. At last, Chapter 6 presents the conclusions as well as suggestions for further study.

CHAPTER 2

Background

The development of low power electronics has been motivated by three reasonably distinct requirements.The earliest and most demanding of these is for portable battery operated equipment that is sufficiently small in size and weight and long on operating life to satisfy the user. The ever increasing packing density in ULSI chips required to enhance the speed of high performance systems, imposes severe restrictions on power dissipation density. The broadest requirement is for conservation of power in desk-top and desk-side systems where a competitive life cycle cost-to-performance ratio demands low power operation to reduce power supply and cooling costs.

There are two main reasons for interest in low voltage VLSI CMOS. One reason is to reduce the electric field inside MOSFETs and to maintain high reliability with scaled down devices. The other reason is to reduce the power consumption, which is proportional to V_{DD}^2. It has been clarified in Kakumu's work [7] that reduction of the threshold voltage and junction capacitance are key issues for low voltage operation of CMOS device. Kakumu also investigated the optimum power-supply voltage for CMOS devices. The upper limit of power-supply voltage is determined by both reliability and power dissipation problems. He showed that the upper limit is proportional to $L^{1/2}$ for reliability considerations and proportional to $L^{3/4}$ for the power dissipation case, where L is the channel length. The lower limit is determined by the circuit performance point due to the monotonic decrease of the delay time as the power-supply voltage increases. Even if power supply voltage greater than a critical voltage V_C is applied, the improvement in the delay time is not significant. Thus this V_C value is regarded as the lower limit of the power-supply voltage for CMOS devices:

$$V_C = 0.87 \cdot E_C \cdot L_{eff} + V_{th} \tag{2.1}$$

where E_C is the critical electric field at which carrier velocity is saturated and L_{eff} is the effective channel length of the transistor. An optimum power-supply voltage is therefore chosen considering the long-term device reliability, power dissipation and circuit performance.

Subthreshold leakage plays an important role in determining the power supply and threshold voltages in MOS circuits. The subthreshold slope of a MOS device is a figure of merit that describes the gate voltage swing required to change the drain current by one order of magnitude. Specifically, $S = \Delta V_G / \Delta \log_{10} I_D$. If, for example, we have a device with a subthreshold swing of 90 mV/decade and the stand-by current is to be 10^{-7} times the current at threshold, then the threshold voltage of the transistor must be at least 0.63 volts. By definition, the subthreshold slope is measured below the threshold voltage of the particular device when the semiconductor surface is in a state of weak inversion. For a bulk device, the subthreshold slope is given by:

$$S = \left(\frac{kT}{q}\right) \ln\left(10 \cdot \left(1 + \frac{C_D}{C_{OX}}\right)\right) \tag{2.2}$$

where C_D is the depletion capacitance in the silicon at the onset of weak inversion. The subthreshold characteristics of a partially depleted thin film transistor will be similar to those of a bulk device because the maximum depletion capacitance associated with the surface potential will be supported by the silicon film. A thin film fully depleted transistor can, however, offer a significant reduction in S.

It has been shown that as the threshold voltage approaches one half of V_{DD}, the gate delay increases rapidly due to drastic reduction of the MOSFET's current. As a result, the threshold voltage should

be less than 20% of power supply voltage, in order to maintain acceptable circuit performance even at reduced power supply voltage. The subthreshold leakage current when gate bias is less than the threshold voltage is defined as the drain current at V_G=0 (Fig. 2.1). When the threshold voltage is lowered as far as possible, to improve circuit performance, the leakage current is inevitably increased. This is because it is difficult to improve the subthreshold slope by adjusting device parameters only. However, if the threshold voltage cannot be reduced in the future MOS device, then the upper limit of the power-supply voltage cannot be reduced. Finally, The threshold voltage will become higher than the lower limit of power-supply voltage. Therefore, a steeper subthreshold slope is required for the reduction of the lower voltage limit in order to keep the same subthreshold leakage.

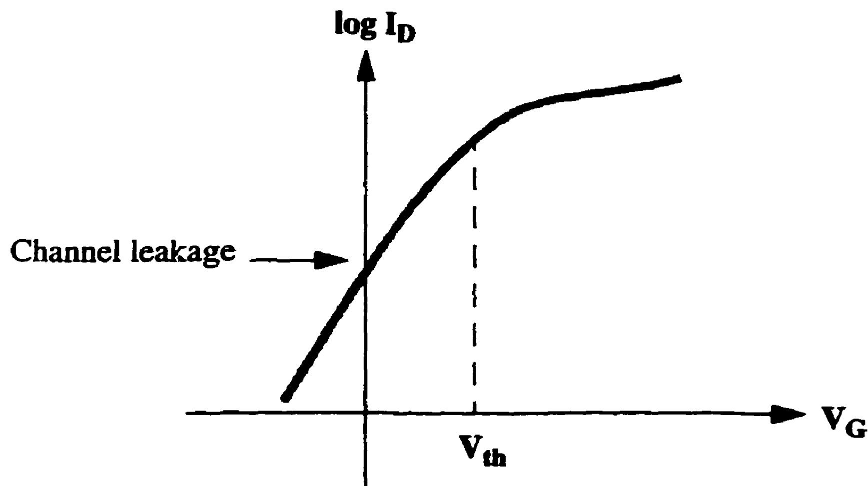


Fig. 2.1 A diagram that displays the subthreshold leakage current.

Parasitic capacitance such as junction capacitance, gate capacitance and wiring capacitance play an important role in the performance of bulk CMOS. The junction capacitance is inversely proportional to the square root of the drain voltage, while the gate capacitance and the wiring capacitance are independent of operating voltage. Therefore, the junction capacitance increases as operating voltage is decreased. Since the junction capacitance may become the dominant factor as the power sup-

ply voltage is reduced, reduction of the junction capacitance is a key issue for achieving high circuit performance at low-voltage operation.

Silicon on insulator (SOI) CMOS technology, discussed in the next section, offers a means of reducing both parasitic capacitance and subthreshold swing.

2•1 SOI -MOSFET

The SOI MOSFET can provide steep subthreshold characteristics and a drastic decrease in the source-drain capacitance and thus high speed capability in addition to complete latch-up suppression, and radiation hardness. SOI CMOS can also provide much closer packing of p- and n-transistors by eliminating the need to grow a thick field oxide.

It is also reported [8] that very thin film SOI technology shows very attractive MOSFET characteristics such as very steep subthreshold characteristics, better short channel effect and high carrier mobility owing to low transverse electric field. In the fully depleted MOSFET in the SOI structure, the depletion layer reaches the SiO_2 substrate interface, and thus the differential depletion capacitance C_D vanishes. As a result, the subthreshold swing approaches the theoretical limit, 60 mV/decade at room temperature, which enables a lower threshold voltage to be used. In addition, the large reduction of junction capacitance leads to improved circuit performance and a very low power-delay product, which should be superior to those of bulk-CMOS devices.

In the SOI process a thin layer of single-crystal silicon film is formed on an insulating layer of SiO_2 that has been in turn grown on silicon. The idea is based on the use of an inexpensive and readily

available substrate. Various masking and doping techniques are then used to form p-channel and n-channel devices. Several techniques such as Separation by IMplanted Oxygen (SIMOX) [9], Zone Melt Recrystallization (ZMR) [10], epitaxial/polishing process [11] and bonding wafer [12] are available, all providing a good quality SOI wafer with mobility comparable to that of bulk CMOS. SIMOX is currently the most commonly used technique for SOI substrate preparation.

The steps used in typical SOI-CMOS process are as follows:

- A thin film (< 100 nm) of very lightly-doped Si is formed over an insulator.
- Device wells are formed by mesa etching or by a LOCOS process in which the silicon film in the field region is completely consumed.
- The p-islands are formed next by Boron implantation through a photoresist mask. The p-islands will contain the n-channel devices.
- The p-islands are then covered with a photoresist and an n-type dopant--Phosphorus, for example, is implanted to form n-islands which will contain the p-channel devices.
- A thin gate oxide is grown.
- A polysilicon film is deposited over the oxide. In modern SOI technology, poly is usually undoped.
- The polysilicon film is then patterned by photomasking and is etched. This defines the critical polysilicon gate layer in the structure.
- The next step is to form the n-doped source and drain of the n-channel devices in the p-islands. The n-islands are covered with photoresist and an n-type dopant, normally arsenic, is implanted. The dopant will be blocked at the n-islands by the photoresist, and it will be blocked from the gate region of the p-islands by the polysilicon. After this step the n-channel devices are com-

plete.

- The p-channel devices are formed next by masking the p-islands and implanting a p-type dopant such as boron. The polysilicon over the gate of the n-islands will block the dopant from the gate, thus forming the p-channel devices.
- A layer of borophosphosilicate glass is the deposited over the entire structure.
- The glass is etched at contact-cut locations. The metallization layer is formed next by evaporating aluminium over the entire surface and etching it to leave only the desired metal wires. The aluminium will flow through the contact cuts to make contact with the diffusion or polysilicon regions.

A final passivation layer of phosphorus glass is deposited and windows are etched through this layer over the bonding pads.

Although SOI devices have a number of advantages over bulk CMOS, SOI MOSFET characteristics are strongly dependent upon film quality and thickness controllability of the thin silicon layer. For instance, the threshold voltage of the fully depleted MOSFEET is a function of both the SOI thickness and the backside Si-SiO_2 interface charges. Furthermore, in order to suppress short-channel effect, film thickness of less than 50 nm is required for below quarter micron channel length. However, the thinner Si film results in higher source/drain sheet resistance, which is not desirable for high speed operation. Therefore, technological improvement is still required.

2•2 Threshold Voltage Of Thin Film SOI MOSFET

Threshold voltage of a bulk transistor is normally described by the classic relation as:

$$V_{th} = V_{FB} + 2\phi_B - \frac{Q_D}{C_{OX}} \qquad (2.3)$$

where V_{FB} is the flat band voltage, ϕ_B is the bulk (substrate) potential, Q_D is the space charge density in the depletion region, and C_{OX} is the gate oxide capacitance. In the case of a thin film transistor in which the silicon film thickness is greater than the gate-induced spaced charge layer, there will be a charge neutral region within the silicon film. This is the case of a partially depleted device. It is expected that this device has a similar threshold characteristic as described in eq. (2.3).

For thin films that are fully depleted, the doping concentration must be much greater than that of the silicon substrate in order to overcome the ϕ_{ms} term in eq. (2.3). The back interface of the silicon film is assumed to be at or very near flat band with respect to the substrate, since the majority of the band bending due to the substrate/silicon film work function difference will appear in the lightly doped substrate. If the silicon film thickness is less than that of the gate induced depletion layer, there will be no neutral region in the film. Under these conditions, the silicon film is fully depleted. The depletion charge is no longer determined by the total band bending at the front surface of the film but is now limited by the thickness of the silicon film. The threshold voltage of the fully depleted silicon film should therefore be smaller than that of a comparable bulk or partially depleted device with the same well doping.

It can be shown that the threshold voltage for the fully depleted case is given by [13]:

$$V_{th} = (1+\alpha)(V_{FB}+2\phi_B) - q\frac{N_A t_{si}}{\alpha C_{OX}} - q\frac{N_A t_{si}}{2Csi} \quad (2.4)$$

where $\alpha = \frac{C_{box}C_{si}}{C_{ox}(C_{box}+C_{si})}$, C_{box} is the capacitance of the buried oxide, C_{si} is the capacitance of the fully depleted silicon film, N_A is the acceptor concentration, and t_{si} is the silicon film thickness. Since α is small, the threshold voltage varies approximately linearly with the film thickness for a fixed and uniform doping. In the limit of the film thickness tending to zero, the threshold voltage of the film is independent of the film doping.

If the silicon film is fully depleted at the onset of weak inversion, then the capacitance associated with the depleted region will consist of the buried oxide capacitance in series with the depleted film capacitance. The capacitance due to the space charge layer in the substrate can be ignored. The subthreshold slope is now given for a FD silicon film as:

$$S = \left(\frac{kT}{q}\right)\ln 10 \cdot (1+\alpha) \quad (2.5)$$

If the film is sufficiently thin so that it is fully depleted well below threshold, then the value of S observed is indeed quite low, on the order of 62 to 75 mV/decade for n-channel and p-channel devices.

2•3 Methods Of Controlling Threshold Voltage

In order to achieve high performance and low power in continuously computing systems (e.g., modules of a video compression system), reduction of supply voltage V_{DD} and threshold voltage V_{th} is required. For technology generations with gate length less than 1 μm, the saturation drain

current $I_{D,SAT}$ is approximately proportional to (V_{DD} - V_{th}). A small V_{th} is preferred to give a high $I_{D,SAT}$ when V_{DD} is small. However, a small subthreshold leakage current (shown in Fig. 2.1) requires a high V_{th}. A trade off should be made to find optimal V_{DD} and V_{th} values [14][15][16]. CMOS-based high performance burst-mode computation systems (e.g. a microprocessor running an X server or cellular phone which is idling more than 90% of the time) will suffer high-static leakage energy dissipation operating at low V_{DD} with constant low V_{th} even with clocks stopped [17]. In order to simultaneously achieve high performance during active periods and low leakage power during idle periods for burst-mode computational systems, several schemes of reducing the leakage current have been proposed. One is multiple V_{th} CMOS design which uses high V_{th} transistors to gate the low V_{th} blocks [18][19]. Another approach is dynamic control of V_{th} by biasing the bulk CMOS wells [20].

The idea of making use of a substrate bias effect to control threshold voltage has been known since at least 1976 [21]. The main objective of the paper was to reduce short-channel effects. Two external reference voltages were needed to operate the circuit. Much more recently, Kobayashi *et al.* introduced a circuit technique to reduce the threshold voltage fluctuation due to process variation [22]. The technique uses substrate self-biasing, namely the Self-Adjusting Threshold-Voltage Scheme (SATS) which consists of a leakage sensor and a self-substrate bias circuit. The substrate bias is controlled with a feed back loop so that leakage current of a MOSFFET is held constant. Fig. 2.2 shows a block diagram of the proposed scheme to reduce the V_{th} fluctuation down to ± 0.05 V. A leakage sensor senses leakage current of a representative MOSFET and outputs a control signal, V_{cont}, to the Self-Substrate-Bias (SSB) circuit. Assuming we are dealing with NMOSFETs, the triggered SSB draws charge from P-wells of NMOSFETs and lowers the substrate voltage, V_{BB},

and the lowered V_{BB} in turn increases V_{th} and lowers leakage current. Here the V_{BB} is distributed to all other NMOSFETs on the chip.

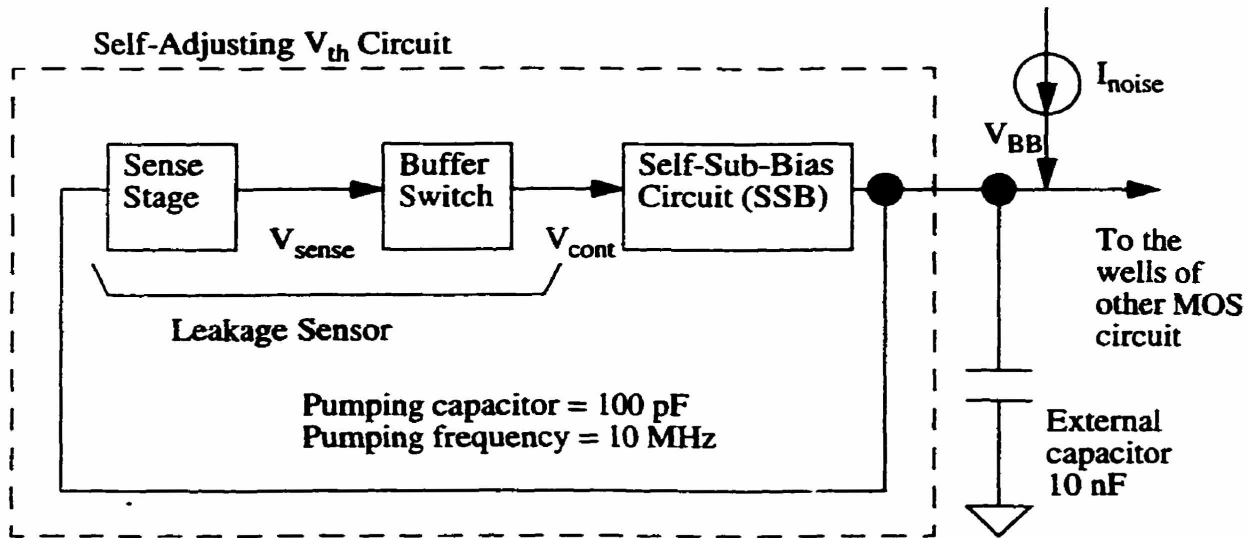


Fig. 2.2 Block diagram of Self-adjusting V_{th} Scheme (SATS) [22].

It is shown in [22] that the sub-threshold leakage current I_D has an exponential dependence on V_{th} written as $I_D \sim \exp[(V_{GS}-V_{th})/S]$ where S is the subthreshold swing with a value close to 110 mV/decade when V_{BS} is zero, dropping to 90 mV/decade when V_{BS} is less than -1V. This suggests that with the substrate-bias, V_{th} can be set lower than in the case without the substrate-bias while maintaining the leakage current. Thus, V_{th} is controlled to make the leakage current equal to the specified value, that is, V_{th} is set to the lowest possible value while satisfying the power specification. Consequently, the speed is optimized. Substrate bias is also good for reducing junction capacitance to further improve performance. The process target for V_{th} should be low enough so that the SSB can tune V_{th} to whatever value is necessary. Threshold voltages for PMOSFETs are controlled in the same way at the same time. The threshold voltage is reported to be controlled within $\pm$ 0.05 V and the speed gains for1.5 V and 1 V V_{DD} operation are estimated to be a factor of 1.3 and 3, respectively.

In order to address the problem of exponential decrease in circuit performance as supply voltage approaches threshold voltage, Burr *et al.* used back bias of bulk CMOS to modify the transistors to have thresholds close to zero volts and then "tuning" these thresholds [1]. Their process features 230 A oxide, 2 μm drawn channel lengths, and surface-channel PMOSFETs. Devices with thresholds near 0V are produced without any process changes other than modifying threshold-shifting implant masks to exclude the low-voltage circuits. The device I-V curves show that both NMOSFETs and PMOSFETs have subthreshold swings close to 70 mV/decade. The effective channel dopant concentration is $5\times10^{15}/cm^3$ for the NMOSFETs and $10^{16}/cm^3$ for the PMOSFETs. The study found substantial decrease of power-delay product with only modest decrease in performance. It also supports a high degree of "voltage scalability", so with appropriate biases the same chip can run at supply voltages from 200 mV to 5 V.

2•4 V_{th} Control in FD-SOI MOSFET

There have been numerous studies on the merits of fully-depleted (FD) SOI in CMOS and its implications for low power electronics. Various researchers have exploit FD-SOI in dual-gated devices in which the top and bottom gates are tied together, resulting in enhanced transconductance [23][24][25][26]. For partially depleted device, it has also been demonstrated that the threshold voltage V_{th} can be controlled dynamically by tying the body to the gate [27]. The threshold voltage then drops as the gate voltage is raised, resulting in a much higher current drive than in a regular MOSFET at low V_{DD}. In addition, it is possible to make V_{th} high at zero bias, and thus the leakage current is guaranteed to be at low level.

Recently, another group developed a technology, silicon-on-insulator-with-active-substrate (SOI-AS), to fabricate back-gated FD CMOS device by combining on existing SIMOX, wafer bonding and thinning technologies [2][3]. A quite complicated process is required to prepare SOIAS, which is shown in Fig. 2.3. A multilayered blanket film stack consisting of the silicon wafer, oxide, intrinsic polysilicon, back-gate oxide, and silicon film is used as the substrate of SOIAS. These substrates were prepared using either bonded SIMOX or etched-back bulk wafers. For the bonded SIMOX process, the back-gate oxide to be was formed by dry oxidation and intrinsic amorphous silicon was deposited as the back-gate material. The handle wafer had an oxide/nitride stack. The SIMOX wafer was then bonded to the handle wafer, and annealed. After being etched to remove the bulk of the SIMOX wafer, the bonded wafers were then thinned by localized plasma etching to a thickness of approximately 0.2 μm. Final thinning of the silicon film was accomplished with thermal oxidation and wet oxide strip..

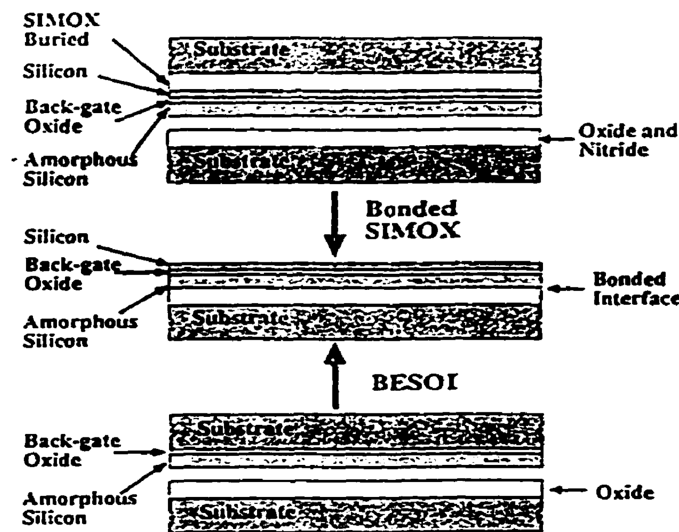


Fig. 2.3 SOIAS preparation using bonded SIMOX and BESOI process [2].

Forming of the back-gates includes ion implantation through the silicon film in two masking steps, resulting in islands of p^+ and n^+ polysilicon insulated by intrinsic poly. To set the zero back-gate bias value for the front-gate V_{th}, the silicon film was also doped. The same type of doping was applied in the back-gate poly and silicon film. The front-gate device is then built as in a conventional SOI CMOS process using LOCOS isolation. The back-gate controls the threshold voltage V_{th} of the front-gate device since the surface potentials at the front and back interfaces are coupled in FD-SOI devices. Fig. 2.4 shows the schematic of a SOIAS back-gated CMOS device. It is apparent that the NMOS and PMOS back-gates are switched independently from one other and the front-gate.

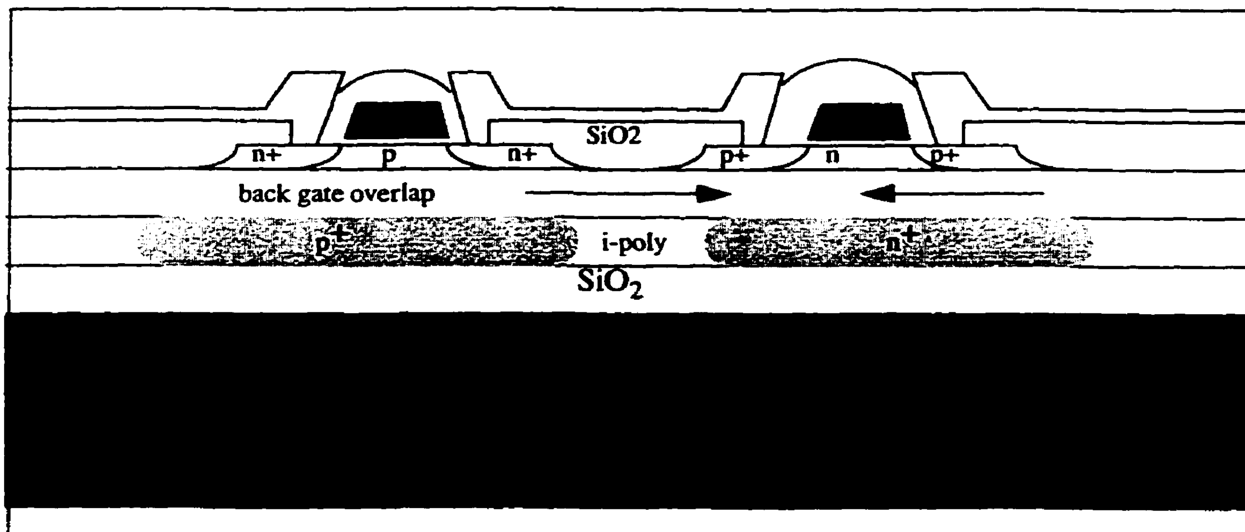


Fig. 2.4 SOIAS back-gated CMOS device schematic [2].

It is found that the tunable V_{th} range is quite large for fully depleted back interface as can be seen from the lowest V_{th} case at zero back-gate bias. This has implications for making FD SOI a viable technology since the threshold voltage and the device operating mode can be controlled precisely by the back-gate. Fig. 2.5 shows the maximum and minimum tunable V_{th} limits. The x-axis is nominally designed V_{th0} which is the threshold voltage at zero back-gate voltage. The y-axis, tunable

V_{th}, is obtained by applying various back-gate biases. It is shown that a nominal V_{th} of 500 mV

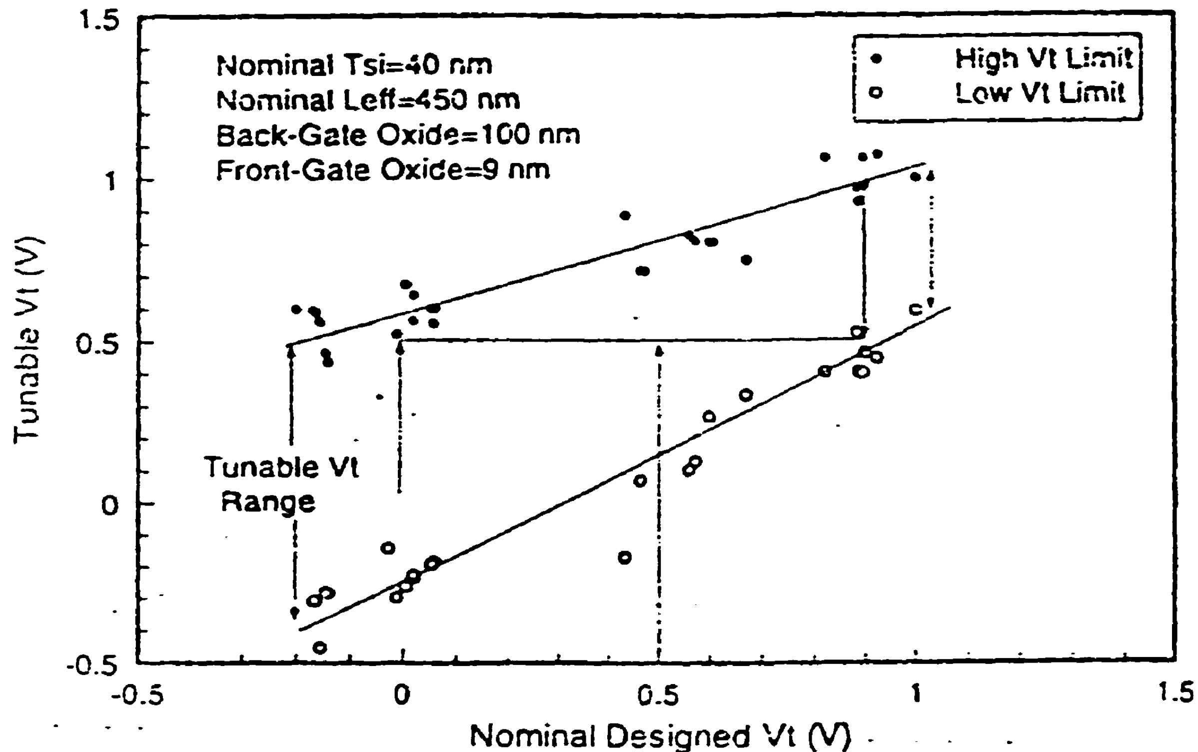


Fig. 2.5 Tunable V_{th} ranges by back-gate biasing [2].

maybe reached from around ± 500 mV deviation by using a ±5-6 V back-gate bias. However, physical mechanisms limiting range of V_{th} control are not explained.

Similar SOI structures with oxide-isolated back-gate electrodes have been describe previously elsewhere [23][28] [29] although in these studies the back-gate electrodes were not used for V_{th} control. However, the structures described in these studies are based on complex wafer bonding and etch-back techniques, and appear extremely difficult to manufacture.

An alternative means of forming fully depleted (FD) dual-gated (DG) thin-film SOI-MOSFETs with an isolated buried back-gate was studied in [4]. Epitaxial lateral overgrowth (ELO) into SOI islands is used as shown in Fig. 2.6. Situated in an SOI island, the fully depleted DG SOI MOSFET allows independent operation of both top-gate and back-gate, which is buried and totally isolated from all other devices [28]. This provides a method to control the threshold voltage of the top MOSFET with a bias on the back-gate ($V_{G,back}$) for fully-depleted (t_{si} < 2000A) devices. According to a similar work [30], the back-gate can switch the top MOSFET to more "on" for larger drive currents and to more "off" for lower subthreshold leakage currents. It is reported that the dynamic control of $V_{th,\,top}$ by the $V_{G,back}$ increases the speed, reduces the device width (W) for a given I_{Dsat}, and is ideal for ultra-low power circuits for $\leq$1.2 V power supplies.

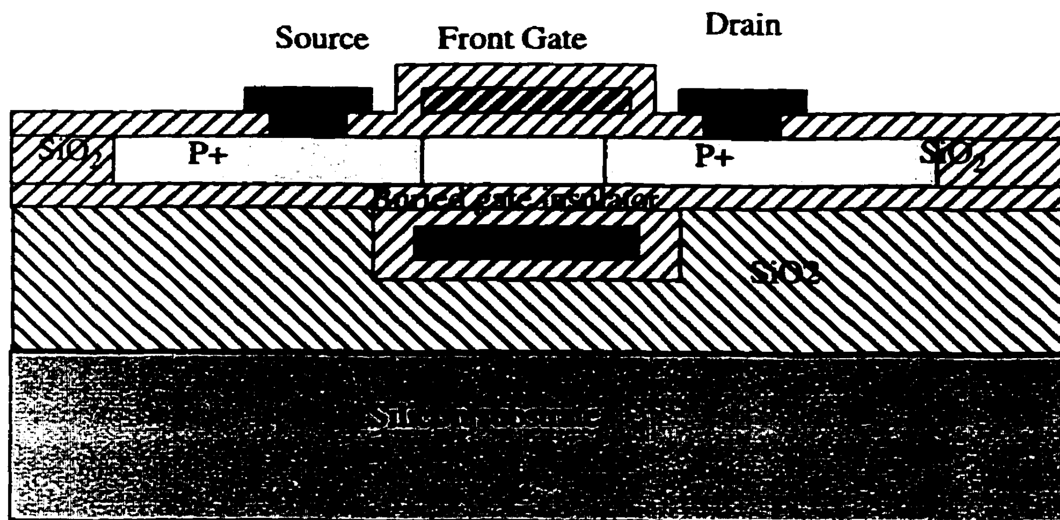


Fig. 2.6 Dual-Gated Thin-Film SOI MOSFET by ELO [4].

The ELO has a thin buried thermal gate oxide using standard Si wafers, hence providing less expensive and simple production. The close symmetry and size between the top-gate and back-gate which generates less overlap capacitance C_{stray} also simplifies device layout and circuit design for this structure. Furthermore, the buried polysilicon gate can also serve as a buried interconnect between devices and circuits, without an area penalty.

Again, according to [30], the buried polysilicon gate and poly-oxide does not significantly affect the quality and electrical performance of the back-gate device. Therefore, in order to simplify the experiments, the structure in Fig. 2.7 was fabricated with either a thermal oxide (OX) or nitrided thermal SiO2 (NOX) as the buried gate insulator. Averaged over 11 devices, the measured shift of $\Delta V_{T,top}/\Delta V_{G,back} = 0.34$ V/V for NOX and 0.33 V/V shift for OX. The data indicates that the nitride buried oxide had little or no effect on the operation of the SOI PMOSFETs as compared to the thermal oxide. It is also observed that thinner buried NOX has increased $\Delta V_{T,top}/\Delta V_{G,back}$ to 0.52 V/V for even better V_{th} control.

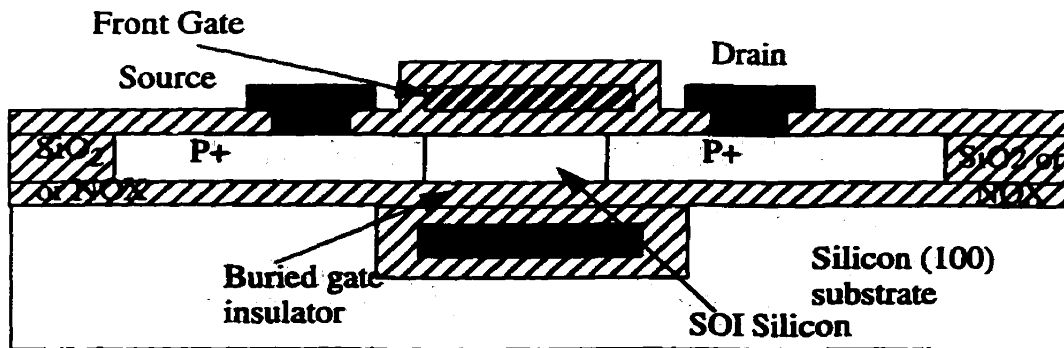


Fig. 2.7 SOI P-MOSFET Device fabricated in [30].

2•5 Implanted Back-gate Electrodes For V_{th} Control In Fully-Depleted SOI CMOS

It has been shown recently that it is possible to dynamically control the threshold voltage V_{th} of MOSFETs in a fully-depleted silicon-on-insulator (FD-SOI) technology by constructing a junction-isolated implanted back-gate electrode under the buried oxide [5][6].

In the work of [6], an SOI CMOSFET with a variable threshold-voltage using simple implanted back-gate electrodes is proposed and fabricated in a 0.5 μm process. The back-gate electrodes are simply formed by P-ion implantation in a p type Si substrate (with a concentration of 3×10^{17} cm^{-3}) through a 60-nm-thick Si layer and a 100-nm-thick buried SiO_2 layer. Independent substrate biases (positive biases for NMOSFETs and negative biases for PMOSFETs) can therefore be applied through the back gate electrodes and the p^+ substrates. A LOCOS process is used to achieve isolation, followed by 12-nm-thick gate SiO2 formation, comparatively deep non-uniform channel implantations [31], and W/Si_2/poly Si dual-gate-electrode formation, *i.e.* n^+ poly silicon for NMOSFETs and p^+ poly silicon for PMOSFETs. W and Al layers are respectively formed for the first and second level wiring. As only adding one mask process and one ion implantation process enables to make the variable V_{th} SOI CMOSFETs, the process is much simpler than work reported in [2].

The simulation results of SOI NMOSFETs with SOI thickness of 20 to 70 nm show that a 2 V V_{bkgt} change results in a approximately 0.35 V V_{th} change for devices with an identical channel implan-

tation BF_2 dose of 3×10^{12} cm^{-2}. The experimental thresholds shift about $\pm$ 0.5V for a V_{bkgt} of 2V for long-channel NMOSFETs and PMOSFETs. The drain current in the V_{bkgt} biased SOI MOSFETs showed 30% more current for n-channel and 24% more for p-channel than those in unbiased (0V for NMOSFET and -2V for PMOSFET) SOI devices. These lead to a 46% smaller propagation delay of a power-managed SOI CMOS ring oscillator with 0.7-µm-long gates operating at 1V than that of a bulk ring oscillator under almost the same power consumption.

However, the approach to back-gate electrode formation presented in [6] is somewhat restrictive, in that a p^+ substrate is used, and back-gate electrodes are formed only beneath the n-channel transistors through high-energy phosphorous ion implantation. In this approach only blanket V_{th} adjustment is possible for pMOSFETs.

In a recent study of the simple buried back-gate electrode method of V_{th} dynamic controlling by Tarr *et al.* [5], a similar back-gate structure is used. Its cross-section is shown in Fig. 2.8. The p-type back-gate electrode is formed by high energy boron implantation through the silicon film and buried oxide into a lightly doped n-type substrate. For the 1 µm gate length technology generation, the buried oxide thickness is typically 300 nm, and the silicon film thickness 80 nm. SUPREM3 simulation in [5] showed that an $^{11}B^{++}$ implant of $2\times10^{13}cm^{-2}$ at 150 keV can create a moderately doped p-type layer beneath the buried oxide while adding less than $10^{16}cm^{-3}$ to the boron concentration in the silicon thin film. A brief anneal was applied to raise the boron concentration at the interface between the back gate electrode and the buried oxide to more than $10^{17}cm^{-3}$, allowing effective back-gating. Back-gate electrodes could be placed beneath either n- or p-channel transistors, and could be shared by groups of transistors when desired. In the circuit application the n-type

substrate was connected to the most positive potential produced, so that the back-gate electrodes are always reverse biased relative to the substrate, and are always junction isolated. Although Fig. 2.8 shows an extension of the back-gate electrode underneath the MOSFET source to illustrate that contact to this electrode is made through a window in the field oxide, in a practical transistor overlap between the back-gate electrode and the source and drain regions would be minimized to avoid adding parasitic capacitance.

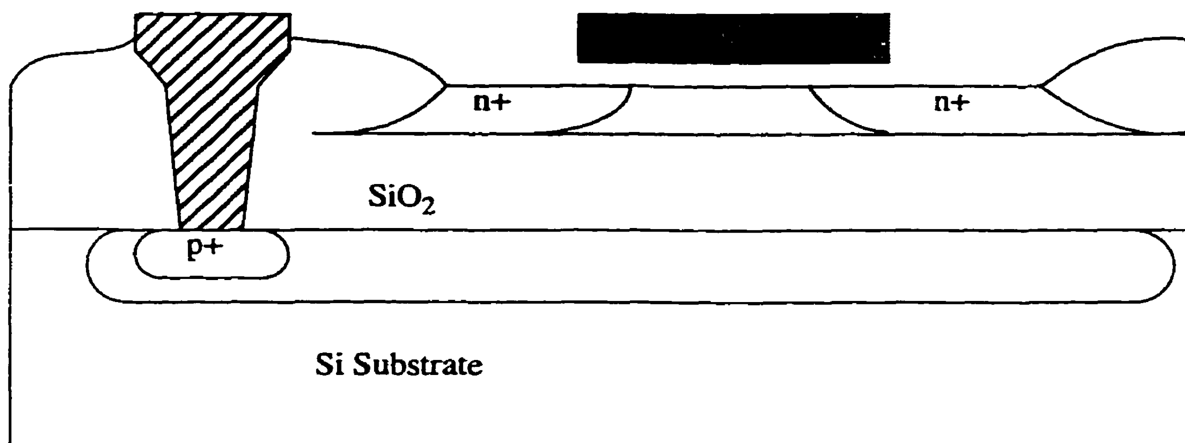


Fig. 2.8 Cross-section of SOI MOSFET with implanted back-gate electrode [5].

The electron and hole sheet density in the channel as function of the front gate bias V_G and back-gate V_B was studied, also using SUPREM3. It shows that S is increased slightly by the addition of the back-gate electrode, from 60 to 63 mV/decade, but is still far lower than in a typical bulk CMOS technology. The shift in V_{th} for different V_B was found by means of SUPREM3 simulations. For V_B changing from -2 V to 2 V, V_{th} of NMOS changes from 325 mV to 10 mV while PMOS changes from -45 mV to -360 mV. The shift is relatively small, but the effect on off-state channel leakage

is large due to the low subthreshold swing. It is concluded that back-gate control of V_{th} could be improved through the use of a thinner buried oxide, but only at the expense of increased parasitic capacitance between source/drain junctions and the substrate, and a slight increase in S.

Experimentally, there were two concerns in developing the back-gate SOI process flow which could not be answered through simulation. The first was that the back-scattered "tail" of Boron atoms produced during the back-gate electrode implant would not be accurately modelled by SUPREM3, giving an undesirably high concentration of Boron in the device wells which would have to be compensated by subsequent implants. The second concern was that the PN junctions formed between the back-gate electrodes and the substrate might be extremely leaky as a result of residual damage left by the high- dose oxygen implant used to produce SOI material in the SIMOX technique [13].

Experimental devices were fabricated using SIMOX substrate phosphorous doped to 10^{15} cm^{-3} with nominal buried oxide, silicon film and gate oxide thickness identical to those used in the simulations. The boron doping profile prediction by SUPREM3 is shown in Fig. 3.3 with the comparison with experimental data obtained from spread resistance profiling. It was found that the back-scattered boron "tail" is visible in the surface region, but for depths less than 0.1μm the back-scattered dopant concentration is far below the final target well doping of 4-5$\times 10^{16}$ cm^{-3}, and so should not interfere with well formation. The current voltage characteristics of a large-area back-gate-electrode-to-substrate diode shows that reverse leakage is less than 30 $nAcm^{-2}$ for reverse biases less than 5 V. This indicates that it should be relatively easy for a charge-pump circuit to supply bias to the back-gate electrode.

The experimental subthreshold characteristics shows that it is necessary to apply a relatively large negative back-gate bias (~10 V) to bring V_{th} to the 200 mV target due to the light well doping. A 1V change in V_B from this starting point shifts V_{th} by 70 mV, which agreed with SUPREM simulation.

In the same paper, the SOISPICE circuit simulator [32] was used to simulate a simple circuit capable of adjusting the back-gate electrode bias to provide dynamic control of V_{th} for an n-channel transistor. Fig. 2.9 shows the schematic. A reference voltage V_{ref} was applied to the gate of test transistor N1. If V_{th} for N1 is low, current is drawn through resistor R, pulling the input of inverter INV1 low and turning on the ring oscillator. The output of each oscillator stage is connected to the cascade charge pump circuit shown in Fig. 2.9. A cascade design was used to maximize the output voltage magnitude provided by the pump for small input voltage. The charge pump outputs are in turn connected to a back-gate electrode shared by all n-channel transistors in the circuit, applying a negative bias to this electrode to raise V_{th}. A distributed charge pump is used to minimize ripple on the back-gate electrode. Simulation shows the charge pump circuit is capable of providing an output voltage magnitude of up to 2 V for 1V supply operation.

2•6 Relation of This Thesis to Previous Work

This thesis extends the study of the implanted back-gate FD-SOI MOSFET structure introduced in [5]. In particular, the dependence of back-gate threshold control sensitivity $\Delta V_{th}/\Delta V_B$ on back gate doping concentration, buried oxide and silicon film thickness is studied through SUPREM3 simulations. SUPREM3 and MEDICI simulations are used to investigate the limitations in the range of threshold voltage control that can be achieved through back-gating. The simulation results are con-

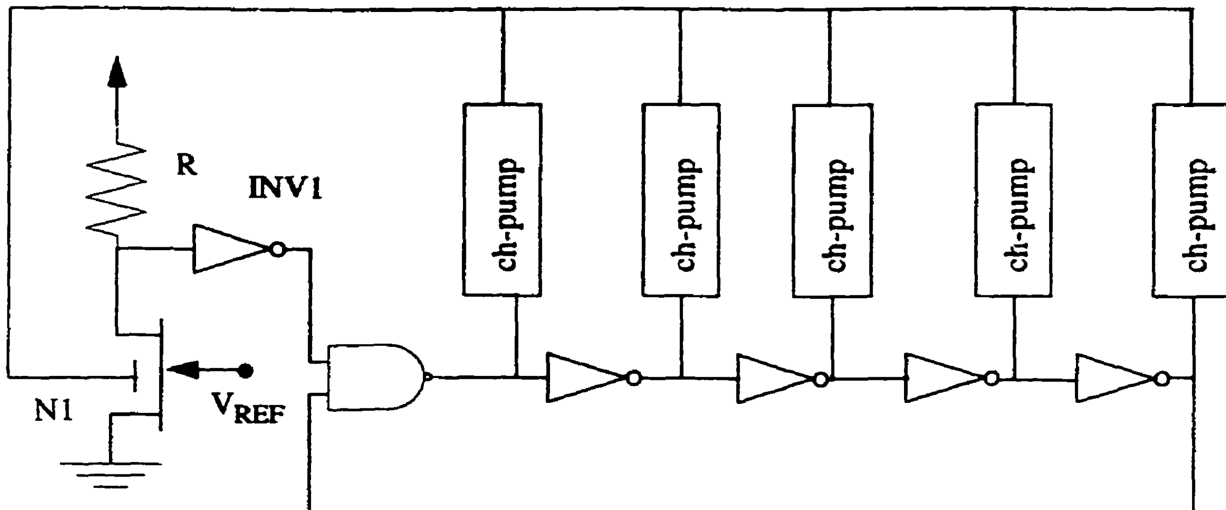


Fig. 2.9 Schematic of circuit providing dynamic control of V_{th}.

firmed by comparison with the characteristics of experimental device. The thesis goes on to consider the design of a complete threshold voltage control system using charge pumps to provide bias to the back-gate electrodes. The system presented is superior to that described in [5] in that back-gate biases much larger in magnitude than the power supply voltage can be generated. Improvement have also been made in the circuitry used to sense whether V_{th} lies within the desired range.

CHAPTER 3

Device Simulation Results

The cross-section through an n-channel SOI MOSFET with an implanted back-gate is shown in Fig. 3.1 while a plan view of the device is shown in Fig. 3.2. It is this structure that is being studied both in simulation and experiment.

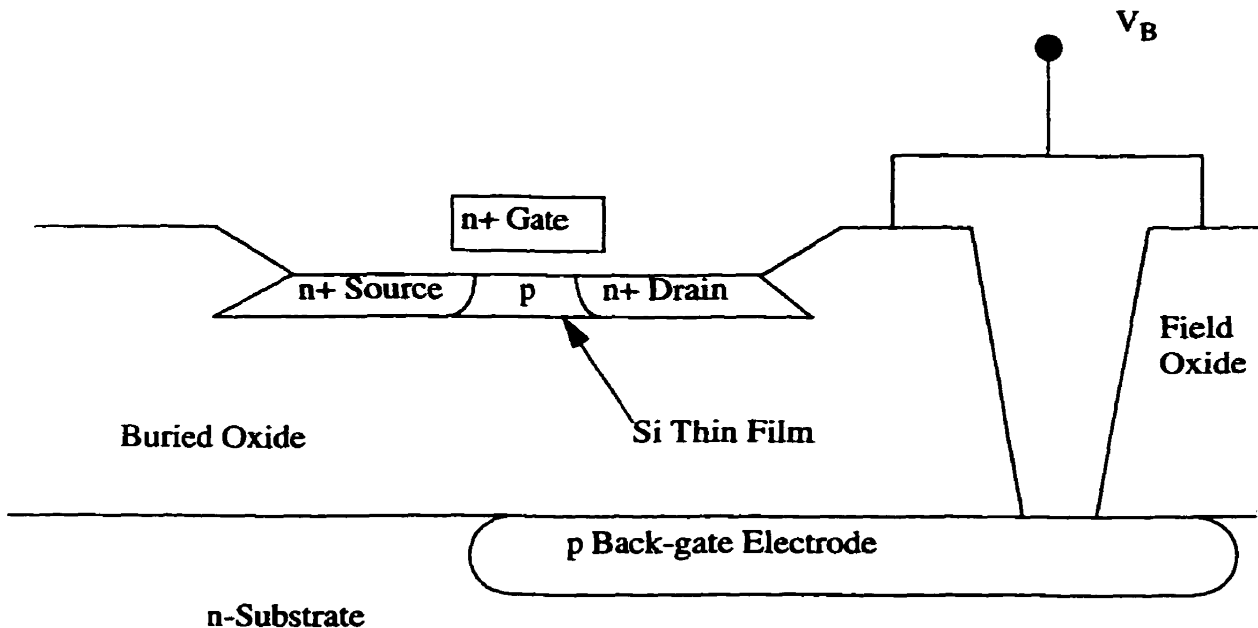


Fig. 3.1 Cross-section of SOI MOSFET with implanted back-gate electrode.

It is illustrated in the plan view that the overlap between the source and drain regions and the buried back gate electrode is minimized in order to reduce parasitic capacitance. For an n-type substrate, a p-type back gate electrode is formed by high energy boron implantation through the silicon thin film and buried oxide. By connecting the n-type substrate to the most positive potential generated in a circuit, the back gate electrodes can be junction isolated. This technique permits different back gate biases to be applied to n- and p-channel transistors in a CMOS circuit, which is required in

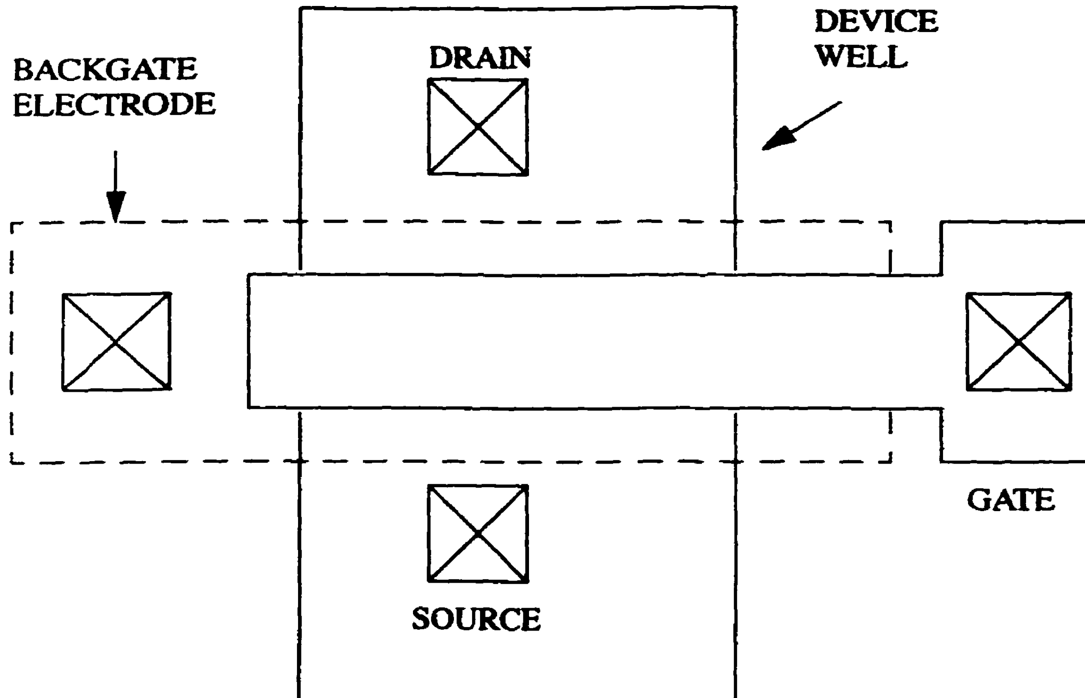


Fig. 3.2 Plan view of SOI MOSFET with implanted back-gate electrode.

practice. It is also possible to apply different back gate biases to different groups of transistors in a large circuit, allowing power consumption to be reduced at the expense of decreased current sourcing capability and speed.

The structure shown in Fig. 3.1 and Fig. 3.2 is simulated using the one-dimensional Poisson equation solver in SUPREM3. This chapter provides more detail on the device structure. Numerical device simulation is then used to examine the limitations on V_{th} adjustment by back-gating in FD-SOI, including the effect of buried oxide and silicon film thickness on V_{th} controllability. The range of back gate bias over which useful V_{th} control can be obtained is also investigated. The results are presented for the 1 and 0.25 µm channel length technology generations. Most of the simulation results are obtained using the one-dimensional Poisson equation solver in SUPREM3. The two-dimensional device simulator MEDICI is used to examine short channel behaviour.

3•1 Device Structure

For the purpose of the simulations, representative silicon film (t_{Si}), gate oxide (t_{gox}), and buried oxide (t_{box}) parameters were selected for the 1 μm and 0.25 μm technology generations based on values presented in[13] [33] [34]. The parameters are listed in Table 3.1. Using SUPREM3 process simulator, the p-well (N_A) and n-well (N_D) doping levels required to give long channel front gate threshold voltages V_{Tn} = 200 mV and V_{Tp} = -200 mV (appropriate for 1V supply operation) for V_B = 0 here determined to be 5×10^{16} and 3×10^{17} cm^{-3} for the 1 and 0.25 μm generations, respectively. The gate was assumed to be doping by the source/drain implant was assumed, giving n^+ gates for n-channel devices, and p^+ gates for p-channels.

Table 3.1 Structural parameters assumed in simulation for various SOI technology generations

L_{eff} (μm)	t_{gox} (μm)	t_{Si}(nm)	t_{box}(nm)	N_A(cm^{-3})	N_D(cm^{-3})
1	25	80	350	4.4×10^{16}	5.0×10^{16}
0.25	7	40	100	3.1×10^{17}	3.4×10^{17}

The p-type back gate electrodes can be formed with relative ease by implanting doubly ionized boron using a conventional implanter. This applies even for the thickest buried oxides normally produced by the Separation by IMplantation of OXygen (SIMOX) technique [13] which is now in widespread use for forming SOI substrates. Fig. 3.3 shows the boron profile predicted by SUPREM3 for implantation of $^{11}B^{++}$ at an energy of 300 keV and dose of 2×10^{13} cm^{-2}. We assumed an 80 nm thick Si film overlying a 350 nm buried oxide, these are values appropriate for the 1μm generation. For comparison we include data obtained from spreading resistance profiling of a lightly-doped bulk n-type test wafer which had received this implant and a 1050°C 20 seconds rapid thermal anneal. It is shown that the high-energy boron implant can form a moderately-doped buried

electrode without leaving a back-scattered "tail" in the silicon for concentration high enough to interfere with well doping. Fig. 3.3 also shows that a brief anneal at 1100°C will raise the boron concentration at the buried oxide/substrate interface to over 10^{17} cm^{-3}, which is sufficient to provide effective back-gating. The sheet resistance of the buried layer is 1.2 kΩ/□ which, in series with the junction capacitance to the lightly doped substrate, gives an RC time constant much less than 1 ns for a 10 μm long, 2 μm wide electrode. This allows sufficiently rapid switching of back gate potential for any practical application. Similar results can be obtained for the 0.25 μm generation using slightly lower implant energies to compensate for the thinner buried oxide. On the other hand, an n-type back-gate electrode can be formed in a p-type substrate, but would require the implantation of triply-ionized phosphorus if accelerating voltages are limited to the normal maximum of 200 keV and t_{box} is greater than approximately 100 nm.

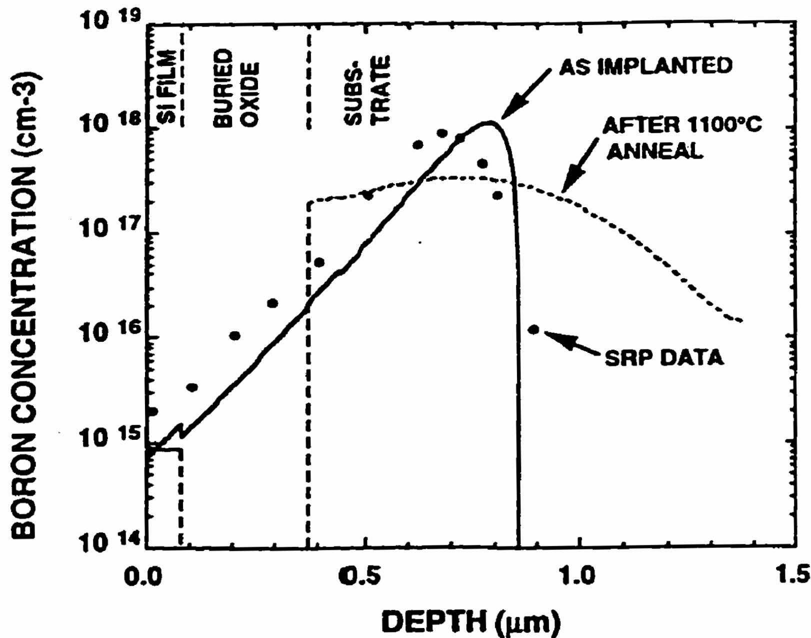


Fig. 3.3 Doping profile predicted by SUPREM3 for 300 KeV, 2×10^{13} cm^{-2} $^{11}B^{++}$ implant into SOI structure, both as-implanted and after 1100°C drive in. Dots show experimental data obtained by spreading resistance profiling of bulk n-type test wafer after rapid thermal annealing (RTA) implant activation.

3•2 Simulated Electrical Characteristics

Results presented in this section are for n-channel transistors. Results for p-channel devices are similar. The only minor difference between n- and p-channel devices results from the work function difference between a p-type back-gate electrode and an n-well, which tends to invert the n-well, lowering $|V_{Tp}|$ slightly.

3•2•1 Subthreshold Characteristics

The one-dimensional Poisson equation solver in SUPREM3 was used to determine the electron sheet density Q_n in the silicon film as a function of front and back-gate bias. V_{Tn} was determined by extrapolating the linear region of the Q_n - V_G characteristic to locate its intercept with the Q_n = 0 axis. By plotting Q_n versus V_G, the subthreshold characteristics of a long-channel device can be constructed. These characteristics are shown in Fig. 3.4 for an n-channel device from the 1 µm generation. Fig. 3.5 shows V_{th} and the subthreshold swing S as a function of V_B for the same device.

For $-3\ V < V_B < 3\ V$, application of back-gate bias leads to a simple displacement of the subthreshold characteristic along the V_G axis. For V_B in this range, S is approximately 63 mV/decade, close to the minimum theoretical value at 300 K, while $\Delta V_{th}/\Delta V_B = 70$ mV/V.

For $|V_B| > 5$ V, more complex behaviour is found, with significant changes in the shape of the subthreshold characteristic apparent depending upon whether the hole population in the silicon film is or is not allowed to reach a thermal equilibrium condition. For $V_B < -5$ V, if holes are available in sufficient supply, an accumulation layer forms at the back interface of the silicon film. Once the accumulation layer has formed, the MOSFET characteristics become similar to those of a partially-

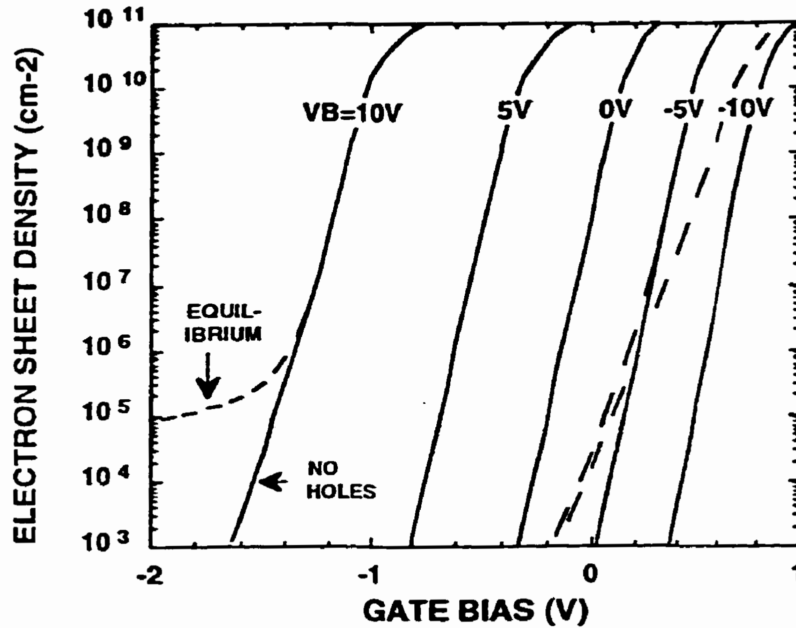


Fig. 3.4 Subthreshold characteristics predicted by SUPREM3 for device from 1μm generation. Dashed lines are based on equilibrium hole concentration in Si film, solid line on complete hole depletion.

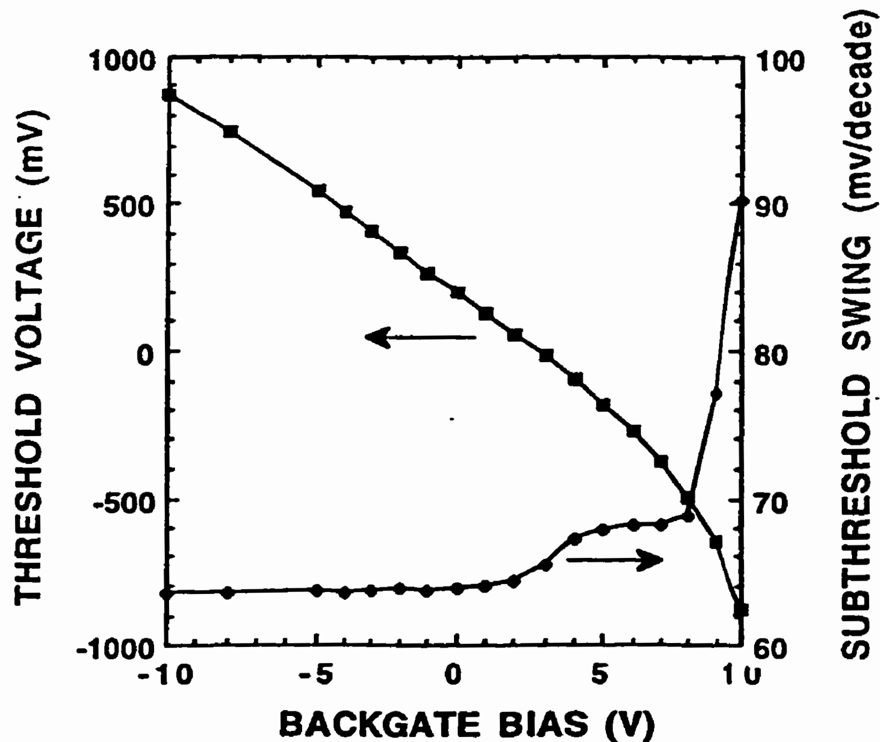


Fig. 3.5 Dependence of S and V_{th} on V_B for devices of Fig. 3.4. Complete hole depletion assumed.

depleted device in a heavily doped silicon film. At $V_B = -5$ V, S has degraded to 120 mV/decade. The accumulation layer also serves as an electrostatic screen, preventing further increases in $|V_B|$ from modulating V_{th}.

For $V_B > 3$ V SUPREM3 shows that an electron inversion layer or back channel can form along the interface of the silicon film with the buried oxide for low values of V_G. As V_G is increased a front channel forms and begins to dominate conduction, but Fig. 3.5 shows that there is an overall slight increase in S since gate control over electrons in the back channel is weaker than for those in the front channel. For $V_B > 8$ V the back channel dominates conduction throughout the subthreshold regime. If film remains depleted of holes, the front gate can still exert some control over this back-channel inversion layer, but S is badly degraded, increasing to 90 mV/decade at $V_B = 10$ V. If sufficient time is allowed for the hole population to reach its equilibrium value, for $V_B > 7$ V a hole accumulation layer forms at the front surface of the silicon film for low V_G. This accumulation layer effectively screens the back channel from changes in V_G, so the front gate loses all control of the drain current. This effect can be seen in Fig. 3.4 for $V_B = 10$ V. The influence of silicon film back interface accumulation and inversion on subthreshold characteristics in FD-SOI devices has been considered previously [35], but the effect of non-equilibrium hole concentrations was not discussed.

If the back-gate bias changes slowly enough for the majority carrier population in the silicon film to reach thermal equilibrium, then the useful range of V_{th} adjustment is limited to approximately 1300 mV for all the structures listed in Table 3.1. Attempting to increase V_{th} by more than 300 mV will lead to accumulation of the back surface of the silicon film, with associated degradation of sub-

threshold swing, while attempting to decrease V_{th} by more than 300 mV risks formation of a back channel. If buried oxides thinner than specified in Table 3.1 are used, the range of useful V_B values is reduced, but the V_{th} adjustment range remains unchanged to a first approximation.

Since intervals of many seconds are required to form an accumulation layer in an initially fully-depleted film in good-quality SOI material, it might be expected that the above restrictions could be ignored for rapid excursions in V_B. However, it is shown in Chapter 5 that equilibrium majority carrier population may be established very quickly if even a weak avalanche forms at the drain end of the MOSFET channel. This may be a significant factor if the drain voltage exceeds 1.5 V.

3•2•2 Dependence of $\Delta V_{th}/\Delta V_B$ on Back-gate Doping Concentration

Formation of the back-gate electrode by implantation allows for a very simple fabrication process, but restricts the dopant concentration in the electrode to the range 10^{17} - 10^{18} cm^{-3}. Fig. 3.6 shows the dependence of $\Delta V_{th}/\Delta V_B$ on back-gate doping concentration as V_B is lowered from 0 to -1 V for a 1 µm generation device with buried oxide thickness reduced to 200 nm. Even for this relatively thin oxide, it is seen to be saturated for back-gate doping above approximately 10^{17} cm^{-3}, verifying that a moderately-doped implanted back-gate electrode can provide effective control of V_{th}.

3•2•3 Dependence of S and $\Delta V_{th}/\Delta V_B$ on Buried Oxide Thickness

Fig. 3.7 shows the dependence of S and $\frac{\Delta V_T}{\Delta V_B}$ on t_{box}. As expected, reducing t_{box} increases the ability of back gate biasing to control V_{th}, but at the expense of a slightly increased subthreshold swing. Even for relatively thin buried oxides, S is still markedly lower than would be expected for a con-

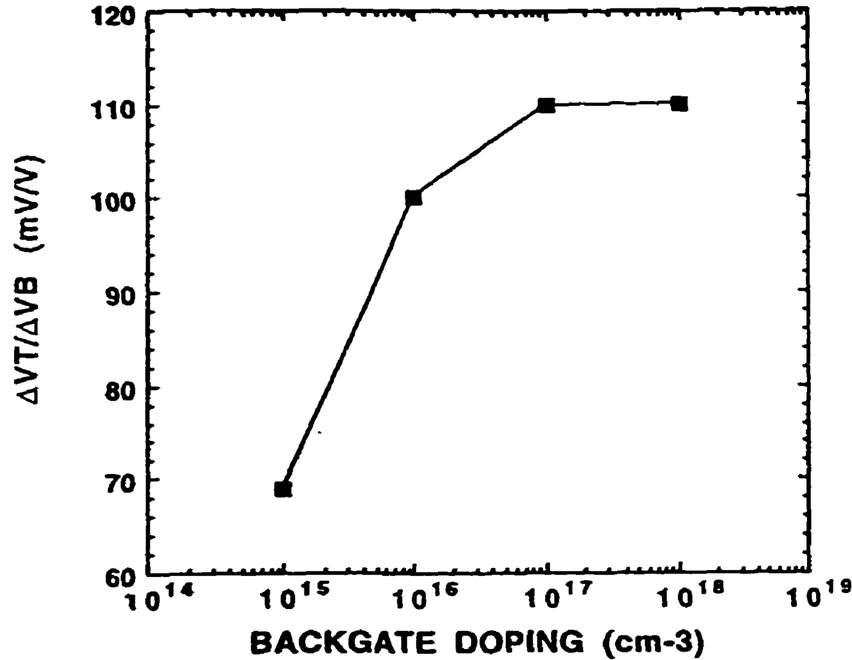


Fig. 3.6 Dependence of $\Delta V_{th}/\Delta V_B$ (for V_B from 0 to -1 V) on back gate electrode doping for device from 1 μm generation.

ventional bulk CMOS technology supporting the same minimum channel length.

It should be noted that modelling the back gate electrode as a perfect conductor gives [36]

$$\Delta V_T = -\frac{t_{gox}}{t_{box}} \frac{1}{\left(1 + \frac{t_{Si}}{t_{box}} \cdot \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\right)} \Delta V_B \tag{3.1}$$

which is in agreement with the numerical results of Fig. 3.7.

3•2•4 Dependence of S and $\Delta V_{th}/\Delta V_B$ on Silicon Film Thickness

The dependence of $\Delta V_{th}/\Delta V_B$ on t_{Si} for fixed t_{box} was also studied. $\Delta V_{th}/\Delta V_B$ changed by less than 5% as t_{Si} increased from 40 to 120 nm. This lack of sensitivity of $\Delta V_{th}/\Delta V_B$ to t_{Si} results from the silicon film typically being considerably thinner than the buried oxide, and having roughly three

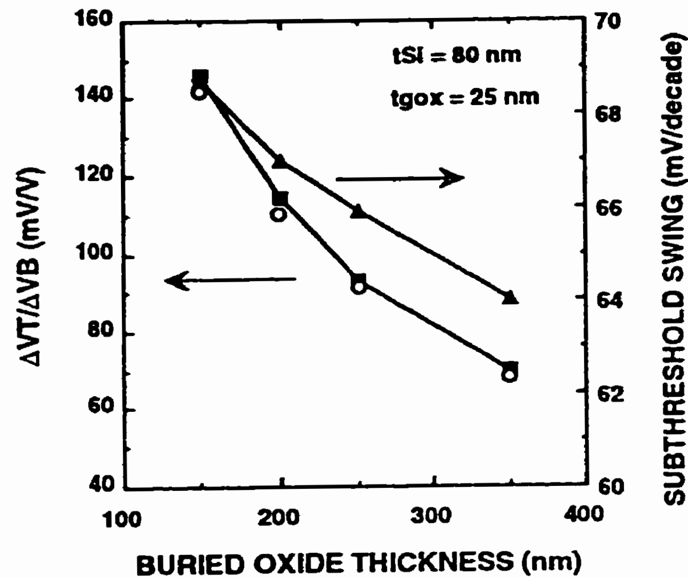


Fig. 3.7 Dependence of S and $\Delta V_{th}/\Delta V_B$(for V_B lowered from 0 to -1V) on buried oxide thickness for 1 μm generation.

times greater permittivity. For given t_{box} and t_{gox}, a similar $\Delta V_{th}/\Delta V_B$ value can be expected for any reasonable value of t_{Si} appropriate for a fully depleted device.

3•2•5 Back-gate Influence on Short Channel Effects

Application of a small positive back-gate bias insufficient to cause strong inversion of the back surface of the silicon film still tends to increase susceptibility to short-channel effects including short-channel reduction in V_{th}, drain-induced barrier lowering, and punch-through. This arises because positive V_B lowers the energy barrier holding electrons in the source near the back side of the silicon thin film. Barrier lowering near the bottom edge of the film is particularly undesirable, since this region is poorly controlled by the front gate. Additional lowering of the barrier by electric field

lines encroaching from the drain allows electrons to escape from the source. Fig. 3.8 illustrates the effect of positive V_B in enhancing drain induced barrier lowering, plotting the difference $V_{G,DIBL}$ between the gate bias required to obtain I = 10 nA for V_D = 0.1 V and for V_D = 1.0 V as a function of back-gate bias for a 1 μm wide device with L_G = 0.4 μm, but with other structural parameters appropriate for the 1 μm generation. $V_{G,DIBL}$ is seen to increase with increasing V_B.

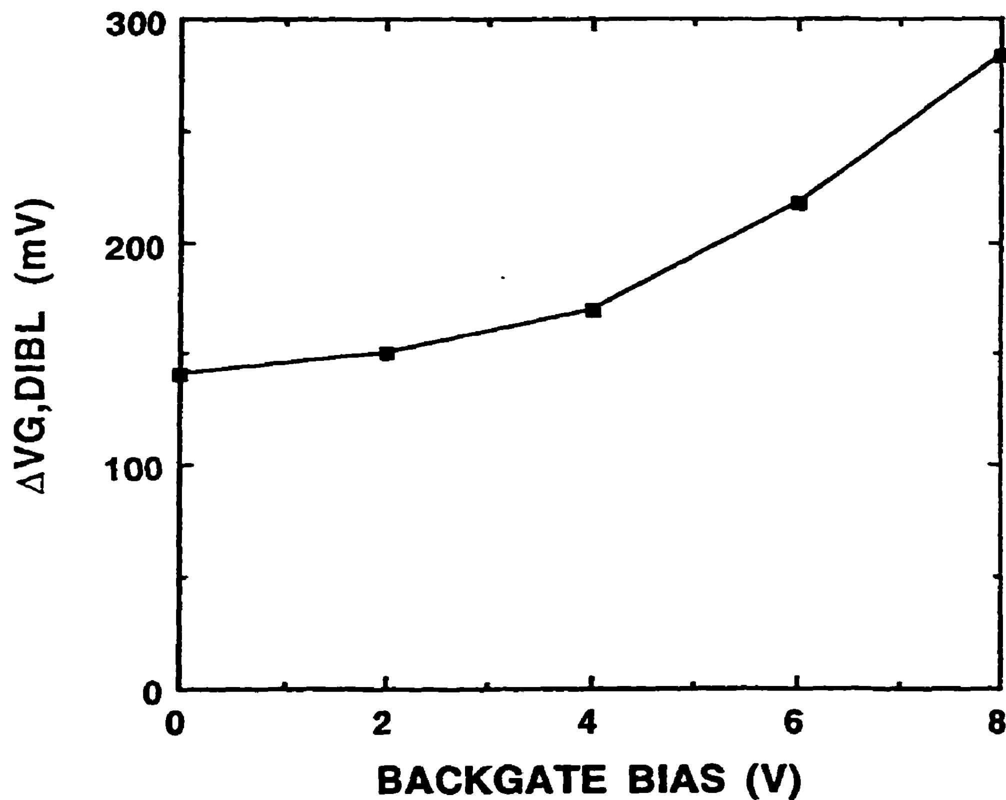


Fig. 3.8 Dependence of difference in gate bias $\Delta V_{G,DIBL}$ required to maintain I_D = 1nA/μm as V_D is increased from 0.1V to 1 V, as a function of V_B. L_G = 0.4 μm, otherwise 1 μm generation structural parameters. L_G was chosen to be 0.4 μm to ensure that short channel effects is apparent. MINIMOS6 simulation.

3•2•6 Effect of Back-gate Electrode on Circuit Speed

SOI technologies typically make use of much lighter substrate doping than bulk technologies. Combined with the presence of the buried oxide layer, they can lead to very low parasitic capacitance between source and drain regions and the substrate in SOI, which translates to an advantage in circuit speed at equal channel dimensions. It might be expected that some of this advantage would be lost through the use of a moderately-doped back-gate electrode, particularly if the buried oxide is thinned to improve $\Delta V_{th}/\Delta V_B$. A rough estimate of the loss in circuit speed resulting from the use of a back-gate electrode was made by computing the parasitic capacitance associated to parameters specified in Table 3.1. A gate length of 1 μm and width of 5 μm and drain area of 12 μmXμm were assumed. For a device with no back-gate electrode and a substrate doping of 10^{15} cm^{-3}, the capacitance between the channel region and the substrate is 0.27 fF, while the capacitance between the drain and the substrate is 0.65 fF, assuming that the substrate is always depleted to the maximum extent possible. For a device with a back-gate electrode overlapping the channel by 1 μm, the capacitance between the channel and substrate is 0.49 fF, and between the drain and substrate 0.90 fF. For both devices the gate-channel capacitance is 6.9 fF. Assuming a circuit configuration in which the drain of each device is loaded with the channel-substrate and drain-substrate capacitance plus the gate-channel capacitance (representing the input of the next stage), use of a back-gate electrode increases the load capacitance by just 6% under worst-case conditions. Adding a back-gate electrode would therefore be expected to add at most 6% to the delay of a simple logic gate, with even smaller increases in delay for gates loaded primarily by interconnect capacitance.

3•3 Scaling Down To 0.25μm Technology

The SUPREM3 simulations of the back-gated SOI MOSFET presented in the above sections are based on a 1 μm technology generation. It is of interest to consider whether threshold voltage control by back-gate biasing is a useful technique as technology scales down to 0.25 μm generation. In comparing Fig. 3.9 below and Fig. 3.7 in Section 3•2•3, one can see that similar values of $\Delta V_{th}/\Delta V_B$ are obtained for the two technology generations listed in Table 3.1. Scaling down t_{box} at roughly the same rate as t_{gox} as the minimum channel length is reduced gives similar $\frac{\Delta V_{th}}{\Delta V_B}$ for both technology generations.

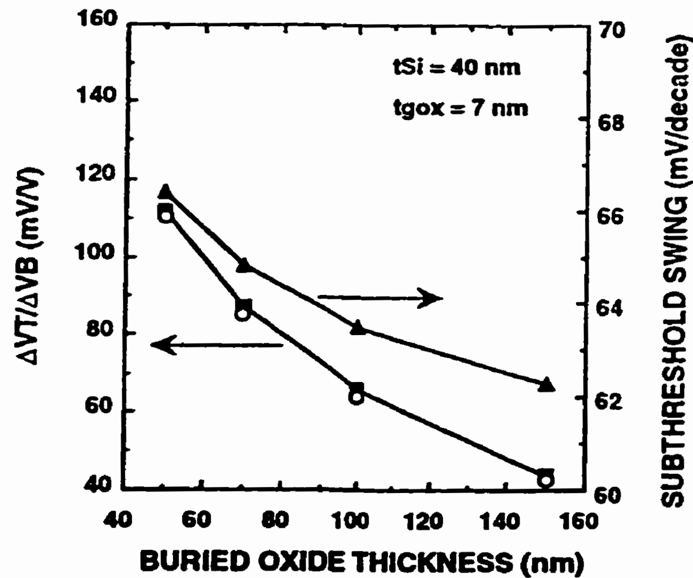


Fig. 3.9 Dependence of S and $\Delta V_{th}/\Delta V_B$(for V_B lowered from 0 to -1V) on buried oxide thickness for 0.25 μm generation.

In Fig. 3.7 which is for 1 μm technology, the threshold voltage control ability which is marked by $\Delta V_{th}/\Delta V_B$ gives 100 mV/V with a front to back gate oxide thickness ratio of 1/10 (25 nm/250 nm). In Fig. 3.9, which is for 0.25 μm technology, the same V_{th} control ability is obtained at a similar

ratio of front to back gate oxide thickness (1/10 or 7 nm/ 70nm). This tells us that the ability of threshold voltage control by back-gate biasing on the transistors is not compromised by technology scaling down as long as the back-gate oxide thickness is scaled down proportionally with the front gate oxide thickness as the minimum channel length is reduced. We can therefore conclude that provided the front gate and back-gate oxide thicknesses are in the same ratio in the 0.25 μm technology as in the 1 μm technology, a back-gate bias threshold voltage control sensitivity of approximately 100 mV/V could be achieved. It is notable that commercial suppliers of SOI wafers are thinning the back-gate oxide thickness in this way already [37].

3•4 Chapter Conclusion

This chapter examines in detail the consequences of using implanted back-gate electrodes for V_{th} adjustment in FD-SOI, including the effect of buried oxide and silicon film thickness on V_{th} controllability, the range of back-gate bias over which useful V_{th} control can be obtained, the influence of back-gating on short-channel effects, and degradation in switching speed resulting from the presence of the back-gate electrode. The investigation is aimed primarily at evaluating the usefulness and limitations of implanted back-gate electrodes for dynamic threshold control for 1 V supply operation. It has been shown through simulation that back-gate electrodes formed by a simple ion implantation technique can provide useful control of threshold voltage in fully-depleted SOI CMOS. This result holds as channel lengths are scaled from 1μm down to 0.25 μm, provided the buried oxide and silicon film thicknesses are scaled at roughly the same rate as the gate oxide thickness. For a long n-channel MOSFET, the maximum useful negative back-gate bias which can be applied is limited by the formation of an accumulation layer at the back surface of the silicon film. Conversely, the maximum useful positive back-gate bias is limited by the enhancement of short-chan-

nel effects and, in more extreme cases, by formation of a backside inversion layer. These constraints restrict the available useful range of threshold adjustment by back-gating to approximately 1300 mV regardless of t_{box} for both the 1 μm and 0.25 μm technology generations. Experimental results are given for device structures appropriate for use in a 1 μm channel length technology generation, and will be described in Chapter 5.

CHAPTER 4

Charge Pump Circuit: Design and Simulation

It was described in Chapter 2 that although the threshold voltage V_{th} has a target value of 200 mV in a low-voltage FD-SOI integrated circuit, it could conceivable deviate by as much as $\pm$300 mV due to variations in temperature or process parameters. (In particular, V_{th} is affected by the variation of temperature ($\pm$ 50°) and silicon film thickness ($\pm$ 50 A). All these variations can contribute up to 300 mV deviation from the nominal V_{th}). Therefore for devices resembling those described in Chapter 3, back-gate biases (V_B) up to approximately $\pm$ 4 V must be applied to the back-gate electrode to compensate for this V_{th} deviation. The choice of an on chip charge pump circuit for 1 V power supply operation to provide the required V_B is based on efficiency and simplicity. In this chapter, a charge pump introduced by Dickson [38] is modified to meet the requirements of back-gate bias generation for low-voltage SOI. The design is guided by SOISPICE simulation. Simulation results show that even if V_{Tn} = -100 mV initially, a pump output of less than -4 V can be supplied to the back-gate electrode to restore a V_{Tn} of 200 mV. In the case of V_{Tn}= 500 mV initially, the pump output can be greater than +4 V to restore V_{Tn} to the 200 mV target. The circuit design and simulation results are followed by a discussion of charge pump layout.

4•1 History of Charge Pump Circuit

Methods of generating a voltage greater than the supply voltage originated with the Cockcroft-Walton multiplier shown in Fig. 4.1. Its design uses a basic property of the capacitor. If we have a ca-

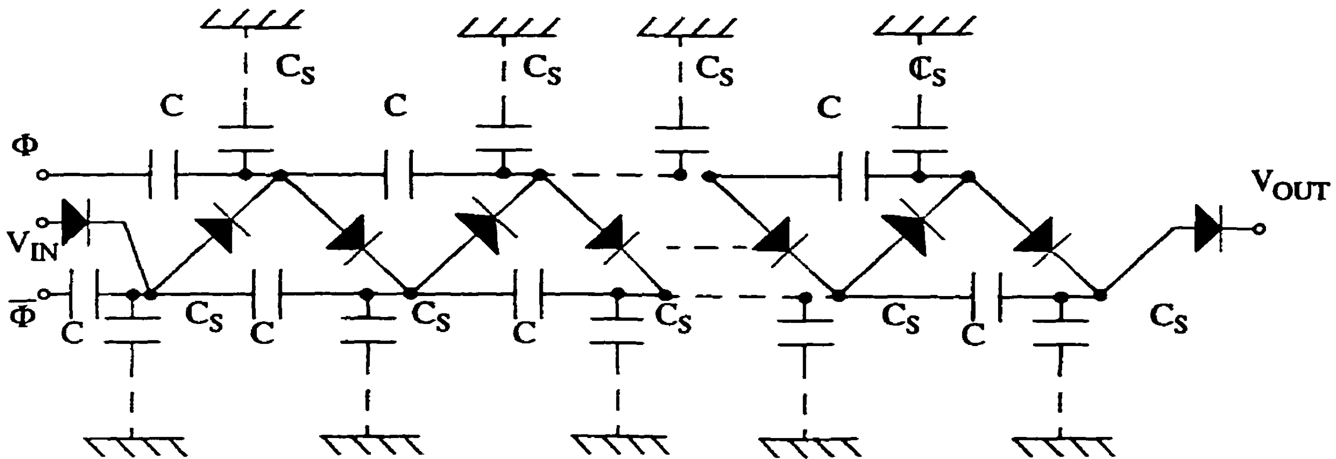


Fig. 4.1 Basic Cockcroft-Walton voltage multiplier. Usually implemented with discrete components such that $C \gg C_S$.

pacitor that is initially charged to a voltage V_{cc} and then we apply to the lower voltage terminal a constant voltage generator of V_{cc}, we obtain a voltage of value $2*V_{cc}$ in the other terminal. (Fig. 4.2(a)). The capacitor in an open loop (*i.e.* with an infinite impedance load) is equivalent to a dc voltage source (in our example of value V_{cc}), or put more simply, it performs a voltage level shift. However, this does not hold if we have a finite load. More specifically, assuming a capacitive load C_L with a stored charge according to the sign in Fig. 4.2(b), the final output voltage of the circuit after the switches have been closed is fixed by the voltage generator plus a voltage due to the final charge in the capacitor C (Fig. 4.2(c)). This charge is less than the initial one because the capacitor C loses part of its initial charge on the capacitor C_L. The charge redistribution allows a growth in the C_L voltage drop to be equal to the C voltage drop plus V_{cc}.

It is simple to understand that the final voltage of the circuit in Fig. 4.2(c) is dependent upon the charge previously stored in C_L (*i.e.* the initial voltage of C_L). Consequently, if we open the switches, recharge the capacitor C to hold a voltage V_{cc}, and then close the switches, we obtain a final

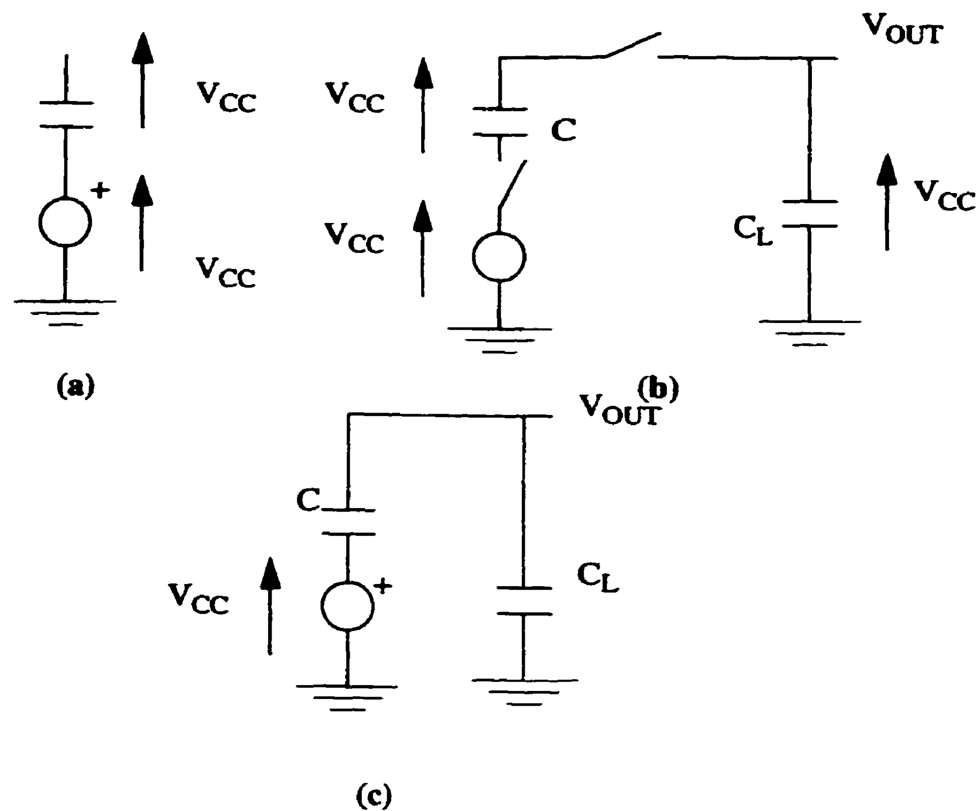


Fig. 4.2 Principal scheme of voltage elevator.

output voltage value greater than the previous one. By repeating these operations many times the output voltage grows asymptotically to the voltage $2V_{cc}$.

Historically, the Cockcroft-Walton multiplier has been used to generate voltages greater than those which could be easily handled by electromagnetic transformers. This is possible since the maximum voltage across any of the coupling capacitors is only equal to the input drive voltage, regardless of the number of multiplying stages. In this type of application, however, the circuit is implemented with discrete components so that the coupling capacitors can be made sufficiently large for efficient multiplication and adequate drive capability. This type of multiplier is not usable in monolithic form since on-chip capacitors are limited to a few picofarads with relatively high values of stray capacitance to substrate. In practice, it is difficult to generate voltages significantly

greater than twice the supply voltage, irrespective of the number of multiplying stages. In fact, if the number of stages is increased beyond a critical number (typically 3 or 4), determined by the ratio of C and C_S, the output voltage actually decreases due to voltage drops in the diode chain.

4•2 Dickson's charge pump circuit

A new multiplier circuit shown in Fig. 4.3 was devised by Dickson [38] to overcome these limitations. It operates a similar manner to the classical Cockcroft-Walton multiplier and can be shown to be an equivalent circuit. However, the nodes of the diode chain are coupled to the inputs via capacitors in parallel instead of in series, so that the capacitors have to withstand the full voltages developed along the chain. The advantages of this configuration include efficient multiplication with relatively high values of stray capacitance, and a current drive capability which is independent of the number of multiplier stages.

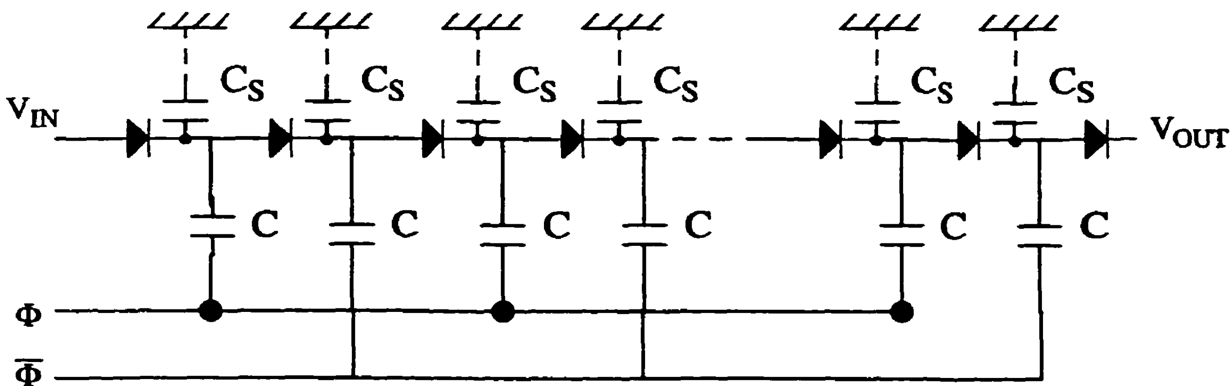


Fig. 4.3 Dickson's voltage multiplier configuration [38].

Fig. 4.4 illustrates the operation of the circuit, showing the typical voltage waveforms in an N-stage multiplier. As can be seen, the two clocks ϕ and $\bar{\phi}$ are in antiphase with amplitude V_f, and are ca-

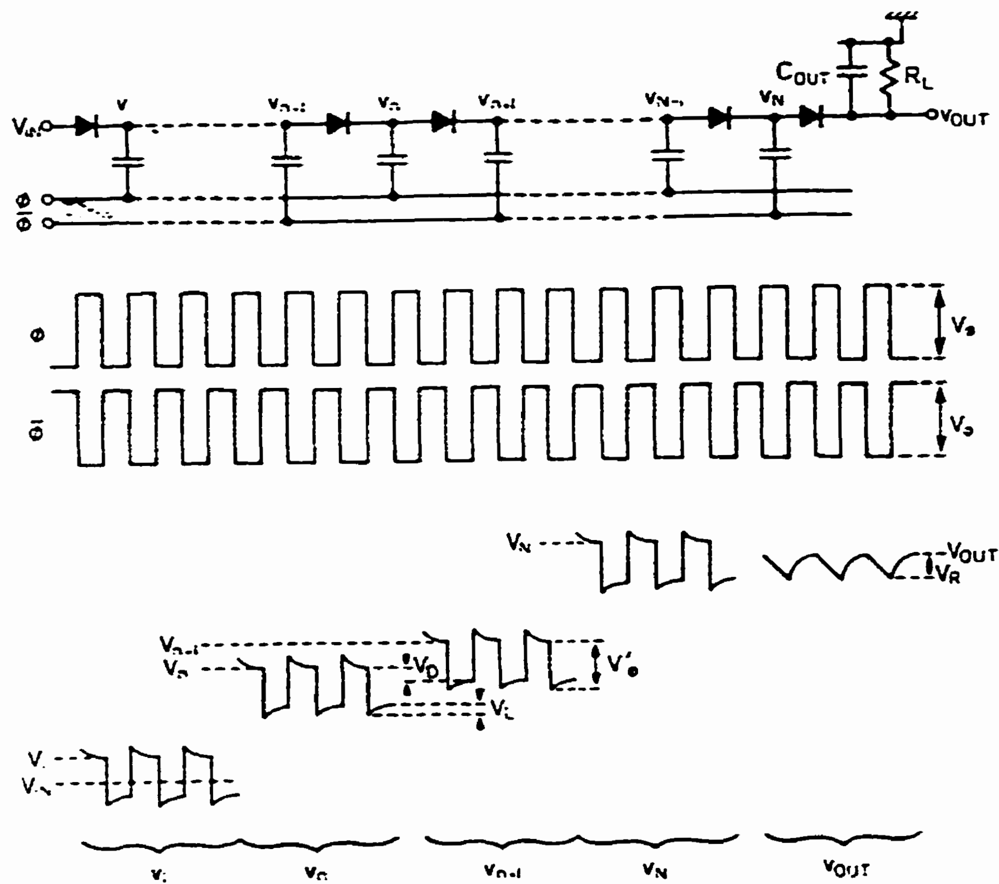


Fig. 4.4 Operation illustration of Dickson's charge pump[38].

pacitively coupled to alternate nodes along the diode chain. The charge pump operates in a manner similar to a bucket-brigade delay line, by pumping packets of charge along the diode chain as the coupling capacitors are successively charged and discharged during half of the clock cycle. Unlike the bucket-brigade delay line, the voltages in the diode chain are not reset after each pumping cycle so that the average node potential increases progressively from the input to the output of the diode chain. This operation is also similar in principle to the "bootstrap" technique often used in MOS integrated circuits in which a bootstrap circuit incorporates a voltage doubler. However here, the coupling capacitor is connected to the input clock, unlike in bootstrap circuits where it is connected to the output.

The difference between the voltages of the nth and (n+1)th nodes at the end of each pumping cycle is:

$$V_{n+1} - V_n = V_\phi' - V_D - V_L \tag{4.1}$$

where the voltage swing at each node due to capacitive coupling from the clock is V_Φ and the forward bias diode voltage is V_D. V_L is the voltage by which the capacitors are charged and discharged when the multiplier is supplying an output current, I_{OUT}.

For a clock coupling capacitance C and stray capacitance C_S, at each node, capacitance division gives:

$$V_\phi' = \frac{C}{C + C_S} \cdot V_\phi \tag{4.2}$$

Also considering the charge pumped by each diode in a clock cycle, the voltage V_L can be expressed as a function of output current I_{OUT} as:

$$V_L = \frac{I_{OUT}}{f \cdot (C + C_S)} \tag{4.3}$$

Therefore the output voltage for N stages is:

$$V_N - V_{IN} = N\left[\left(\frac{C}{C + C_S}\right) \cdot V_\phi - V_D - \frac{I_{OUT}}{f \cdot (C + C_S)}\right] - V_D \tag{4.4}$$

where V_{IN} is the input voltage and an additional isolation diode is required at the output to prevent clock breakthrough. Rearranging (4.4), we can write:

$$V_{OUT} = V_O - I_{OUT} R_S \tag{4.5}$$

where

$$V_O = V_{IN} - V_D + N\left[\left(\frac{C}{C + C_S}\right) \cdot V_\phi - V_D\right] \quad (4.6)$$

and

$$R_S = \frac{N}{f \cdot (C + C_S)} \quad (4.7)$$

V_O and R_S are the open-circuit output voltage and output series resistance of the multiplier, respectively. Thus, a simple equivalent circuit of the multiplier output can be constructed as shown in Fig. 4.5.

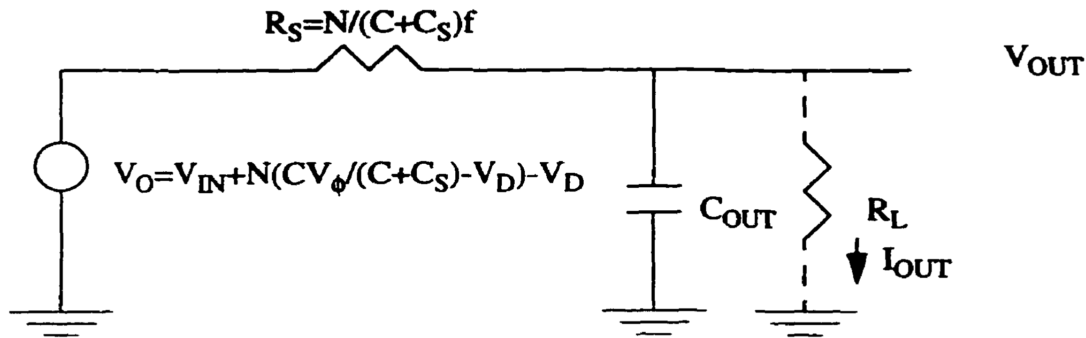


Fig. 4.5 Equivalent circuit of N-stage multiplier.

4•3 Simulation Results

In this work, the Dickson's charge pump was used. A control circuit is also provided which turns on either the positive or the negative pump as required. The complete threshold voltage control system is composed of the decision circuits and the charge pumps. As mentioned for the case of a NMOSFET in Chapter 2, when V_{Tn} is too low (< 200 mV) a negative voltage on the back-gate helps

to restore V_{Tn} back to normal while in the high V_{Tn} case (> 200 mV) a positive back-gate voltage pulls V_{Tn} back to a reasonable value. Therefore a comparator structure was implemented to compare the threshold voltage to a reference voltage which is in the range of the nominal NMOSFET V_{Tn} (around 200 mV). If the NMOSFET V_{Tn} is near 200 mV, the pumps are shut down. When V_{Tn} is lower than 200 mV, both comparators are turned on with the one connected to negative pumps giving positive output to the buffer. This in turn provides clock signals to the pumps while a NMOSFET at the top of the pumps connects V_{SS} as the starting point. The positive pump is turned off by a PMOS device. The detail of the circuit is described in the following sections.

4•3•1 The Decision Logic Circuit

The decision circuit is composed of a comparator structure where a current mirror with a load element is used to maximize the voltage swing at the output node. The current mirrors used for NMOSFET circuits and PMOSFET circuits are complementary between the two devices. In this section, only the NMOS version of the circuit, shown in Fig. 4.7, is described in full. The operation of the PMOS decision circuit shown in Fig. 4.10 is analogous.

In the circuit of Fig. 4.7, transistors M1 and M2 form a voltage divider generating reference bias V_{ref_low} which is applied to the gate of M5. M5 is the test transistor used to determine whether V_{th} lies below the desired range. M5 is loaded with p-channel transistor M4, which is in turn connected in a current mirror configuration with M3. M4 operates in saturation, providing a current source load to M5. The very high differential resistance of the current source ensures that the intermediate output $\overline{V}_{th_low}$ will change rapidly in response to small changes in the threshold of M5. In other words, the circuit block has high gain. $\overline{V}_{th_low}$ is inverted and used to control a logic block which

gates the clocks feeding the negative charge pump.

In this application, the current source is provided off chip. To avoid current noise from the environment, a current magnitude of 1μA is necessary. However, a reference current of 1μA would require a gate voltage of 500 mV to turn on an NMOS transistor with a 200 mV V_{Tn}. A decision voltage V_{nd} is therefore defined denoting the decision voltage applied at the gate of test NMOSFET. Fig. 4.6 shows an I_D-V_{GS} characteristic illustrating the difference between V_{Tn} and V_{nd}.

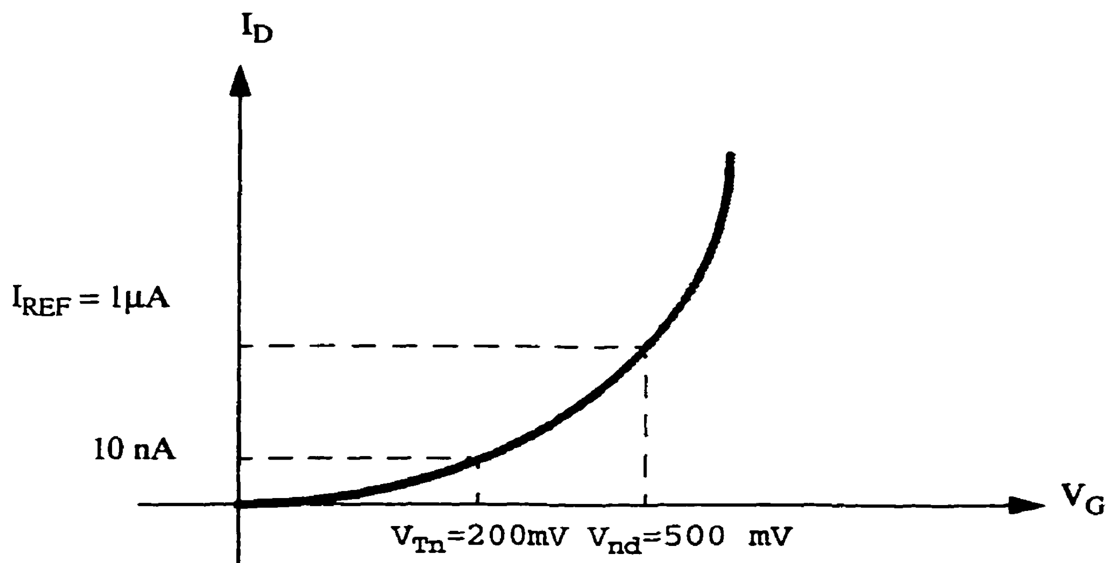


Fig. 4.6 I_D-V_{GS} characteristics of NMOS transistor. V_{Tn} and V_{nd} are compared.

In order to adjust the threshold voltage V_{Tn} of the test NMOSFET device, a positive back-gate bias is needed when V_{Tn} is low (around 0 mV, in which case V_{nd} is around 300mV). A negative back-gate voltage is needed when V_{Tn} is high (around 400 mV, where V_{nd} ranges around 700mV). Therefore, the logic circuit should be able to sense the threshold voltage V_{th} and activate the corresponding charge pump whose output is connected to the back-gate of the test MOSFET. Fig. 4.7 shows the decision circuit. The test transistor is biased by a reference voltage at the gate. The ref-

erence voltages are generated on chip by two or three diode connected NMOSFETs in series between V_{DD} (1 V) and V_{SS} (0 V). The voltages are therefore close to 500 mV and 667 mV respectively. When V_{nd} is lower than 500 mV, both NMOSFETs are off, thus the outputs are pulled high, activating the negative charge pump and shutting off the positive one. In the case of V_{nd} between 500 mV and 667 mV, both charge pumps are disabled since none of them are needed. When the case comes that V_{nd} is beyond 667 mV, positive charge pump is turned om while the negative pump is left off.

The circuits were simulated by SOISPICE-2, which is a version of SPICE2 modified by researchers at the University of Florida and enhanced with a physical model for the fully depleted SOI MOSFET [39][40]. The physical charge-based model for SOIMOSFET, with parasitic BJT and other optional features which can be important for the short channel structure are implemented in SOISPICE-2. The five-terminal (source, drain, front gate, back gate, and body, which normally floats) model is based on the assumption of a fully depleted film body, including the back surface. The SOISPICE MOSFET model includes drain, gate, source, silicon thin film (body) and substrate terminals, and accurately describes floating body effects and back-gate bias effects.

The simulation results of the decision circuits show that the output voltages match expectations under different V_{nd} values. It should be noted that the initial value of V_{nd} was set by arbitrarily adjusting the front gate flat-band voltage (V_{FBF}) in the SOISPICE MOSFET model. In the case of the PMOSFET, the corresponding quantity V_{pd} is adjusted. The values of V_{nd} and V_{pd} corresponding to different values of V_{FBF} are shown in Fig. 4.8 and Fig. 4.9 for NMOSFET and PMOSFET respectively.

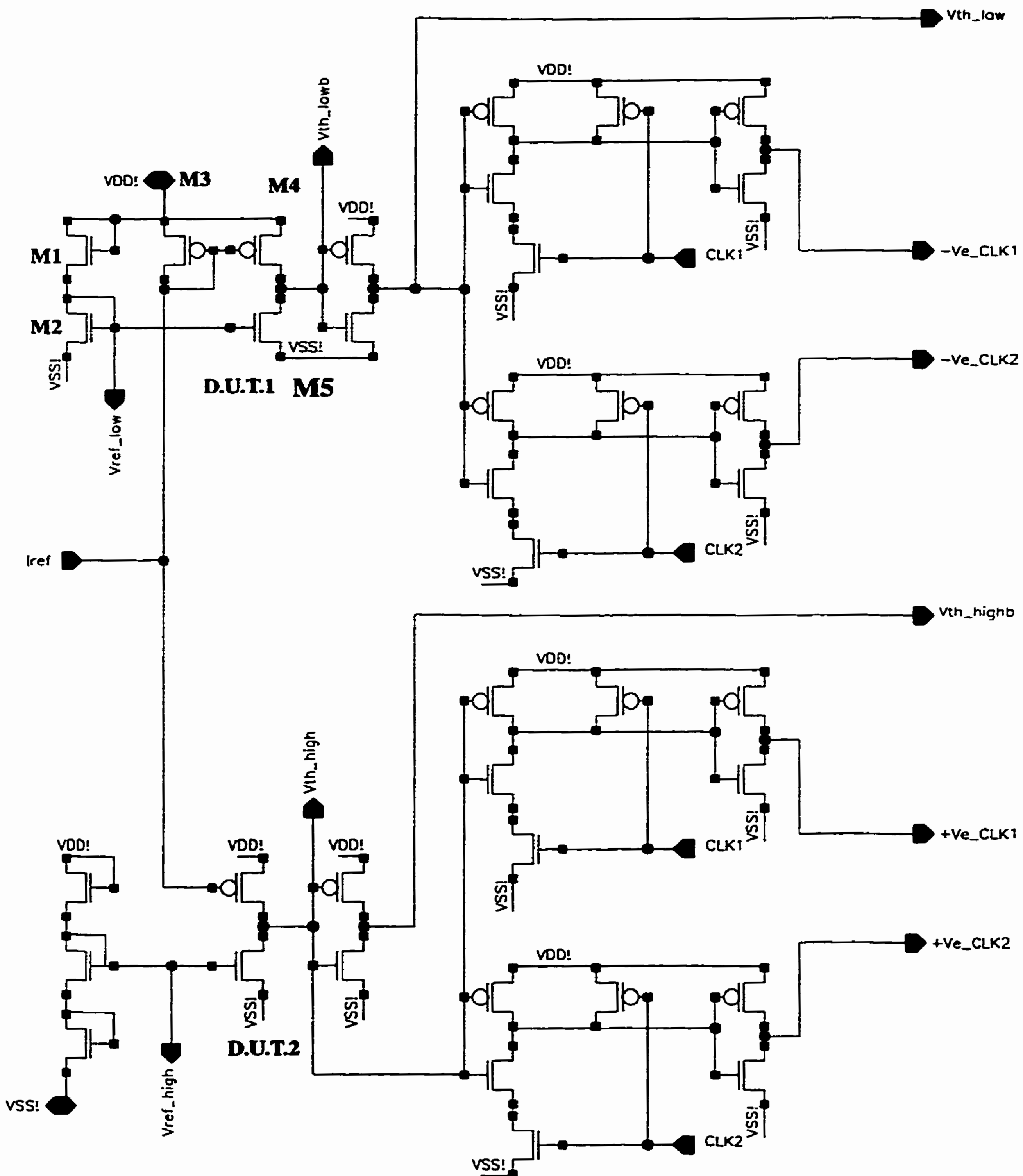


Fig. 4.7 Decision circuit for driving charge pumps (NMOSFET case).

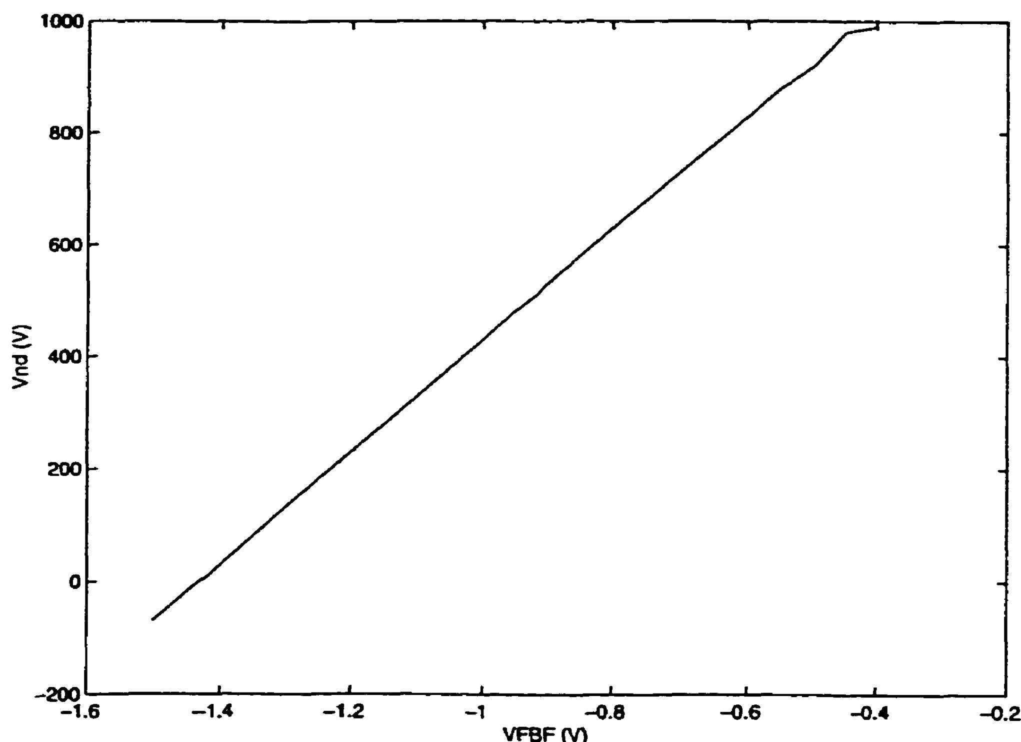


Fig. 4.8 The corresponding value of V_{nd} to V_{FBF} for NMOSFET.

For a given V_{FBF}, the threshold voltage V_{nd} is extracted by recording I_D as a function of V_{GS} for small V_{DS}. For NMOSFET, when I_{DS} starts to grow beyond 1 μA, the corresponding V_{GS} is taken as V_{nd}. For PMOSFET, V_{pd} is defined as the gate voltage where I_{DS} starts to decrease beyond -1 μA.

Table 4.1 shows the voltages at critical nodes under different V_{nd} conditions. For the case of the NMOSFET circuit, which is shown in Fig. 4.7, V_{FBF} is chosen to give three cases: V_{nd} higher than 700 mV, near 500 mV and lower than 400 mV. The node marked as V_{th_low} is the node that should be pulled high by the decision circuit when V_{nd} is too low (~ 300 mV). Meanwhile, node $V_{th_low_b}$ would be pulled low. When V_{nd} is around 500 mV, neither node V_{Th_low} nor V_{Th_high} should be pulled high. For the case of a high V_{nd} (~700 mV), node V_{th_high} should be pulled high and node

$V_{th_high_b}$ pulled low. In SOISPICE simulation, when V_{nd} is low, where a V_{FBF}=-1.1 V is applied (thus V_{nd} =300 mV) with initial conditions of V_{th_low} at logic 0 and V_{th_high} at 1 (which are opposite the desired values), node V_{th_low} is driven high while V_{th_high} is pulled low. This result is exactly as expected. Here zero back-gate bias is applied. The logic levels of these nodes will be used later to trigger the charge pumps to bring up corresponding back-gate voltages.

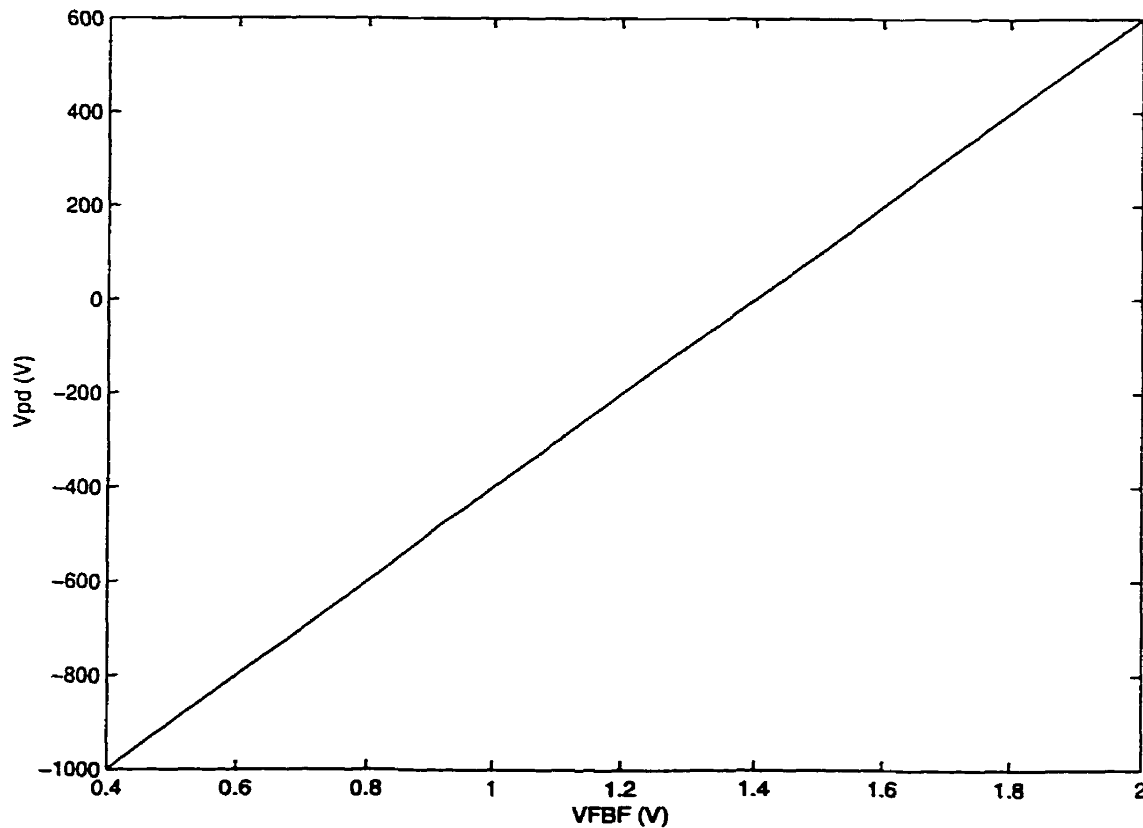


Fig. 4.9 The corresponding value of V_{pd} to V_{FBF} for PMOSFET.

Table 4.1 Logic levels of critical nodes under different V_{nd} and NMOSFET back-gate bias conditions.

V_{FBF} (V)		$V_{th_low_b}$	V_{th_low}	V_{th_high}	$V_{th_high_b}$
-1.1 V_{nd} low	Init. Cond. (V)	1	0	1	0
	Desired (V) $V_{NBKGT} = 0$	0	1	0	1
	Simu. Res.(V) $V_{NBKGT} = 0$	0	1	0	1
	Desired (V) $V_{NBKGT} = -4.4$	1	0	0	1
	Simu. Res.(V) $V_{NBKGT} = -4.4$	1	0	0	1
-0.916 V_{nd} normal	Init. Cond.(V)	0.5	1	0.5	0.5
	Desired (V)	1	0	0	1
	Simu. Res.(V)	1	0	0	1
-0.75 V_{nd} high	Init. Cond.(V)	0	1	0	1
	Desired (V) $V_{NBKGT} = 0$	1	0	1	0
	Simu. Res.(V) $V_{NBKGT} = 0$	1	0	1	0
	Desired (V) $V_{NBKGT} = 4.5$	1	0	0	1
	Simu. Res.(V) $V_{NBKGT} = 4.5$	1	0	0	1

Table 4.2 Logic levels of critical nodes under different V_{pd} and PMOSFET back-gate bias conditions.

V_{FBF} (V)		$V_{th_low_b}$	V_{th_low}	V_{th_high}	$V_{th_high_b}$
1.1 V_{pd} low	Init. Cond. (V)	1	0	1	0
	Desire(V) $V_{PBKGT} = 0$	0	1	0	1
	Simu.Res.(V) $V_{PBKGT} = 0$	0	1	0	1
	Desired (V) $V_{PBKGT} = 4.5$	1	0	0	1
	Simu. Res.(V) $V_{PBKGT} = 4.5$	1	0	0	1
0.916 V_{pd} normal	Init. Cond.(V)	0	0	0	0
	Desired (V)	1	0	0	1
	Simu. Res.(V)	1	0	0	1
0.75 V_{pd} high	Init. Cond.(V)	0	1	0	1
	Desired (V) $V_{PBKGT} = 0$	1	0	1	0
	Simu. Res.(V) $V_{PBKGT} = 0$	1	0	0	1
	Desired (V) $V_{PBKGT} = -4.4$	1	0	0	1
	Simu. Res.(V) $V_{PBKGT} = -4.4$	1	0	0	1

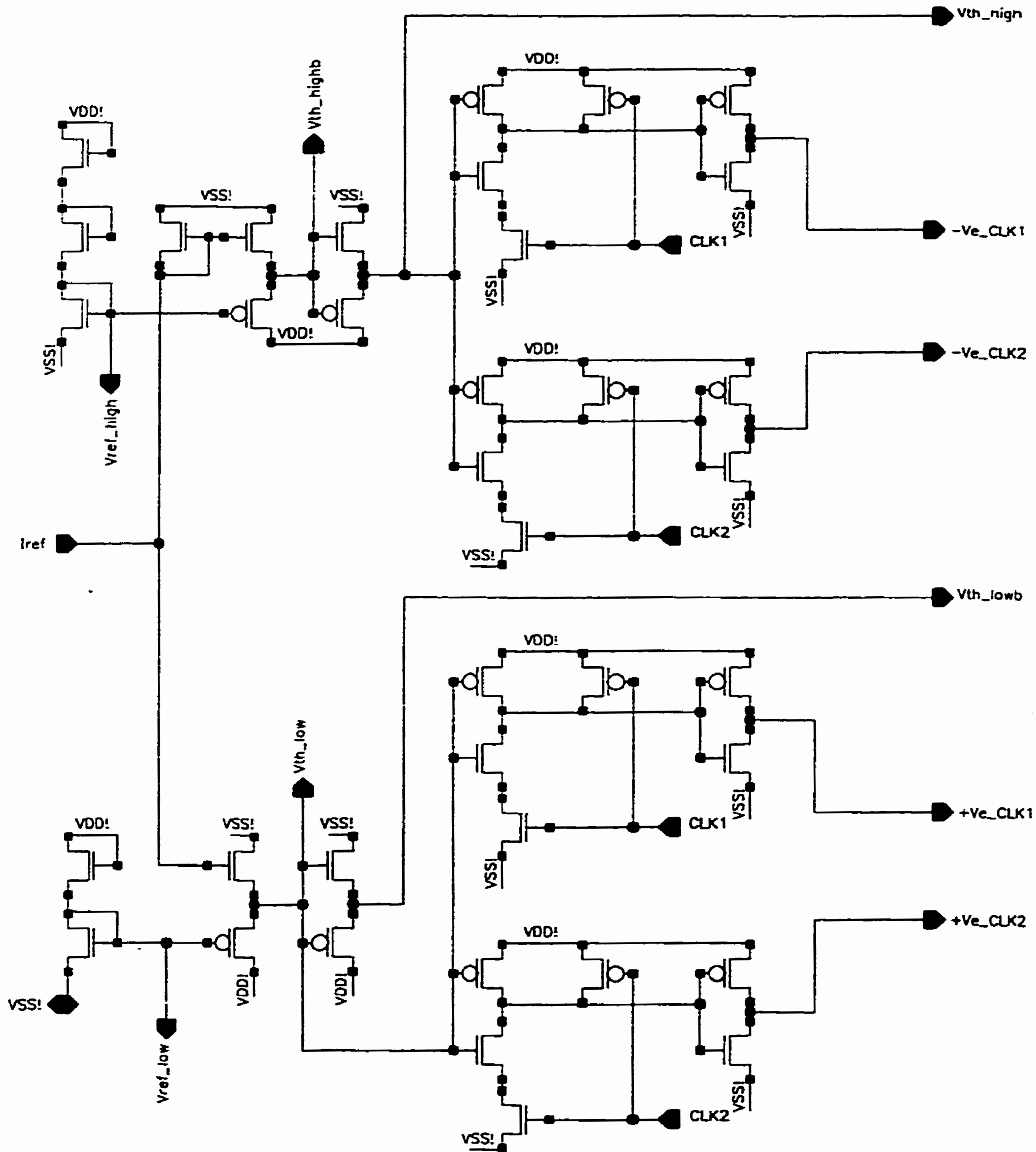


Fig. 4.10 Decision circuit for driving charge pumps (PMOSFET case).

Fig. 4.10 and Table 4.2 shows the PMOSFET decision circuit and logic values of its critical nodes. It is essential to know that the decision circuit would turn off after the back-gate of NMOSFETs is applied with the desired bias for a reasonable period of time. The threshold voltage (or more specifically V_{nd}) would come back to normal value, and therefore the decision circuit output should indicate that the charge pumps are not needed any more.

It is shown in Table 4.1 for the case of the NMOSFET circuit that when V_{nd} is low where a V_{FBF}=-1.1 V is applied (thus V_{nd}=300 mV) and a back-gate bias of -4.4 V is applied, SOISPICE simulation results in both V_{Th_low} and V_{Th_high} being low. This means none of the charge pumps would be triggered. Similar behaviour for both the NMOSFET and PMOSFET decision circuits under various initial V_{nd} and V_{pd} are all shown in Table 4.1 and Table 4.2 with the expectations met.

More SOISPICE simulations were done for the amplifier gain of decision circuit, with the comparison between the deviation of V_{nd} from the nominal value and the circuit output. Fig. 4.11 shows the region where decision circuits starts and stops to work for NMOSFET version. It also shows the gain of threshold voltage deviation. It is shown that the NMOSFET version decision circuit has higher gain when V_{nd} deviates negatively from nominal value than when V_{nd} deviates positively. Analogous results can be obtained for the PMOSFET version circuit.

4•3•2 The Charge Pump Circuit

A charge pump structure similar to the one described in the beginning of Section 4•2 is used as our main pump. Fig. 4.12 (a) shows the schematic of the four stage positive charge pump. This pump drains charge from the V_{DD} supply through p-channel MOSFET M1 connected as a transmission

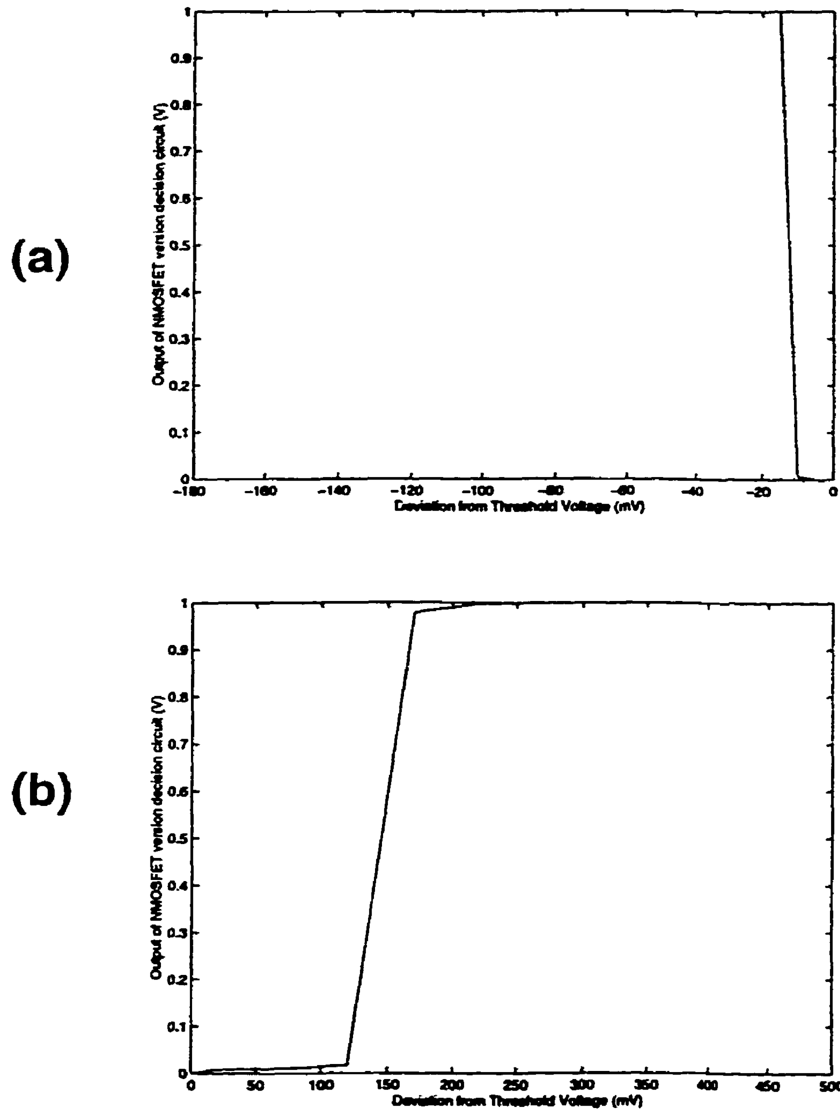


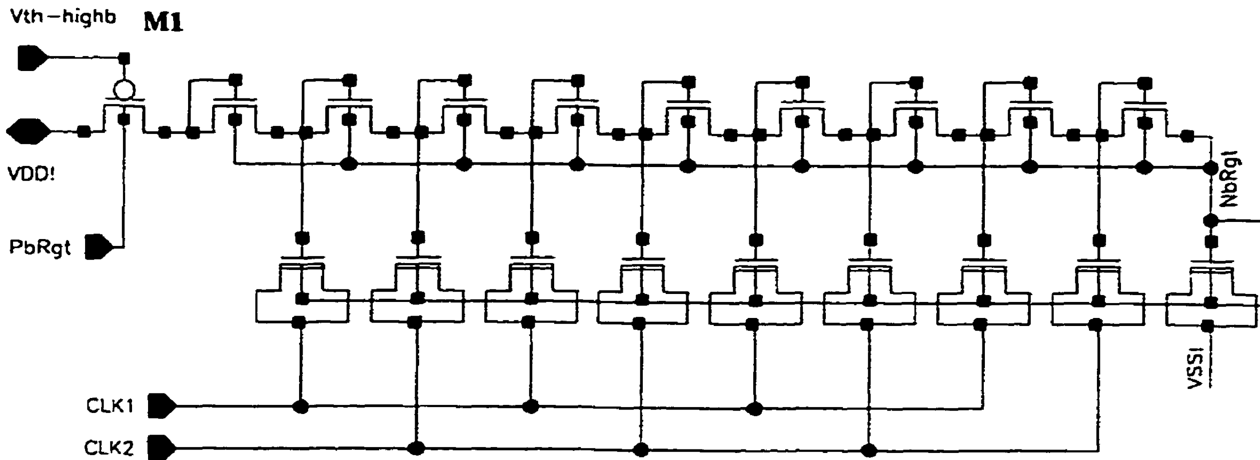
Fig. 4.11 Gain of decision circuit for NMOSFET (a) V_{nd} low (b) V_{nd} high.

gate. The transmission gate is turned on only when the decision circuit concludes that V_{th} for the test MOSFET lies above the target range, and is required since the outputs of both the positive and negative pumps are connected to a common back-gate electrode. Without the transmission gate M1, if the negative charge pump was to be activated, its output would be connected through a chain of

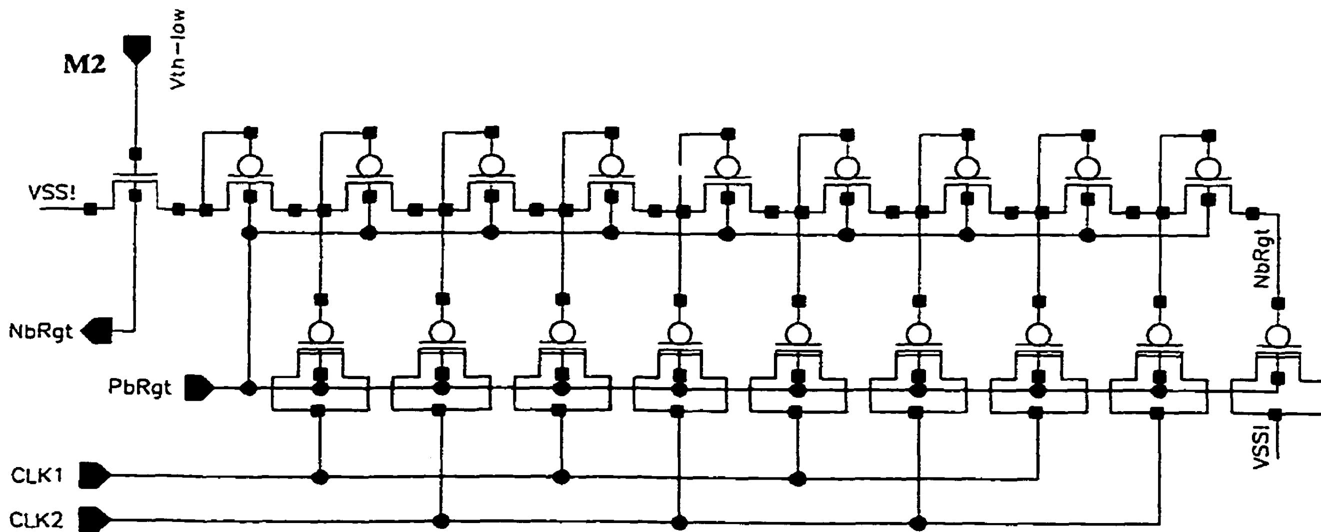
forward biased diodes to the V_{DD} supply. Based on SOISPICE simulations, for a pump with four stages, the output voltage can reach up to 5V under 1MHz clock frequency with reasonable (~ 100 clock cycles which is about 0.1 ms) pumping time. A plot of V_{out} vs time shown in Fig. 4.13.

The negative charge pump schematic is shown in Fig. 4.12 (b). Working in a similar way but opposite direction as in the positive pump, the diodes pump electrical charges from the output node to V_{SS}. Therefore, the output voltage goes below 0 V and becomes negative. N channel MOSFET transmission gate M2 ensures that pump chain is connected to the V_{SS} supply only when the decision circuit calls for a negative back-gate bias to be generated. With same four stage scheme and 1MHz clock signal, the negative pump provides output as low as -5 V within similar time frame taken by its positive counterpart. The SOISPICE simulation results are also shown in Fig. 4.13.

The charge pump circuits described are activated based on the output of the decision circuits. For a NMOSFET version, diode connected PMOSFETs are used for the negative charge pump while its pump capacitors are drain-source shorted depletion PMOSFETs. This structure uses the characteristics of PMOSFET since it is always on as a drain-source shorted capacitor when its gate is at a negative voltage. In order to save space and minimize complexity in layout, diode connected PMOSFETs are used. Four charge pump stages are used in order to bring enough output voltage to the back-gate. The drain-source shorted sides of the pump capacitors are connected to clock signals ϕ_1 and ϕ_2 respectively (marked as -veϕ_1 and -veϕ_2 for negative charge pump circuit). These two clock signals are generated by logical **AND** of the decision circuit output V_{th_low} and off-chip clock signals ϕ_1 and ϕ_2. Thus when the decision circuit decides to turn on the clock signals, the two clock signals -veϕ_1 and -veϕ_2 are generated the same as the original off-chip clock signals ϕ_1 and ϕ_2.



(a) Positive pump, consists mostly of NMOSFETs.



(b) Negative Pump, consists mostly of PMOSFETs.

Fig. 4.12 Schematics of positive and negative charge pumps.

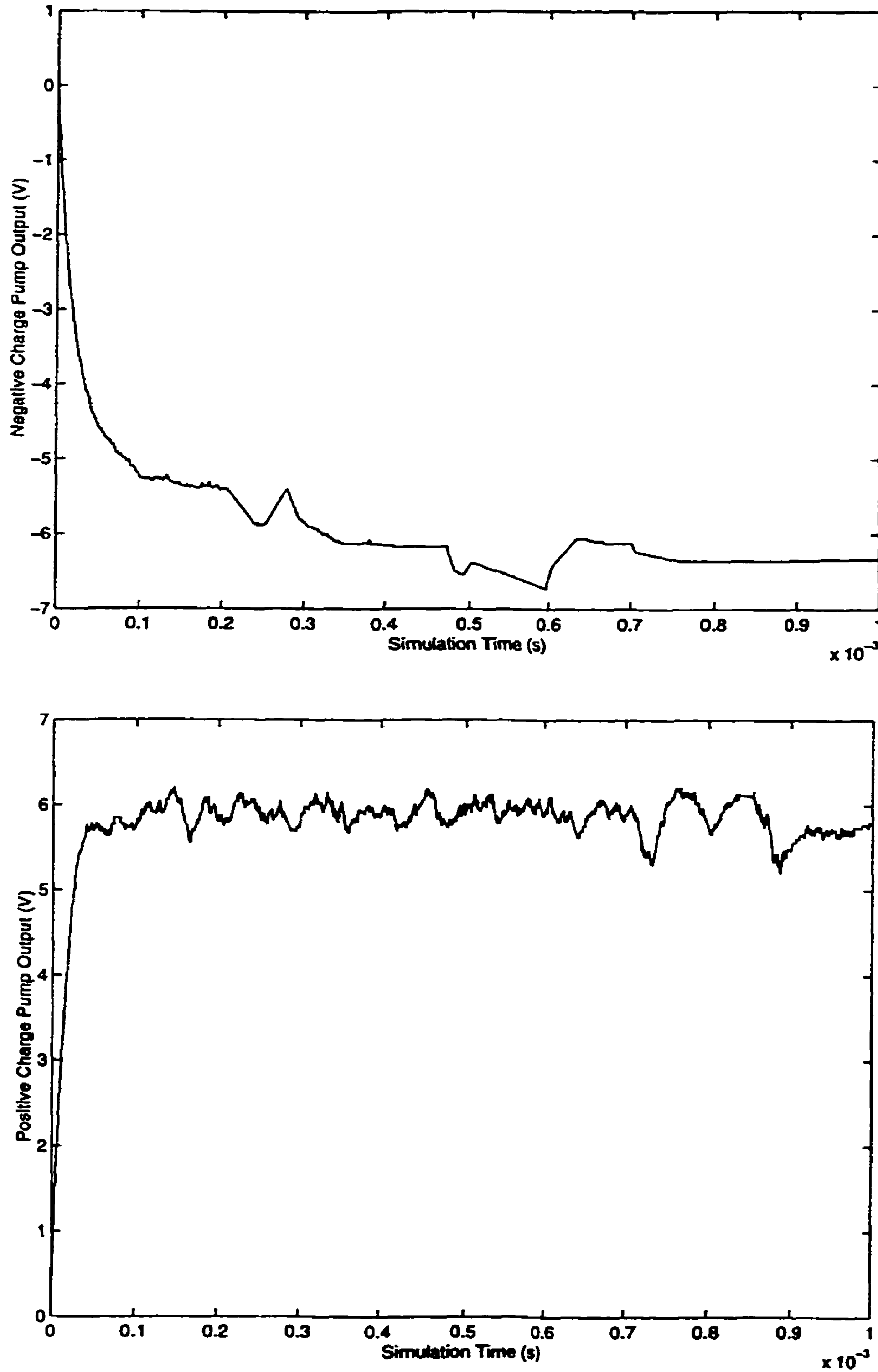


Fig. 4.13 SOISPICE simulation results (V_{out} vs time) of positive and negative charge pumps.

At the same time, the first isolation NMOS is turned on by a high V_{th_low} signal thus providing ground voltage to the first diode of the negative charge pump. In the case of a low V_{th_low} signal, the two regenerated clock signals -veϕ_1 and -veϕ_2 are all low, in addition, the isolation NMOSFET is turned off by the low V_{th_low} signal to prevent contention between the positive and negative charge pumps.

For the positive charge pump, ten stages of diode-connected NMOSFETs are used. The pump capacitors are drain-source shorted NMOSFETs too since their gates are always at higher voltages than V_{DD} (1V). The clock signals of the pump are marked as +veϕ_1 and +veϕ_2, standing for the clock signals for the positive charge pump circuit, which again are logic **AND** of the decision circuit output V_{th_high} and off-chip clock signals ϕ_1 and ϕ_2. The regenerated clock signals +veϕ_1 and +veϕ_2 are both low in the case of a low decision circuit output V_{th_high}, and are the same as off-chip clock signals ϕ_1 and ϕ_2 when V_{th_high} is high. There is a PMOSFET transmission gate at the top of the diode chain as an isolation transistor whose gate is connected to $\overline{V}_{th_high}$ and source to V_{DD}.

SOISPICE simulations were also conducted on the tolerance of V_{nd} for positive charge pump and V_{pd} for negative charge pump. Since the positive charge pump is mostly composed of enhancement and depletion NMOSFETs, the pump output was recorded with V_{nd} varying above and below the nominal value of 500 mV. For the case of the negative pump, the PMOSFET is the dominant device and thus the pump output vs V_{pd} was recorded. Fig. 4.14 below shows the results.

From Fig. 4.14 we find that the output of the positive charge pump decreases as V_{nd} deviates away from its nominal value (~ 500 mV), while the maximum output is obtained when V_{nd} is close to

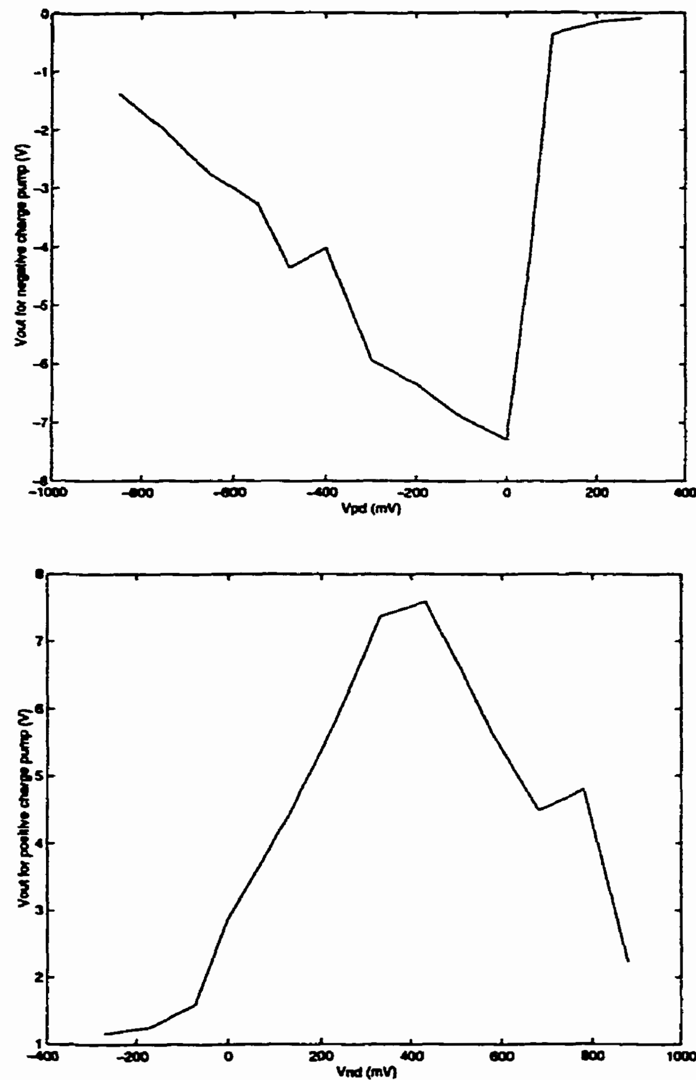


Fig. 4.14 Charge pump tolerance of threshold voltage deviation for the case of positive and negative charge pumps.

its nominal value. For the case of the negative charge pump, when the magnitude of V_{pd} goes higher than the nominal value of -480 mV, its output decreases in magnitude. However, when V_{pd} goes in the other direction, its output voltage increases in magnitude until V_{pd} reaches 0 mV. The output then drops drastically since the PMOSFETs are leaking and cannot hold the charge any more.

4•3•3 The Complete Threshold Voltage Control System

The assembled circuit is composed of the decision circuit described in the previous section and the charge pump circuits. As mentioned before, two on-chip reference voltage generators are implemented by using in-series-diode-connected NMOSFETs which provide reference voltages of 500 mV and 667 mV respectively. The two clock signals ϕ_1 and ϕ_2 are generated offchip. The current source is again provided by an offchip current generator which provides $1\mu A$ current to the test MOSFET through a bonding pad. The outputs of the positive and negative charge pumps are connected together and used as back-gate bias to all the NMOSFETs. As a result, when V_{th} is too low or too high, the output of the charge pumps can provide correcting back-gate-bias to all the NMOSFETs, causing the charge pump to work better when the diode-connected MOSFETs have the correct V_{th}. As to the PMOSFETs used in the NMOSFET version circuit, their back-gate bias is controlled by an off-chip voltage source to guarantee that all PMOSFETs are in the right range of threshold voltage. This way, the complexity of the circuit is reduced, and one needs to only focus on the V_{th} adjustment of one transistor type.

The NMOSFET version of the complete threshold control system is shown in Fig. 4.16, while Fig. 4.17 shows its PMOSFET counterpart. Following the same SOISPICE approach, we simulated the circuits under three different V_{th} initial values controlled by setting of V_{FBF}, both for NMOS and PMOS version of the circuits. The simulation results show that for the NMOS version circuit when V_{nd} is low, the negative pump is turned on to generate negative back-gate bias which starts to pull V_{nd} back to its normal value of around 500 mV. However, because SOISPICE is not a commercial simulation tool, major problems of convergence occurred with the simulations. Only part of this simulation is available. All the other cases failed to converge. Fig. 4.15 displays the simulation re-

sults in the form of V_{out}, *i.e.* the back-gate bias and pump output, versus time under low V_{nd} initial value for NMOSFET version of the circuit. It is shown that the output voltage oscillates toward a negative value. This is an expected result for the complete NMOSFET version of the circuit when V_{nd} is initially low,.

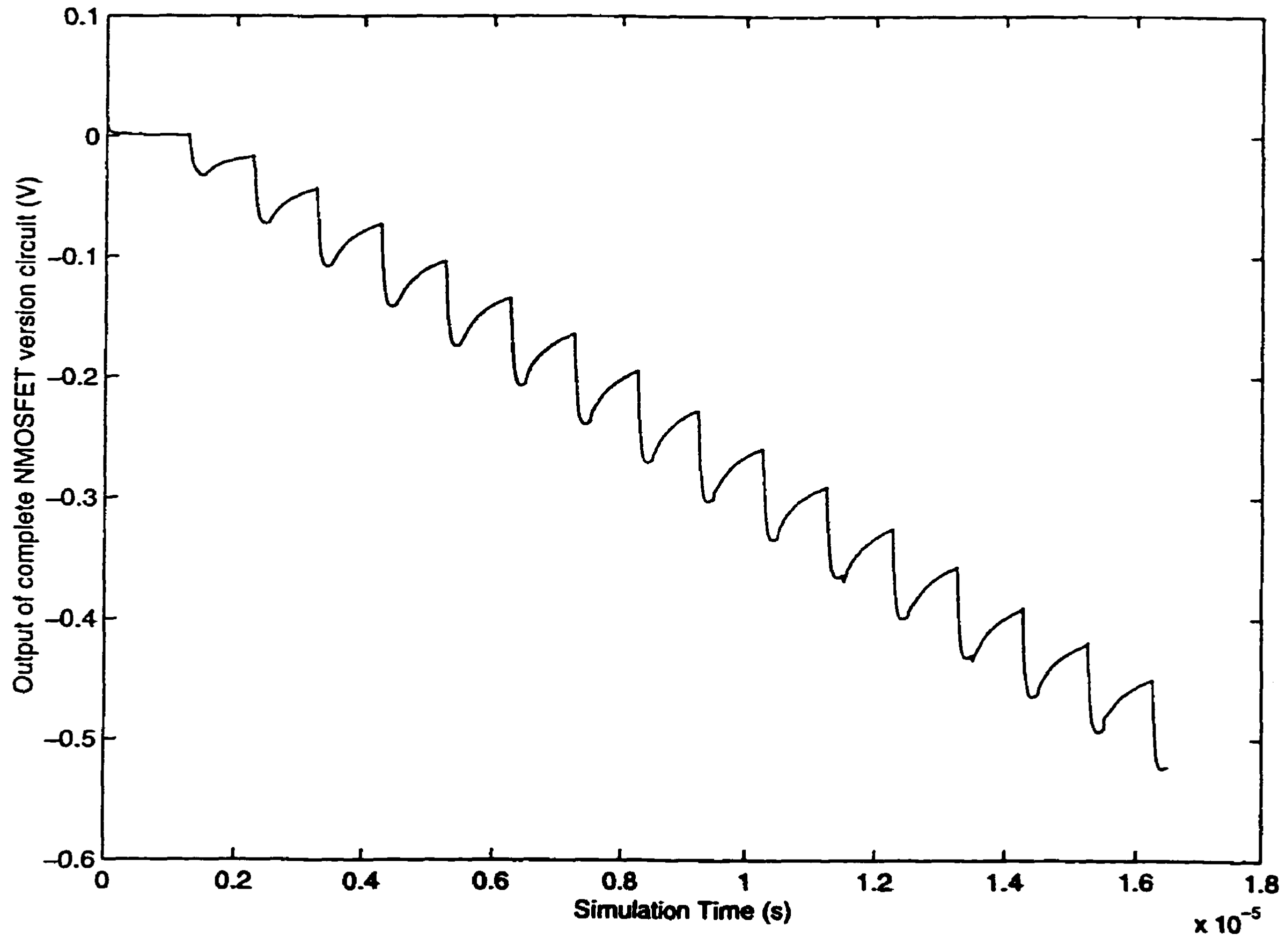


Fig. 4.15 Simulation results in the form of V_{out} vs time under low V_{nd} initial value for NMOSFET control system for Fig. 4.16.

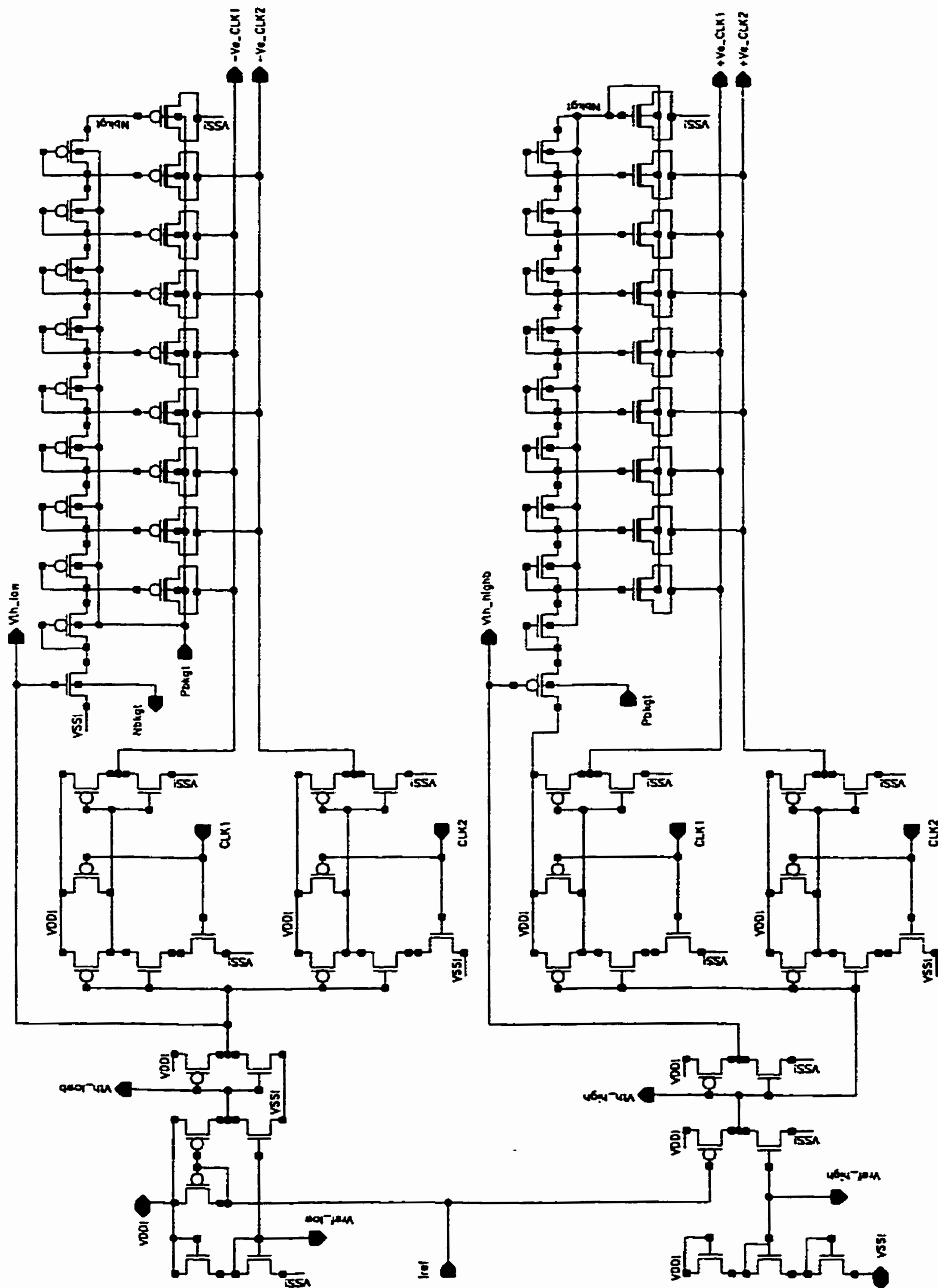


Fig. 4.16 Schematic of the complete NMOSFET threshold voltage control system.

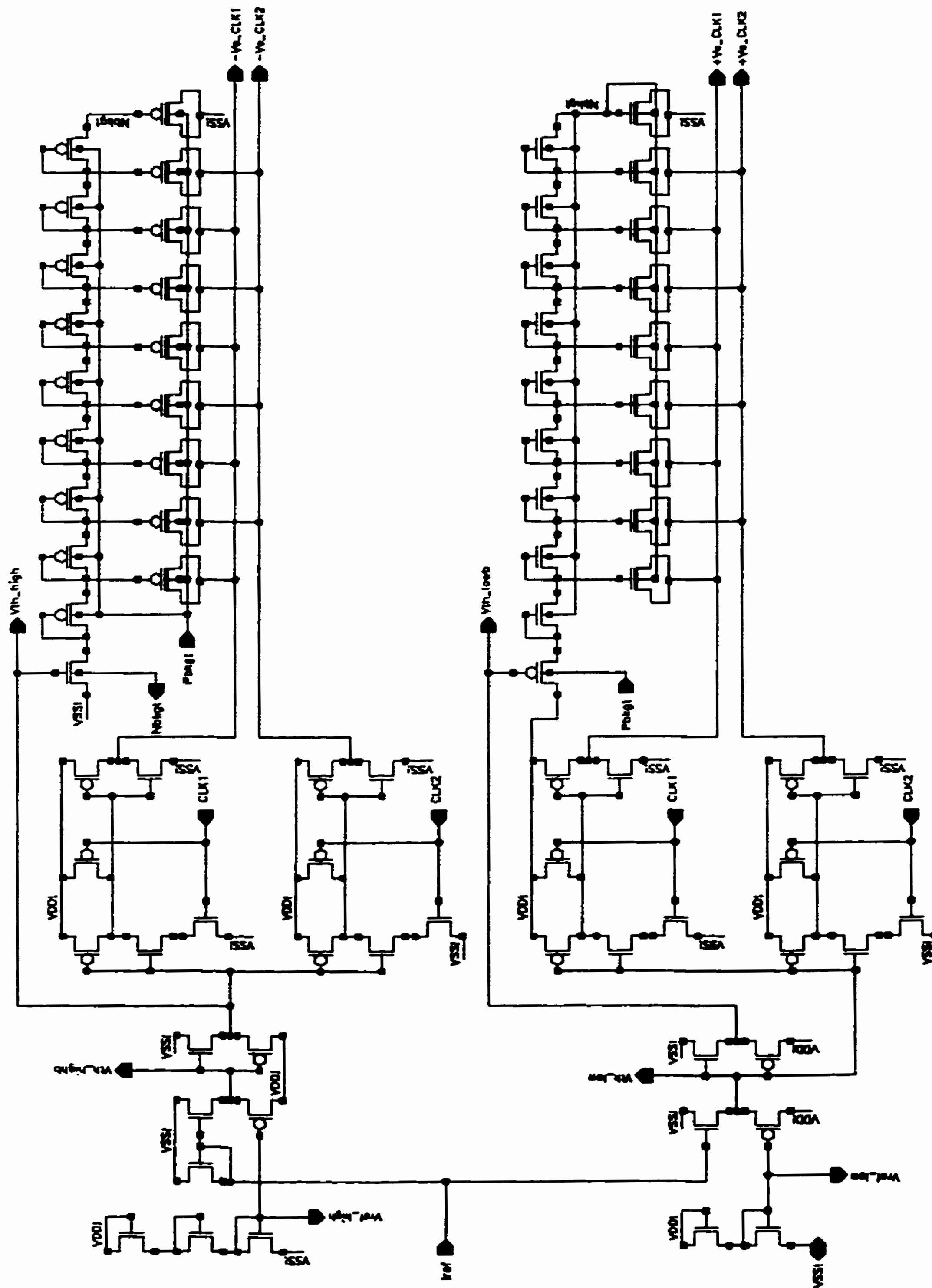


Fig. 4.17 Schematic of the complete PMOSFET threshold voltage control system.

4•4 Circuit Layout

Complete threshold voltage control systems for n- and p-channel transistors were laid out using the L-Edit version 5.6 editor. For this task to be completed, a full layout environment for the FD-SOI technology had to be developed, including design rule checking and circuit extraction. To minimize the number of photo masks which had to be generated and the number of photolithography steps required in processing, the back-gate electrode implants were done through the p-well and n-well masks. This approach requires that two separate back-gate implants be carried out, one for the n-channel and one for the p-channel transistors. This scheme was followed since implant steps are relatively inexpensive compared to photolithography steps.

The eight photo masks required are listed below in the sequence in which they are used:

- The **device well** mask, which is used to pattern the silicon film into active regions by mesa etching.
- The **n-well** and **p-well** masks, which are used to determine which active regions receive n- and p-well implants. These masks also define the areas receiving the back-gate electrode implants.
- The **poly mask**, which patterns the polysilicon gates.
- The **n^+** mask, which defines the areas receiving the heavy n^+ source/drain implant.
- The **buried contact** mask, with opens a window through the buried oxide to the back-gate electrodes prior to the p+ source/drain implant. This minimizes the resistance of contacts to the back-gate electrode.
- The **p^+** mask, which defines the areas receiving the heavy p^+ source/drain implant.
- The **contact** mask opens window through the BPSG to allow metal to contact source, drain and gate regions.

- The **metal mask**, which is used to pattern the single layer of aluminium metalization.

Two derived layers are used for extraction and design rule check. These are the **depletion pmos** and **depletion nmos** layers. As described in Section 4•2, the pump capacitors in charge pump circuits are source-drain shorted PMOS and NMOS transistors. In order to ensure that an inversion layer is always present to form the capacitor plate, depletion PMOS and NMOS transistors are used, and the channel area is therefore n-well for the depletion NMOSFET and p-well for the depletion PMOSFET. Since the extractor would not be able to recognize this type of transistor, two special layers of **depletion pmos** and **depletion nmos** are introduced, which in actual processing revert to p-well and n-well regions respectively. With these new layers, the extractor can recognize the depletion source-drain shorted capacitors and interpret them as source-drain shorted depletion PMOS and NMOS transistors (*i.e.* pump capacitors). Table 4.3 lists all the basic layers and derived layers.

Table 4.3 Basic layers and derived layers of circuit layout.

Layer		Description
Device Well	(Basic)	Boundary of active region, should combine with N^+ or P^+
N-Well	(Basic)	Boundary of N type lightly doped region
P-Well	(Basic)	Boundary of P type lightly doped region
P^+	(Basic)	P^+ region, gives P active when overlapped with Device Well
Metal	(Basic)	Aluminium metal layer, the only metal layer used
Poly	(Basic)	Polycrystalline Si layer for transistor gates
Contact	(Basic)	Connecting metal to gate or metal to active region
Buried Contact	(Basic)	Connecting buried back gate layer to metal
N^+	(Derv.)	= Not P^+ is N^+. N^+ region.
Depletion PMOS	(Derv.)	= P-Well. Depletion PMOS P-Well region.
Depletion NMOS	(Derv.)	= N-Well. Depletion NMOS N-Well region.
Active Contact	(Derv.)	= Contact & Device Well. Contact for source and drain.

Table 4.3 Basic layers and derived layers of circuit layout.

Layer	Description
Poly Contact (Derv.)	= Contact & Poly. Contact between Metal and Poly.
Buried Contact (Derv.)	= Contact & Not Device Well & Not Poly.
Buried Layer (Derv.)	= P-Well or N-Well.
Channel (Derv.)	= Device Well & Poly.

There are special considerations in the layout of charge pump capacitors. According to analysis, the effective capacitance is the gate capacitance of the capacitor while there is parasitic capacitance between the wiring leading to the gate and the substrate. The parasitic capacitance shares the charge with the effective capacitance, thereby decreasing the efficiency of the pump. Interconnections between the diode connected MOSFETs are therefore as short as possible to minimize parasitic capacitance. The pump capacitance is maximized by shaping the device well of the source-drain shorted MOSFETs to a tall slim rectangle perpendicular to the diode direction. In this way, both maximum effective capacitance and minimum parasitic capacitance are obtained.

The layout was constructed in a hierarchical way: subcircuits such as reference voltage generators, decision circuits logic gates and charge pumps were constructed first. Test versions of these subcircuits with input and output metal testing pads were generated and extracted for simulation purposes. After simulation and functional verification, the subcircuits were assembled and interconnected by metal and poly lines. It is a practice in the layout that horizontal connections use metal and vertical ones use poly resulting in lower complexity and higher regularity. In the assembled circuit layout, fifteen probing pads are connected to all inputs, outputs and critical nodes. The inputs include: V_{DD}, V_{SS}, I_{ref}, Φ_1 and Φ_2 as clock signals for the charge pump. The back-gate bias pad PBKGT for PMOS transistors is an input in the NMOS version of the circuit to allow independ-

ent testing of the n-channel and p-channel control circuit. The charge pump output pad of the NMOS version of the circuit allows probing of the back-gate bias NBKGT applied to the NMOS transistors. Probing pads for the purpose of looking into the circuit are: V_{ref_high} and V_{ref_low} for the two on-chip generated reference voltages; V_{th_low} and V_{th_high} for the output of decision circuits, their logic complementary node are probed by pads $V_{th_high_b}$ and $V_{th_low_b}$; -ve_ Φ_1 and -ve_Φ_2 for the two clock signals generated by the decision circuit for negative charge pump and +ve_ Φ_1 and +ve_Φ_2 for the positive pump. Therefore there are a total of 17 pads on the assembled circuit. For testing with a wafer prober, six of these pads are essential inputs, while at least one additional probe is required to sequentially examine the various output.

The L-EDIT layout diagrams for both NMOS version and PMOS version of the complete circuits are shown below in Fig. 4.18 and Fig. 4.19. As described before, eight masks were made for this layout: **Device well, N-well , P-well, P^+, Metal, Poly, Contact** and **Buried-Contact**. Finished devices are not yet available for testing as fabrication of the chip is still under way.

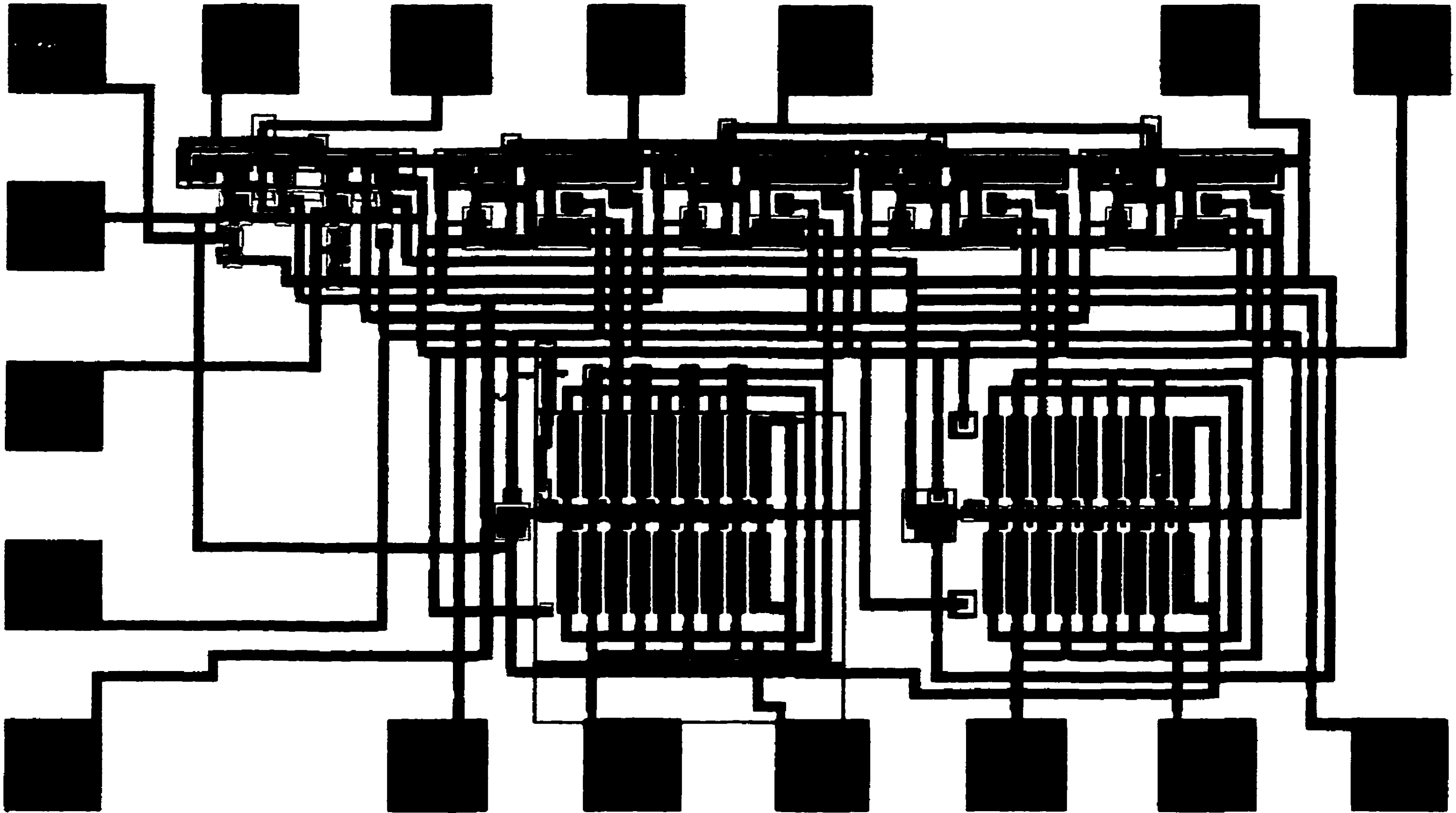


Fig. 4.18 LEDIT layout diagram of NMOS version of complete circuit.

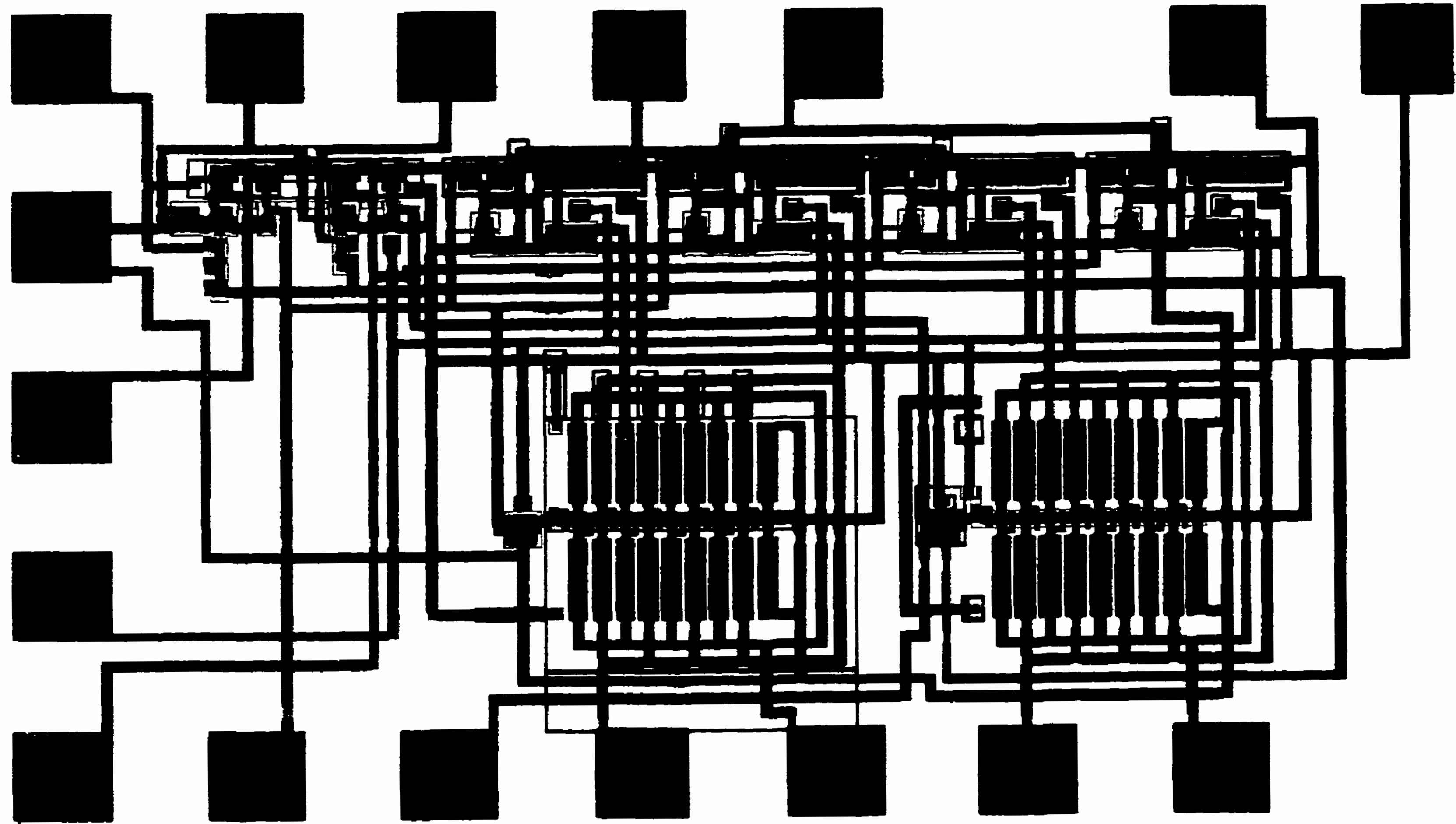


Fig. 4.19 LEDIT layout diagram of PMOS version of complete circuit.

4•5 Scaling Down To 0.25μm Technology

The charge pump circuit discussed in this Chapter is based on 1μm technology. It would be of interest to determine how this circuit would fit into the future generation of technologies, for example, the presently commercially available 0.25 μm technology. A major concern is how much pump output this circuit would give. For the charge pump circuit structure shown in Fig. 4.12, the largest voltage appears across the gate oxide of the capacitor-connected NMOSFET or PMOSFET at the very end of the pump chain. Each device has its gate connected to the pump output and its source and drain grounded.

The gate oxide scaling limits were examined in [41] with respect to time-dependent breakdown, defects, plasma process damage, mobility degradation, poly-gate depletion, inversion layer thickness, tunnelling leakage, charge trapping and gate delay. The operating field was projected to stay around 5MV/cm for reliability and optimum speed. In the 0.25 μm technology generation, the gate oxide thickness might be as small as 4.5 nm [41] which would give us a 2.5 V maximum voltage and limit the charge pump output to approximately ± 2.5 V. Assuming that the front gate and back-gate oxide thicknesses are in the same ratio in the 0.25 μm technology as in the 1 μm technology, a maximum threshold voltage variation of approximately ± 200 mV could be accommodated.

CHAPTER 5

Electrical Characterization of Experimental Devices

This chapter describes the electrical characterization of experimental devices. Tests were carried out on MOSFETs with gate lengths of 5 μm and widths of 25 μm. None of the devices had well contacts in the silicon thin film, so of necessity the well was floating. Parameters such as threshold voltage, subthreshold swing and $\Delta V_{th}/\Delta V_B$ were recorded. The results compared favorably to the simulations.

5•1 Subthreshold Characteristics

Test device electrical characteristics were recorded with an HP4155 Semiconductor Parameter Analyzer. Typical subthreshold characteristics are shown in Fig. 5.1. At $V_B = 0$ the subthreshold swing is 65 mV/decade and $\Delta V_{th}/\Delta V_B$ is 90 mV/V, in reasonably good agreement with SUPREM3 simulation (see Fig. 3.4), while V_{th} is slightly below the nominal target of 200 mV.

Threshold voltage V_{th} values under both dark and light conditions are listed in Table 5.1. V_{th} was determined by finding the tangent to the linear region of the I_D-V_{GS} characteristic at the point of peak transconductance, and taking the intercept of this tangent with the $I_D = 0$ axis. Provided the test device is kept in total darkness, the subthreshold characteristics agree well with those shown in Fig. 3.4 for the case in which the silicon film remains fully depleted of holes.

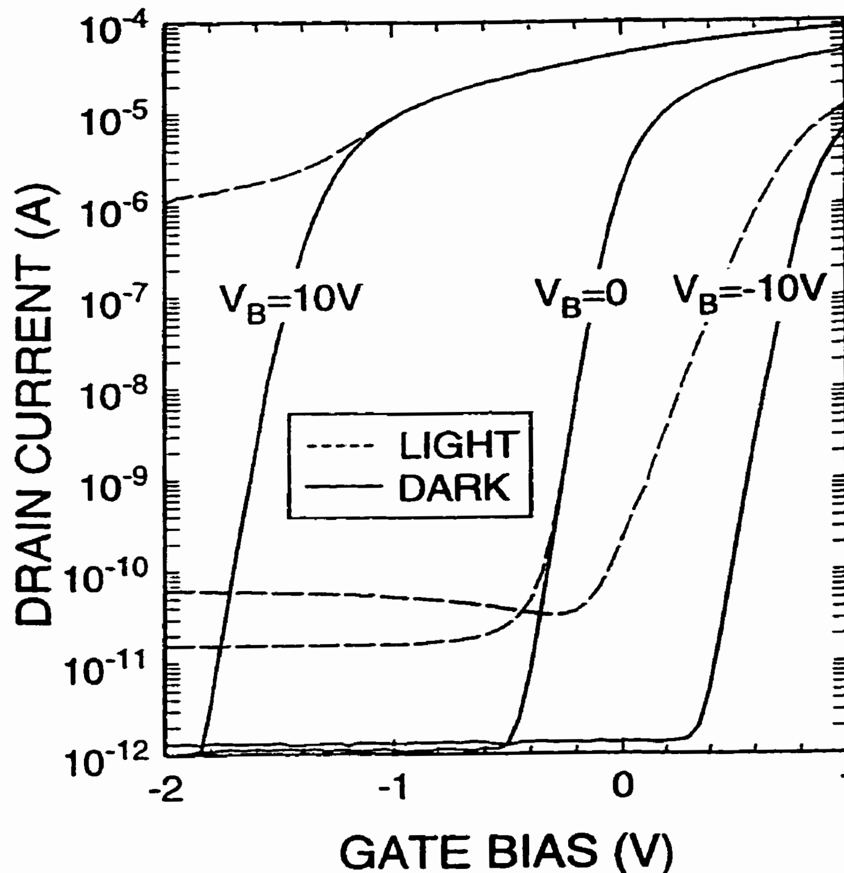


Fig. 5.1 Subthreshold characteristics for experimental back-gated NMOSFET. L_G = 5 μm, W =25μm, 1 μm generation structural parameters. Characteristics are shown for the device in total darkness, and exposed to light from prober microscope.

In order to study electrical characteristics for the case of equilibrium majority carrier concentrations, it is necessary to provide a supply of majority carriers to the thin silicon film. This can best be accomplished with a "T-gate" MOSFET structure of the kind shown in Fig. 5.2. In a T-gate n-channel MOSFET, the channel is attached to a region of the device well heavily doped p-type. An ohmic contact is supplied to this p-type region, effectively serving as a body contact to the silicon thin film. The MOSFET then becomes a five terminal device with contacts to drain, gate, source, substrate (back-gate) and thin film body. Under normal bias conditions in a fully depleted SOI NMOSFET, no holes are present in the silicon thin film. However, if biases

are applied which make it energetically favorable for holes to enter the film, they can readily be supplied from the body contact.

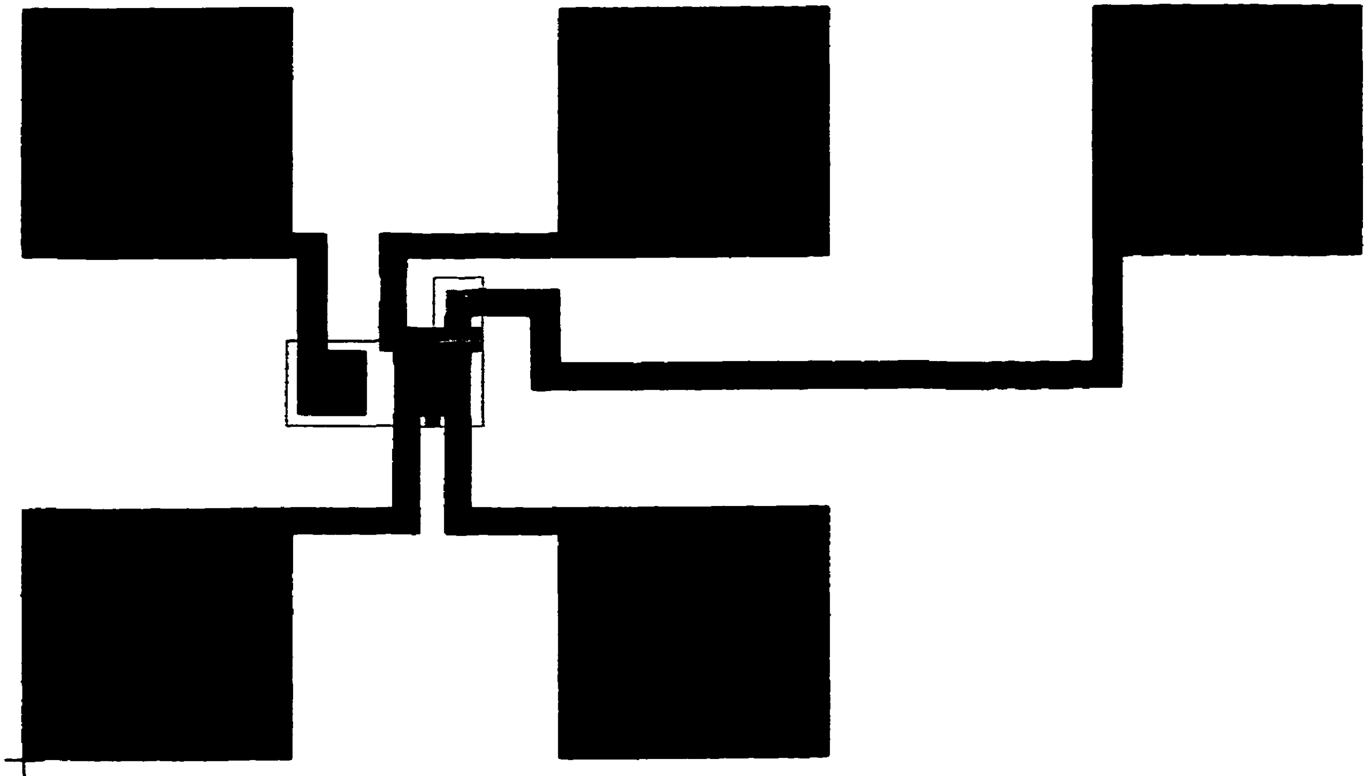


Fig. 5.2 "T-gate" MOSFET structure laid out by LEDIT.

T-gate MOSFETs were not available here since test devices were fabricated in an nMOS-only process (no p+ implant was available). To approximate the characteristics which could be obtained with equilibrium majority carrier concentrations, holes were supplied by illuminating the device with light from the prober microscope.

Table 5.1 Threshold voltage dependence on back-gate bias for NSOIMOSFET experimental device

Dark Case		Light Case	
V_B(V)	V_{th}(mV)	V_B(V)	V_{th}(mV)
-10	836	-10	618
-9	757	-9	609
-8	677	-8	598
-7	596	-7	567
-6	514	-6	508
-5	432	-5	430
-4	349	-4	348
-3	264	-3	264
-2	177	-2	177
-1	88	-1	88
0	-6	0	-6
1	-104	1	-104
2	-202	2	-203
3	-301	3	-301
4	-398	4	-398
5	-493	5	-494
6	-586	6	-587
7	-678	7	-680
8	-769	8	-769
9	-857	9	-858
10	-943	10	-946

Exposure to light from a microscope attached to the wafer prober provided a sufficient carrier generation rate to allow the hole population to reach equilibrium values, leading to the formation of a backside accumulation layer and severe degradation of S for V_B = -10 V, as predicted by SUPREM3. Table 5.1 also reveals that with V_B less than -5 V, the back gate electrode threshold control ability is far less under illumination than in dark. For V_B = 10 V extreme subthreshold leakage which cannot be controlled by the front gate is apparent. SUPREM3 predicts this leakage results from formation of a backside inversion layer and front side accumulation layer in the channel region.

5•2 Drain Characteristics

Fig. 5.3 shows the I_D- V_{DS} characteristics for V_G = 2 V for the device of Fig. 5.1, for V_B =0 and V_B = -10 V. The ability of the back-gate electrode to modify the characteristics is once again apparent. For V_B = -10 V, an unusual "kink" is visible in the characteristic at V_D = 2 V, which is not present for V_B = 0. The kink is believed to result from the onset of a weak avalanche in the drain region. The weak avalanche supplies the holes required to form a backside accumulation layer, which in turn blocks the ability of the back-gate electrode to control V_{th}. As the accumulation layer builds V_{th} falls, increasing I_D. The presence of the kink illustrates that thermal generation is not the only mechanism which can lead to the formation of a hole accumulation layer in an initially fully-depleted silicon film in a practical circuit.

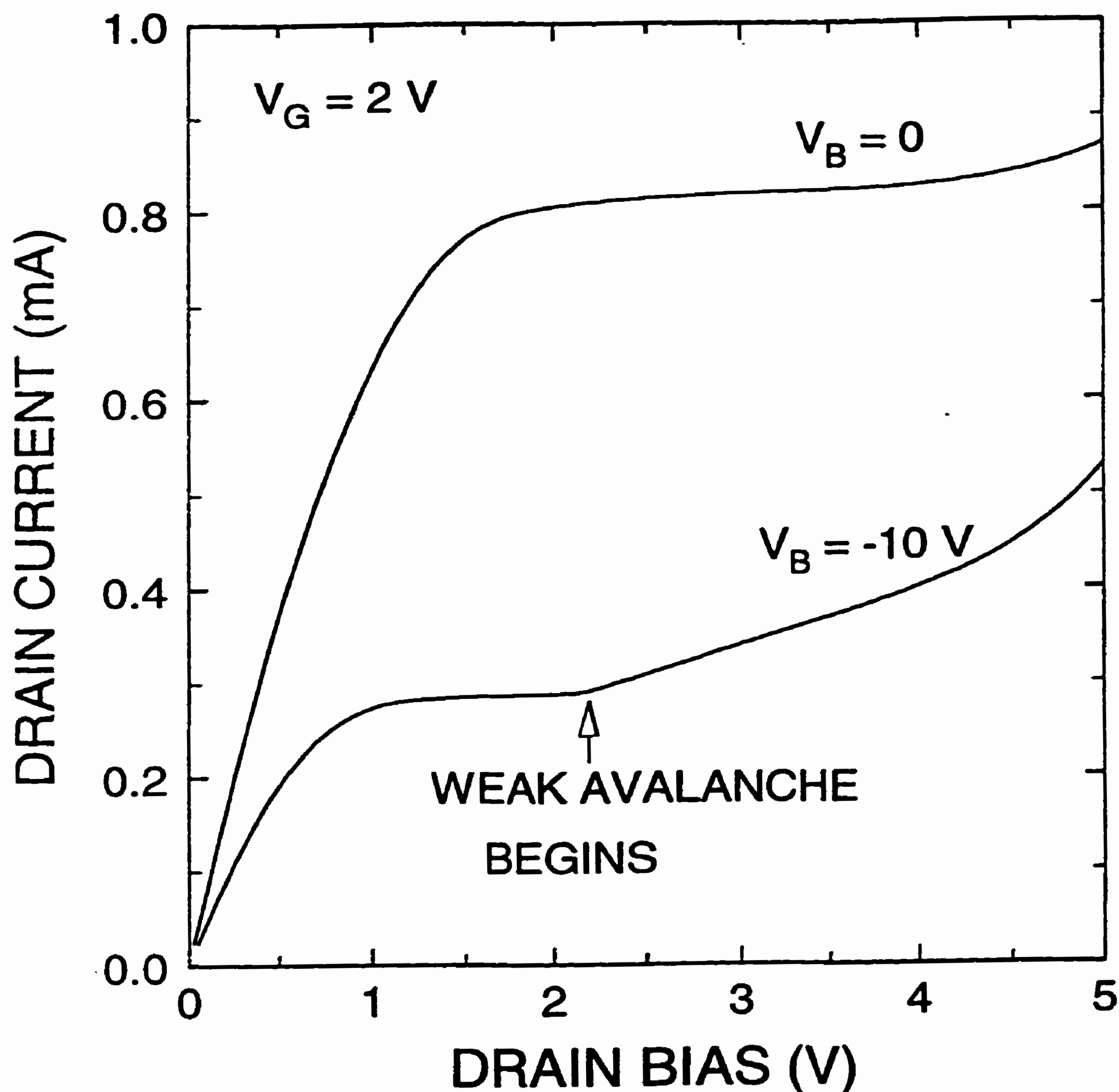


Fig. 5.3 Drain characteristics for device of Fig. 5.1. $V_G = 2$ V, $V_B = 0$ and -10 V.

5•3 Effective Channel Mobility

Fig. 5.4 shows the dependence of the linear region I_D - V_{GS} and transconductance characteristics for the device of Fig. 5.1 on V_B. Given the gate oxide thickness, the effective channel mobility can be obtained from the transconductance characteristics. As V_B is made more negative to raise

V_{th}, the electric field at the silicon film surface is increased, reducing the effective electron mobility $\mu_{n,eff}$ in the channel and lowering the peak transconductance. Measurements on a device with L_G = 25 μm showed $\mu_{n,eff}$ drops from approximately 700 to 650 $cm^2V^{-1}s^{-1}$ as V_B is swept from + 2 to -2 V.

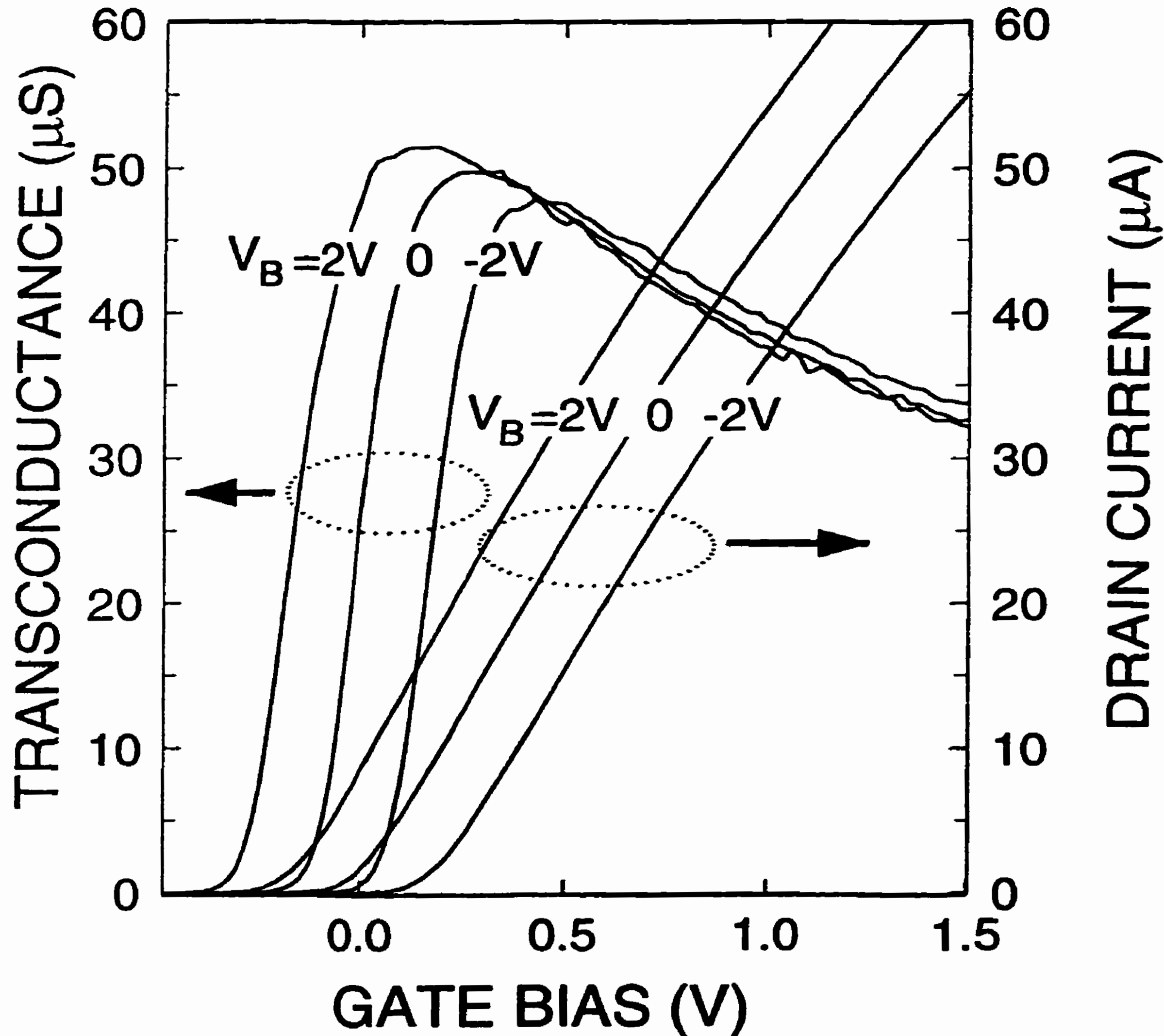


Fig. 5.4 **Linear region and transconductance characteristics for device of Fig. 5.1 for different values of back-gate bias.**

CHAPTER 6
Conclusions

6•1 Conclusions

This thesis has extended earlier studies of threshold voltage control in implanted back-gate FD-SOI MOSFETs by examining physical limitations on the range of V_{th} control which is possible with this structure. Numerical simulation has also been used to study the dependence of $\Delta V_{th}/\Delta V_B$ (the threshold sensitivity to back-gate bias) on buried oxide and gate oxide thickness, silicon film thickness, and back-gate electrode doping. This work has been carried out primarily using the 1-dimensional Poisson equation solver in SUPREM3, with some additional simulation using MEDICI to study short channel effects. Results were reported in Chapter 3.

For a typical SOI MOSFET from a 1 μm technology generation, with a buried oxide thickness of 350 nm and front gate oxide thickness of 25 nm, $\Delta V_{th}/\Delta V_B = 70$ mV/V. $\Delta V_{th}/\Delta V_B$ can be increased by using a thinner buried oxide, but only at the expense of increased parasitic capacitance and subthreshold swing. Further increasing $\Delta V_{th}/\Delta V_B$ does not increase the useful range of threshold voltage control. For n-channel devices, it has been found that the maximum useful negative bias which can be applied to the back-gate electrode is limited by formation of an accumulation layer of holes on the backside of the silicon film. Once the accumulation layer forms the MOSFET behaves like a bulk or partially depleted device, and back-gate control of V_{th} is lost. The maximum useful positive bias is found to be limited by formation of a backside inversion layer which also blocks the back-gate V_{th} controllability. Overall, the useful range of back-gate bias is approximately ±5 V, providing a V_{th} adjustment range of approximately ±300 mV.

Simulation was used to determine whether the implanted back-gate structure would still be useful in the 0.25 μm technology generation. It was found that values of V_{th} and S in the 0.25 μm generation similar to those found in the 1 μm generation can be obtained provided the ratio of front gate to buried oxide thickness is help roughly constant as the technology is scaled down. It was noted that reduction of the buried oxide thickness in this way is already common practice amongst SOI wafer vendors.

The conclusion reached in Chapter 3 was tested by measuring the electrical characteristics of experimental devices fabricated in earlier work in this topic. Satisfactory agreement between theory and experiment was found in the measured values of $\Delta V_{th}/\Delta V_B$ and S, and in the range over which V_{th} could be adjusted.

The main contribution of this thesis is the design of a complete threshold voltage control system for FD-SOI CMOS incorporating implanted back-gate electrodes. The threshold control system includes a decision circuit to activate the charge pumps which supply bias to back-gate electrodes and hold V_{th} within range. Design of the charge pumps presented a considerable challenge due to the necessity of generating output voltages considerably larger in magnitude than the supply voltage in order for the system to be useful for 1 V supply operation. This challenge was met by adopting the charge pump design of Dickson [38], and paying careful attention to the minimization of parasitic capacitance. Depletion nMOS transistors required for pump capacitors were formed in n-well regions, requiring no extra processing operations.

Complete threshold voltage control systems for both n- and p- channel transistors were laid out us-

ing LEDIT and submitted for processing in Carleton's Microelectronic Fabrication Facility. Finished circuits are not yet ready for testing. In the absence of an experimental test, L-EDIT was used to extract the circuit for the layout. The extracted circuit was extensively simulated with SOISPICE. The SOISPICE simulations predicted that all the basic building blocks for the control systems should be functional. It was found that the n-channel control system should be able to return V_{th} to a nominal value of 200 mV starting from initial values ranging from -100 mV to +500 mV. Similar results were found for the p-channel control system. The charge pumps should be able to provide output voltages of up to ± 5 V for 1 V supply operation.

The main obstacle in scaling charge pump threshold voltage control systems to the 0.25 μm generation and beyond is expected to be breakdown of the gate oxide in the pump capacitors. For example, the maximum voltage which can be sustained across the gate dielectric in a 7 nm gate oxide thickness, which might be encountered in the 0.25 μm generation, is just 2.5 V.

6•2 Recommendations for Further Study

Given the convergence difficulties in SOISPICE simulations, there is still much to be done to deal with the SOISPICE simulation of complicated SOI MOSFET circuits. One possible solution might entail the development of approximate models in HSPICE for simulation convergence. In addition, testing of the fabricated circuits should be conducted to compare with the SOISPICE simulation results as the continuation of this work. Testing of "T-gate" MOSFET structures described in Chapter 5 would directly compare the threshold voltage controllability between fully depleted and partial depleted SOI MOSFETs.

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