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CMOS Compatible Power MOSFETs for On-Chip DC/DC Converters

by
Sameh G. Nassif-Khalil

A thesis submitted in conformity with the requirements
for the Degree of Master of Applied Science
Department of Electrical and Computer Engineering
University of Toronto
1999

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CMOS Compatible Power MOSFETs for On-Chip DC/DC Converters

Master of Applied Science, 1999
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Abstract

This thesis deals with low-voltage power MOSFETs which are used in portable, high-efficiency switch mode DC/DC converters for personal digital assistants (PDA's) applications. Two power MOSFETs based on lateral, low-voltage CMOS processes and capable of carrying 1 A of current in the on-state are investigated in this thesis.

The first device uses a 0.8 μm single level metallization CMOS process. The unit cell pitch of the MOSFET switch is 4.1 μm using a channel length of 0.8 μm. The layout of a power switch with 1 A current carrying capability uses a checkerboard pattern to maximize the channel width per unit area resulting in a total active chip area of 290×290 μm^2 corresponding to a total channel width of 31,878 μm. Simulations results of the unit cell show that a specific on-resistance of 117.46 $\mu\Omega.cm^2$, device on-resistance of 90.1 mΩ and total gate charge of 0.34 nC can be achieved.

The second device uses a 0.25 μm - 5 level metallization commercial CMOS process. Experimental results for the 0.25 μm switch show significant performance improvement over the 0.8 μm design. A specific on-resistance of 6.822 $\mu\Omega.cm^2$ is achieved using a cell pitch of 1.85 μm. The layout of the switch utilizes a checkerboard pattern resulting in an active chip area of 130×130 μm^2 corresponding to a total channel width of 12,499 μm. Experimental results also show that the switch achieves a rise and fall time of 5.8 and 3.5 ns, respectively, an on-resistance of 40.37 mΩ and a total gate charge of 0.105 nC.

Acknowledgments

I would like to express my sincere appreciation and gratitude to Professor C. A. T. Salama for his insightful guidance, encouragement and support throughout the course of this work.

My thanks to the clean room staff: Dod Chettiar, Dana Reem and Richard Barber for their technical assistance and cooperation. Assistance from Jaro Pristupa in numerous occasions (not only in software) deserves special thanks. Also thanks to Professor Wai Tung Ng for his insightful advice.

I would like to thank my friends Shahla Honarkhah and Sotoudeh Hamedi-Hagh for very valuable discussions and advice both technically and personally.

My appreciation is extended to every member of the Integrated Circuit Laboratory for a very pleasant working environment. Thanks go to Naoto Fujishima, Diana Gradinaru, Jeewika Ranaweera, Mehrdad Ramezani and Dusan Suvakovic. My thanks also go to my friend Monica Bettich.

Financial support provided by the Natural Sciences and Engineering Research Council of Canada, MICRONET, Gennum Corporation, Mitel, and Nortel is greatly appreciated.

Last, but not least, I would like to especially thank my mother and my sister for their love and support and to take this opportunity to dedicate this thesis to my father whose devotion and support throughout the years deserve special acknowledgments and appreciation.

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CHAPTER 1

Introduction

In low voltage portable applications, the increase in chip densities and frequency of operation is resulting in higher power requirements. These requirements have a significant impact on system performance associated with reduced battery life-time and have created demand for high efficiency switch mode DC/DC converters to power these systems. These converter modules must also satisfy stringent requirements for compact size and light weight.

To reduce the size and weight of the modules, the size of the reactive components which account for a significant volume of the converter must be reduced. This can be done by increasing the switching frequency[1], however, the price is increased power losses in the semiconductor power switch. In order to enable operation at high switching frequency, the converter efficiency and particularly the power switch efficiency must be improved.

Power converters are presently operating at 300-1000 KHz switching frequencies and are implemented using discrete vertical power MOSFETs, a gate driver IC controller and a low pass filter assembled as an integral part of board-mounted systems. Reported efficiencies range between 92% at 300 KHz to 86% at 1000 KHz. The drop in efficiency at high frequencies is related to losses in vertical power MOSFETs attributed to the inherent high on-resistance and large Miller feedback capacitance associated with the vertical structure. This imposes serious limitations on higher frequency switching operation.

Future converters are expected to be implemented on-chip with projected switching frequencies above 10 MHz and require a new generation of high speed, high efficiency, low

voltage lateral power MOSFETs that can be implemented using VLSI compatible processes.

On-chip monolithic implementation of a switch mode DC/DC converter is quite attractive because of its favorable impact on system reliability, performance and cost due to reduced parts count, area savings and elimination of external interconnects.

The reason for choosing MOSFET's rather than bipolar transistors for the implementation of the converter switch is due to the inherent advantages of the former in low voltage switching applications [2,3,4]. These include: 1) high input impedance that considerably simplifies the gate drive circuitry and improves the efficiency, and 2) fast switching speed associated with the lack of the minority carrier storage effects and 3) negative temperature coefficient of current, hence, no thermal runaway.

1.1 Power Losses in Switch Mode DC/DC Converters

Most portable systems utilize switch mode DC/DC converters known as step-down (buck) converters to convert a higher input voltage into a lower output voltage. The main building blocks of the buck converter are illustrated in Fig. 1.1.

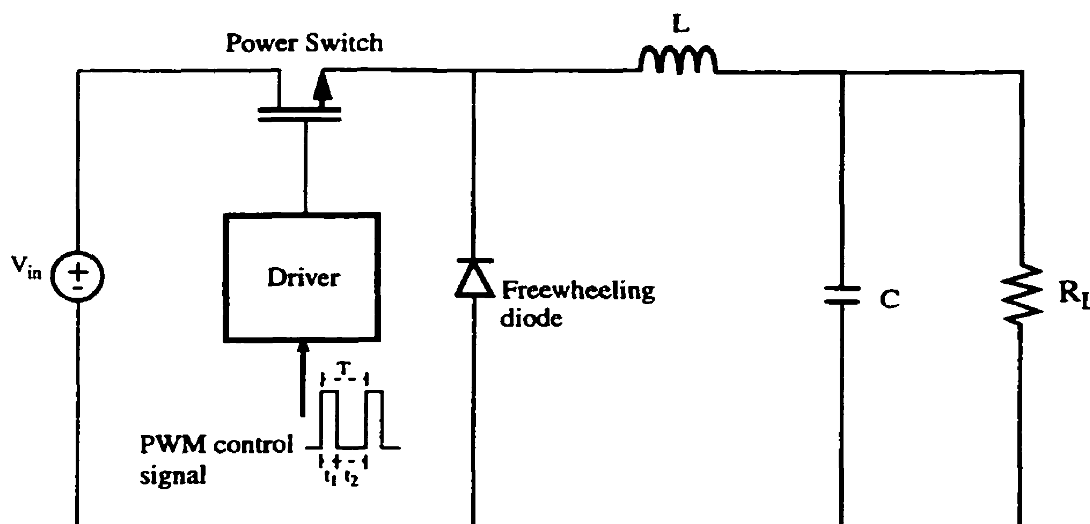

Fig. 1.1: Switch mode DC/DC converter

The gate of the power switch is driven by a pulse width modulated (PWM) control signal, that results in one of three possible states of operation for the switch:

i) The off-state: The gate voltage is low and the power switch is turned off. The device should be able to support a voltage larger than the supply voltage. This voltage is termed the forward blocking capability of the switch. The power losses due to the leakage current in the off-state are relatively small and can be assumed zero.

ii) The switching state: The switch is in a transition period and switches form one state to the other as dictated by the gate driver voltage. An ideal switch exhibits an instantaneous transition (zero turn on and turn off times), however, a real switch exhibits finite switching time due to the charging and discharging of the input capacitance associated with the gate of the MOSFET structure, this in turn results in dynamic power dissipation known as the switching loss. The input capacitance C_{iss} is voltage dependent and is equal to $C_{gs} + (1+A_v)C_{gd}$ where C_{gs} is the gate to source capacitance, the term $(1+A_v)C_{gd}$ accounts for feedback capacitance and A_v is the forward voltage gain in the common source configuration. Another source of power dissipation occurring during the switching mode of operation is the gate drive loss and is associated with the gate resistance R_g as shown in Fig. 1.2[5]. This resistance is arising from the gate electrode internal to the device[6] and is responsible for power dissipation during the charging or discharging of the input capacitance C_{iss}.

iii) The on-state: The gate voltage is high and the power switch is conducting in the triode region. During the on-state the switch behaves as a finite resistor defined by the device on-resistance, that is, the total resistance between the source and the drain contacts. The current passing through the switch is the on-current I_{on} and the voltage across it is the $V_{ds\text{-}on}$. Ideally the on-resistance and therefore $V_{ds\text{-}on}$ should be zero, however, a real switch has a non-zero on-resistance and therefore dissipates a finite amount of power (conduction losses)

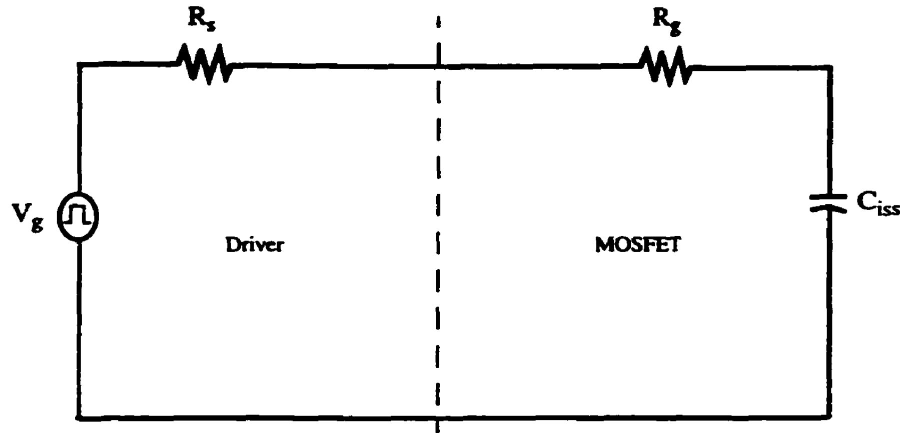

Fig. 1.2: Gate drive equivalent circuit

The total power dissipation P_d in a MOSFET switch can be expressed as

$$P_d = f_s\left(I_{on}^2 R_{on} t_1 + t_{on}\int_0^{t_{on}} v_{on}(t)i(t)dt + t_{off}\int_0^{t_{off}} v_{on}(t)i(t)dt + \frac{R_g}{R_g + R_s} V_{gs} Q_g\right) \quad (1.1)$$

where f_s is the switching frequency of the MOSFET, I_{on} is the switch current during conduction, R_{on} is the switch on-resistance, t_1 is the switch conduction time, t_{on}, t_{off} are on and off switching time, R_g is the gate resistance of the switch, R_s is the driver circuit output resistance, V_{gs} is the peak voltage at the gate and Q_g is the peak gate charge that is required to completely switch the device.

The first term in equation (1.1) represents the conduction losses in the switch and is proportional to the device on-resistance which in turn is dependent on the device structure, doping profile, gate voltage and temperature. The second and third terms represent the switching losses which are proportional to the switch turn-on and turn-off times and hence depend on the input capacitance of the MOSFET. The last term represents the gate drive loss dissipated internally in the MOSFET gate resistance and is proportional to the total gate charge Q_g.

From the above discussion, it can be seen that the total losses are directly proportional to the switching frequency implying that while the increase of operating frequency is desirable to reduce the size of capacitance C and inductance L in the converter circuit of Figure 1.1, it has a negative impact on the total power losses in the semiconductor switch. This represents the most important trade-off in designing switch mode converters.

1.2 Current status of Power MOSFET switches

Traditionally, MOSFET switches in DC/DC converters are implemented in either Planar Vertical Double Diffused MOSFETS (VDMOST) or Trench MOSFETS (TMOST) [8],[9]. In the VDMOST, shown in Fig. 1.3, current emanating from the source flows laterally along the surface, then vertically between adjacent P-body diffusions, through the epitaxial drain and substrate and out the wafer's backside. This long path of current flow translates into a large on-resistance. In other words, VDMOST devices suffer from inherent high on-resistance due to substrate, epi-layer and parasitic JFET pinch resistance (between the two adjacent body region)[8]. Reduction of the on-resistance can be achieved by increasing the packing cell densities through scaling down of the surface geometry.

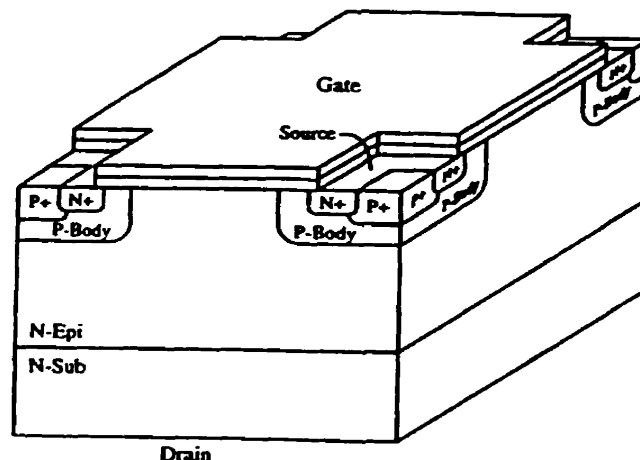

Fig. 1.3: Vertical DMOST cross section

To solve the problem associated with the parasitic JFET effects in VDMOS devices, the TMOST shown in Fig. 1.4, was proposed [10]. The current flow is still vertical along the sidewall of the trench. While the TMOST solves the JFET problem, reduction in the on-resistance is still limited by the substrate and epi-layer resistances.

Finally, the incompatibility of vertical power MOSFETs with standard CMOS or BiCMOS processes makes them unsuitable for monolithic implementation of high frequency switching mode DC/DC converters.

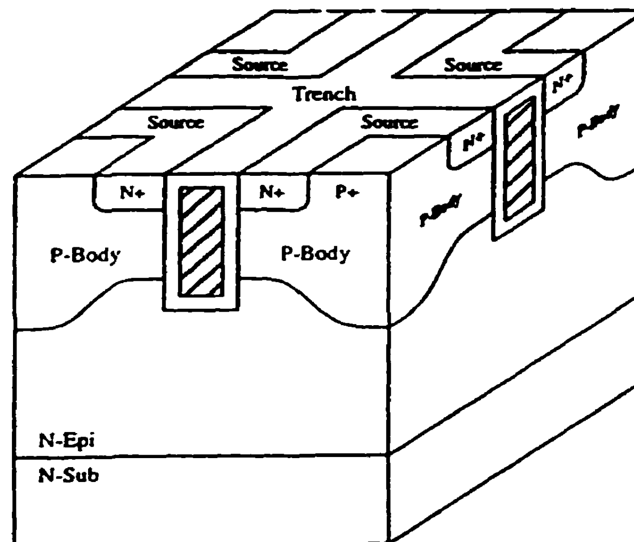

Fig. 1.4: TMOST cross section

1.3 Lateral Power MOSFETs

In low voltage converter applications, high breakdown voltage is not a requirement since the switch needs to support a low voltage (less than 5 V) when it is in the off-state. This fact makes the implementation of lateral Power MOSFETs in a VLSI technology very attractive. The advantages of lateral power MOSFETs, shown in Fig. 1.5, are:

i) ease of integration into VLSI compatible process,

ii) low total gate charge Q_g, gate to source and gate to drain capacitances, and

iii) low on-resistance associated with high packing density and lateral current flow[1].

Lateral devices implemented using a VLSI process can take advantage of aggressive design rules which in turn reduce the cell pitch, increase the cell packing density resulting in low specific on-resistance $R_{on} \cdot A$. The on-resistance also determines the device area for a given current handling capability requirement in the on-state. Since the input capacitances C_{gs} and C_{gd} are proportional to the total area of the device, aggressive VLSI technologies result in low input capacitances and total gate charge Q_g.

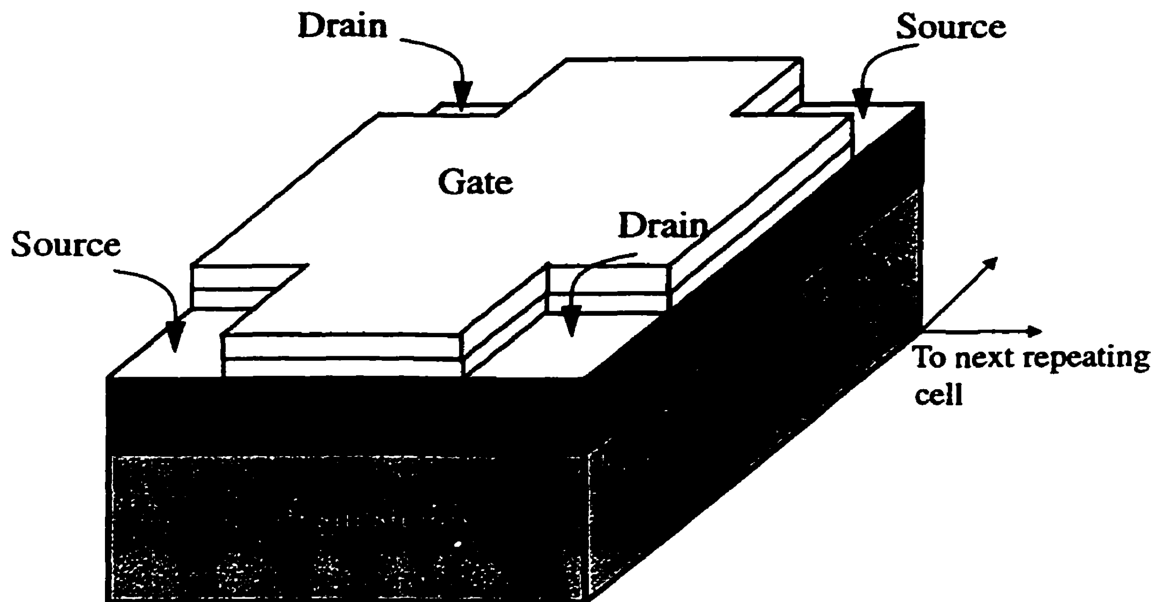

Fig. 1.5: Lateral MOSFET cross section(unit cell)

1. resistance contributions due to substrate and JFET pinching effect are eliminated.

1.4 Figure Of Merit for Power Switches

To compare the performance of different power devices, a Figure of Merit (FOM)[11] is commonly used by power MOSFETs manufacturers and is defined as

$$FOM = R_{on} \times Q_g \qquad (1.2)$$

where R_{on} is the device on-resistance and Q_g is the total gate charge when the device is completely switched on. The value of Q_g can be extracted from the charge transfer characteristics, shown in Fig. 1.6, which is a plot of the gate to source voltage V_{gs} versus the gate charge Q_g. This curve can be obtained using the test circuit shown in Fig. 1.7.

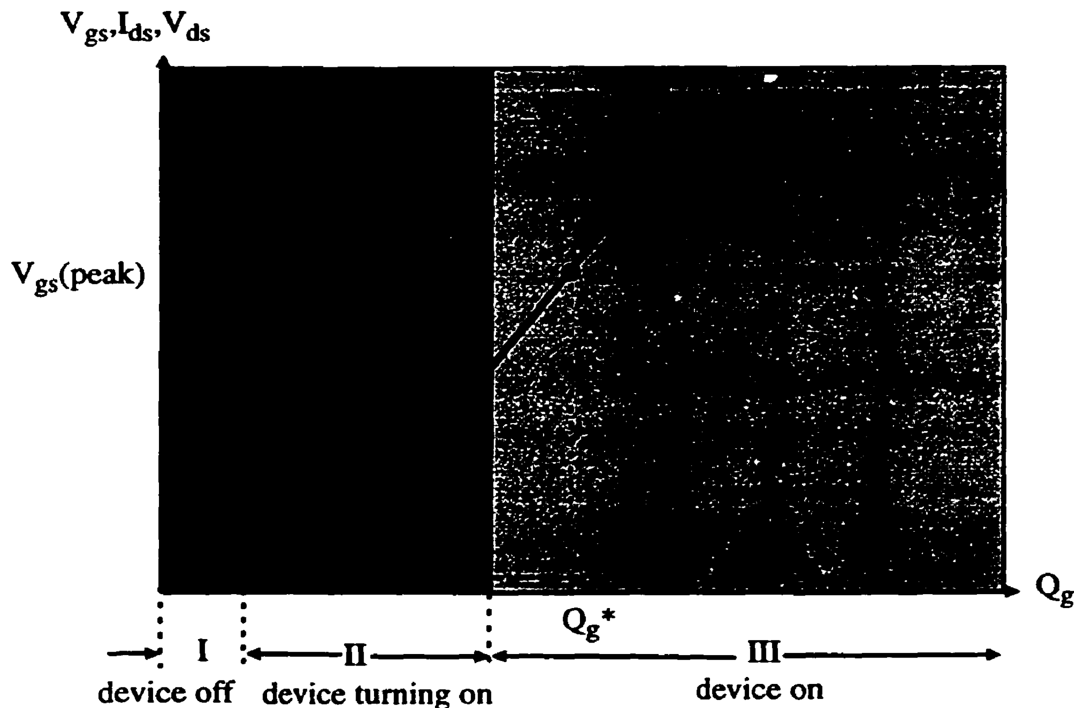

Fig. 1.6: Charge transfer characteristics

There are three distinct regions of importance in this plot. In region I, the device is off, the gate voltage V_{gs} is determined by the voltage across the input capacitance $C_{iss}=C_{gs}+C_{gd}$. The voltage increases linearly in this region until the device starts to turn on.

In region II, the gate voltage turns on the device, the drain current increases, the drain voltage drops and the gate voltage increases slowly as a function of input charge as long as V_{ds} is dropping and I_{ds} is increasing. The input capacitance C_{iss} is now given by the equation

$$C_{iss} = C_{gs} + (1+|A_v|)C_{gd} \tag{1.3}$$

In region III, V_{ds} reaches $V_{ds\text{-}on}$ and the current settles to its final value. The input capacitance C_{iss} is approximately C_{gs} + C_{gd}. The input gate charge Q_g* (at point A) corresponding to V_{gs}(peak) can be determined from that graph.

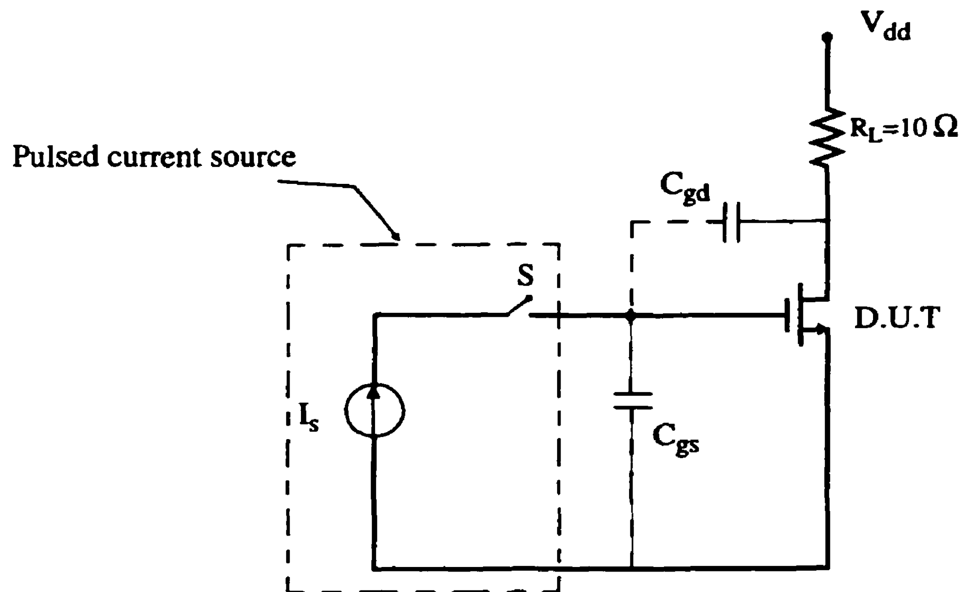

Fig. 1.7: Test circuit for charge transfer characteristics

1.5 Thesis Objective and Organization

Previous publications[11,12] have dealt with the design of high load current (8-13A) power switches for the implementation of voltage regulator modules (VRM) intended for microprocessor applications. It was shown that the lower the FOM the higher the efficiency of the converter[11]. Extrapolation of the reported results suggests that a converter efficiency of 95% can be achieved using a device with FOM less than 10 mΩnC. To the best of our knowledge, there are no published reports that deal with the implementation of CMOS compatible power switches for the 1 A current range category and the majority of state of the art converters are still being implemented using discrete components.

This thesis deals with the design and implementation of a 1 A - low voltage power MOSFET switch using submicron CMOS compatible processes, the target application is high efficiency on-chip switch mode DC/DC converters for portable applications that utilizes dynamic voltage scaling (voltage scheduler algorithms) such as Personal Digital Assistants (PDA's) and digital cameras where load currents are in the range of 0.5 to 1A.

The major specifications of the switch are

- Threshold voltage < 0.6 V
- Breakdown voltage ≥ 5 V
- Current carrying capability ≥ 1 A
- Figure of Merit (FOM) requirement: $R_{on} \times Q_g < 10$ mΩnC
- Switching frequency ≥ 10 MHz.

In this thesis two devices are investigated. In Chapter 2 processing steps, technology issues and optimization of a 0.8 µm single level metallization, N-channel MOSFET are discussed. The design uses 0.8 µm base line and single level metallization which are achievable at the Microelectronics Research Laboratory (MRL). In Chapter 3 the design, implementation and characterization of an optimized switch using a commercial 0.25 µm - 5 level metallization CMOS process are presented. Finally, conclusions along with suggestions for future work are presented in Chapter 4.

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CHAPTER 2

1-A Power MOSFET in 0.8 μm CMOS Technology

2.1 Introduction

In this chapter, an N-channel power MOSFET switch capable of carrying 1 A of current in the on-state is presented. The device is based on a low-voltage lateral CMOS technology with minimum line width of 0.8 μm and a single level metallization dictated by the processing capabilities in the Microelectronics Research Laboratory at the University of Toronto.

Two-dimensional process simulations were performed using TSUPREM-4 to optimize the device structure and doping profiles. This was followed by two-dimensional device simulations using MEDICI. MEDICI's Circuit Analysis Advanced Application Module (CA-AAM) was used to obtain the charge transfer characteristics of the power switch from which the total gate charge value Q_g was extracted.

2.2 1-A Power Switch in 0.8 μm CMOS Process

On-chip implementation of switch mode DC/DC converter implies that the power MOSFET switch, the reactive components and the control circuits must all be implemented on the same silicon chip. The implementation process must be fully CMOS compatible. Furthermore, the power switch must meet the specifications and performance requirements for high-efficiency switch mode converters, particularly a low $R_{on} \times Q_g$.

A cross section of the proposed 0.8 μm N-channel MOSFET unit cell is shown in Fig. 2.1. The 0.8 μm feature size mentioned above defines the minimum drawn gate length. The low doped drain region LDD is required in small channel devices because it enhances

the device immunity to: (1) hot carrier injection which can limit the lifetime of MOSFET devices and (2) parasitic bipolar action.

The process incorporates self-aligned silicide (salicide process) using titanium to reduce the source/drain contact resistance contribution to the switch on-resistance and to enhance the switching speed. The salicide process is very attractive because no extra mask is needed. The gate side wall spacer oxide (SWS) is formed by anisotoropic reactive ion etching (RIE) which: (1) allows the formation of low doped drain junction (LDD) by selectively masking the subsequent heavy arsenic ion-implantation (n+ implant) and (2) prevents bridging between the gate and the source/drain electrodes during the salicide process.

The process features a thin gate oxide (100 Å) to boost current drive and alleviate short channel effects. The lower limit of the oxide thickness is set by fabrication reproducibility. Shallow source/drain junctions are used in the process to minimize short channel effects. The process specifications of the 0.8 μm MOSFET unit cell illustrated in Fig. 2.1 are summarized in Table 2.1.

Table 2.1: Process specifications of the 0.8 μm unit cell

Parameter/Units	Symbol	Value
Threshold Voltage (V)	V_{th}	0.32
Subthreshold Swing (mV/decade)	S	80.34
Gate Oxide Thickness (Å)	t_{ox}	100
P-well Depth (μm)	$X_{j\text{-}p\text{-}well}$	1.5
P-well Surface Concentration (cm^{-3})	$N_{p\text{-}well}$	8×10^{16}
Poly Gate Thickness (μm)	t_{poly}	0.45
Polycide Sheet Resistance (Ω/□)	R_{poly}	<10
Source/Drain Junction Depth (μm)	X_j	0.22
S/D Sheet Resistance (Ω/□)	R_{sd}	<10
S/D Breakdown Voltage (V)	BV_{DS}	9

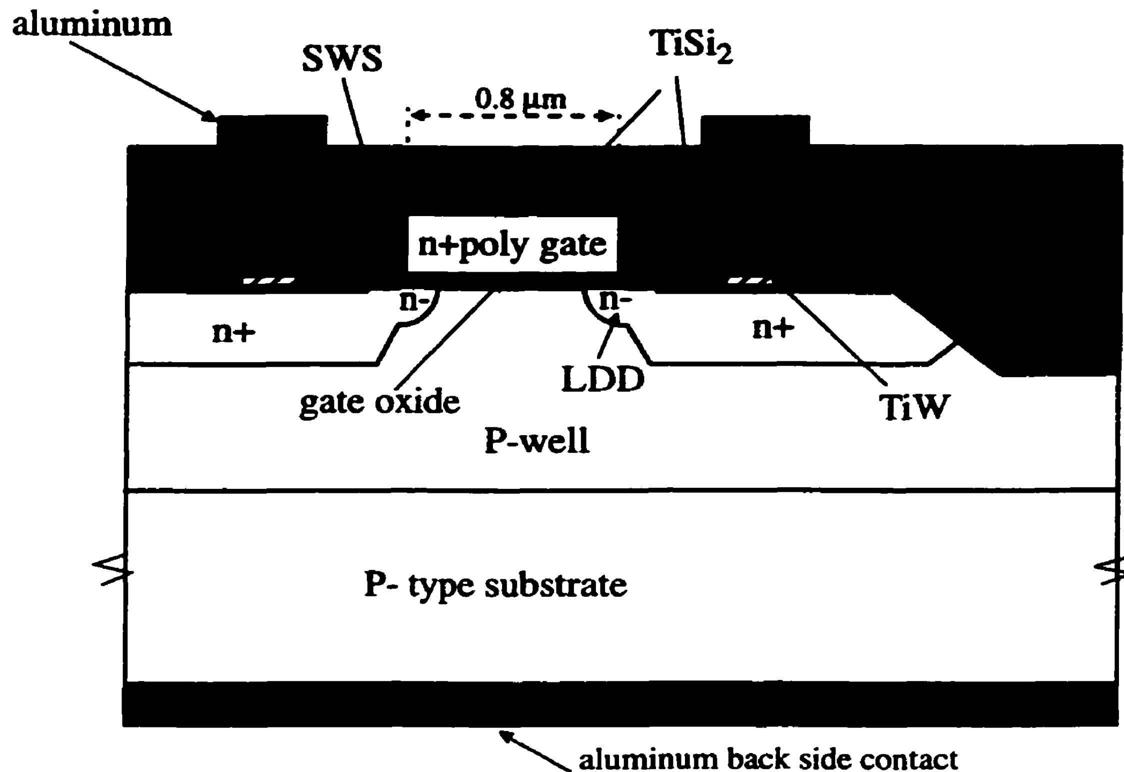


Fig. 2.1: Cross section of the 0.8 μm N-channel lateral MOSFET

2.3 Design Criteria for Low-Voltage Power Switch

2.3.1 Specific On-Resistance

The power losses in the switch during conduction is proportional to the on-resistance. The on-resistance is determined by the total resistance between the source and drain contacts. Although the on-resistance can be reduced by paralleling many individual unit cells using specific layout techniques such as interdigitated or checkerboard patterns, chip area and junction capacitances accordingly increase. Therefore, specific on-resistance $R_{on\text{-}sp}$, which is the product of the on-resistance and the device area, is more commonly used as a measure of performance to compare different switches.

For a LDD N-channel MOSFET, the total specific on-resistance consists of four components, as illustrated in Fig. 2.2 and is given by

$$R_{on-sp} = R_{ch-sp} + 2R_{ldd-sp} + 2R_{sd-sp} + 2R_c \quad (2\text{-}1)$$

where $R_{ch\text{-}sp}$ is the specific resistance of the channel, $R_{ldd\text{-}sp}$ is specific resistance of the LDD regions, $R_{sd\text{-}sp}$ is the specific resistance of the S/D junctions and R_c is the S/D specific contact resistance.

The specific channel resistance can be expressed as

$$R_{ch-sp} = WL\frac{L}{W\mu_{ns}C_{ox}(V_{GS}-V_{th})} = \frac{L^2}{\mu_{ns}C_{ox}(V_{GS}-V_{th})} \quad (2\text{-}2)$$

where W is the channel width, L is the channel length, μ_{ns} is the mobility of electrons in the channel, V_{th} is the threshold voltage, V_{GS} is the gate voltage and C_{ox} is the gate oxide capacitance per unit area and is given by

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (2\text{-}3)$$

where ε_{ox} is the oxide permittivity and t_{ox} is the gate oxide thickness.

The channel specific resistance is the largest among the resistive components and as indicated in Equation 2-2 is dependent on the channel mobility, the channel length, threshold voltage and oxide thickness t_{ox}. The specific resistance $R_{ldd\text{-}sp}$ is associated with the LDD regions and is given by

$$R_{ldd-sp} = WL_{ldd}\frac{L_{ldd}}{W\mu_{na}C_{ox}(V_{GS}-V_{th-ldd})} = \frac{L_{ldd}^{2}}{\mu_{na}C_{ox}(V_{GS}-V_{th-ldd})} \quad (2\text{-}4)$$

where L_{ldd} is the effective length of the LDD region, μ_{na} and $V_{th\text{-}ldd}$ are the electron mobility and the threshold voltage in the LDD region, respectively. The specific source/drain resistance $R_{sd\text{-}sp}$ is due to the n+ junctions and is dependent on the junction depth and the doping concentration.The last term in Equation(2-1) is the specific contact resistance which is directly proportional to the contact resistivity. A reduction in the contact

specific resistance can be achieved by using self-aligned selicide in the source/drain junctions.

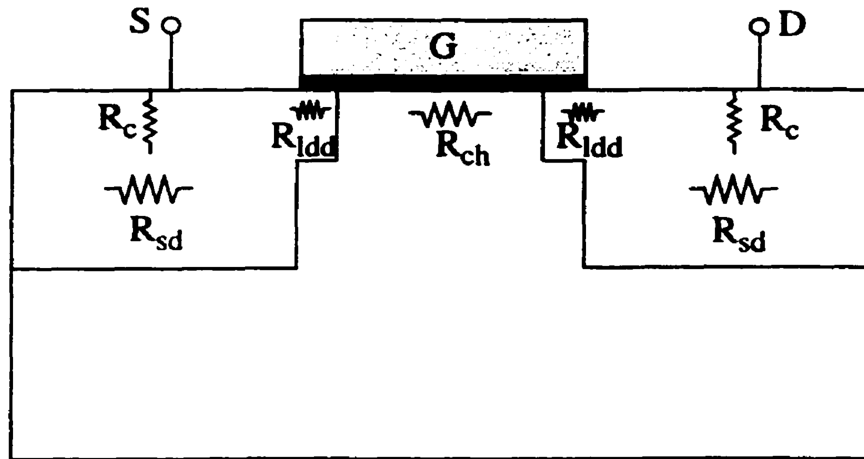


Fig. 2.2: Cross section of the LDD MOSFET structure indicating different components of the on-resistance

2.3.2 Input Capacitance C_{iss}

As discussed in Chapter 1, the switching plus gate drive losses are proportional to the switching times t_r, t_f and the total gate charge Q_g. The switching time is proportional to the carrier transit time across the channel and the rate of charging and discharging of the input capacitance C_{iss} associated with the gate of the MOSFET structure. The carrier transit time is inversely proportional to the channel length L. Thus, a short channel length is preferable for high speed. The different capacitive components associated with the MOSFET structure are illustrated in Fig. 2.3. The input gate capacitance C_{iss} has two components, C_{gs} and C_{gd} (Miller feedback capacitance). The gate to source capacitance C_{gs} is due to overlap capacitance between the gate electrode and the source junction $C_{gs\text{-}ov}$ and the gate to bulk capacitance C_{gb}. The gate to bulk capacitance C_{gb} in turn is the series combination of the oxide capacitance C_{ox} and the space-charge capacitance. The maximum value of C_{gb} is equal to C_{ox} which occurs under accumulation conditions. The gate to drain capacitance is

determined by the overlap length between the gate electrode and drain junctions L_{ov} and the gate oxide thickness.

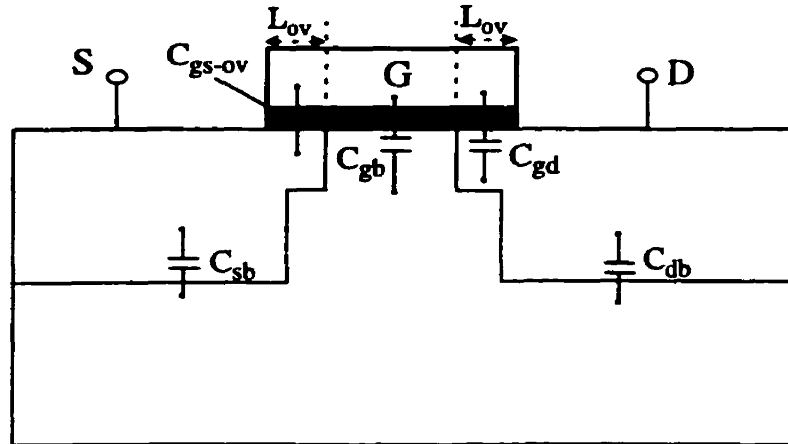


Fig. 2.3: Cross section of the LDD MOSFET indicating various capacitance components in the structure

For accurate estimation of the input capacitance, the fringing capacitances may also be added to C_{gs} and C_{gd}.

Due to the "distributed RC network" nature of the channel of MOSFETs and their voltage dependence, the exact modeling of the MOSFET during switching is not a straightforward practice[1], however, by examining the device parameters contributing to C_{iss}, a design criteria for minimizing the input capacitance can be established. The design criteria are: small gate to source and gate to drain overlap lengths, reduced channel area (W.L), hence, the requirement for shorter channel length and higher current drive.

2.3.3 Short Channel Effects

Scaling of MOSFETs is not free from performance and reliability degradations. Issues such as threshold voltage roll-off (which sets the lower limit for MOSFET physical gate length)[2], hot carrier injection and parasitic BJT action are known to be the most serious problems associated with short channel devices. For no short channel effects the minimum

channel length of a MOSFET for a certain technology can be calculated using the following empirical relationship[3]

$$L_{min} = 0.4[r_j t_{ox}(W_S + W_D)^2]^{1/3} \quad (2\text{-}5)$$

where r_j is the junction depth in μm, t_{ox} is the oxide thickness in Å and W_S and W_D are the depletion region widths in μm at the source and drain junctions, respectively. Generally, as long as the channel length is larger than L_{min} the device maintains long channel behaviour. It can be concluded , from Equation 2-5, that to promote long channel behaviour, the junction depth and oxide thickness must be reduced and the background concentration must be increased.

2.3.4 Subthreshold Current

The fundamental theory of the MOSFET assumes that no drain current exists when the gate to source voltage is lower than the device threshold voltage. In real devices, however, there is a weak current conduction known as the subthreshold leakage current. In battery-powered portable applications, this leakage current can significantly reduce the battery lifetime. The lower the threshold voltage the higher the off-state current (at V_{GS}=0) as demonstrated in Fig. 2.4 (I_{Ls}< I_{Ls}').

The subthreshold current is related to the threshold voltage through the equation

$$I_{Ls} = I_o \frac{W}{L} e^{\frac{qn(V_{GS} - V_{th})}{KT}} \left(1 - e^{\frac{-qV_{DS}}{KT}}\right) \quad (2\text{-}6)$$

where I_o is the characteristic current and n is given by

$$n = \left(1 + \frac{C_{dep}}{C_{ox}}\right)^{-1} \quad (2\text{-}7)$$

in which C_{ox} and C_{dep} are the oxide and depletion capacitances per unit area, respectively

The off-state leakage current can be obtained from the equation

$$I_{off} = A \cdot 10^{\frac{-V_{th}}{S}} \qquad (2\text{-}8)$$

It can be seen, form Equation 2-8, that a low I_{off} requires higher threshold voltage and lower subthreshold swing S. To reduce S, the channel doping and oxide thickness must be lowered.

The subthreshold swing S is used to characterize the subthreshold behavior of MOSFETs and is defined as the inverse of the rate of a decade decrease in current with V_{GS} reduction and is given by

$$S = \frac{\partial V_{GS}}{\partial \log I_{SL}} = 2.3\frac{KT}{q}\left(1 + \frac{C_{dep}}{C_{ox}}\right) \qquad (2\text{-}9)$$

It is desirable to have a low value of S. The lower theoretical limit of S is equal to 59.8 mV/decade (2.3 KT/q) at T=300°K.

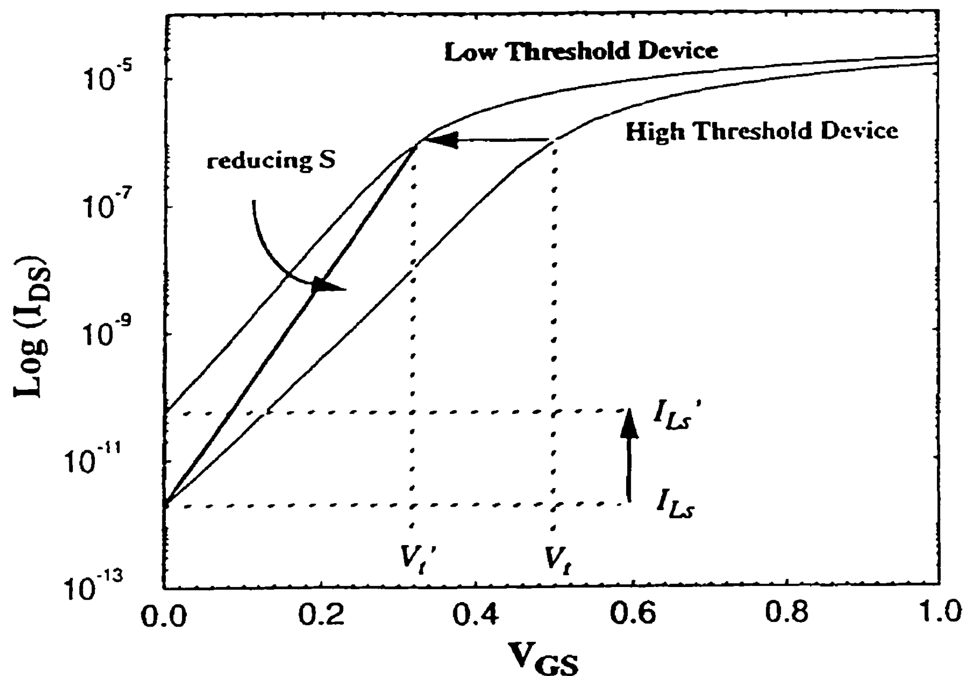


Fig. 2.4: Effect of V_t scaling on subthreshold leakage current[4]

2.3.5 Hot Carrier Injection & Parasitic Bipolar Action

Another important phenomenon associated with short channel MOSFETs is the hot carrier injection (HCI). This phenomenon occurs when channel carriers entering the high electric field region near the drain end of the channel gain sufficient energy to overcome the $Si\text{-}SiO_2$ surface barrier and are injected into the oxide. These carriers can cause damage to the $Si\text{-}SiO_2$ interface and result in trapped charge in the oxide. As a consequence, shifts in the transistor threshold voltage, transconductance and drain saturation current can take place.

Associated with HCI is another mechanism known as parasitic bipolar action illustrated in Fig. 2.5. When the electric field near the drain end of the channel exceeds 100 KV/cm, channel carriers gain enough energy, to cause impact ionization resulting in electron-hole (e-h) pair generation[5]. The electrons drift to the drain while holes are swept to the bulk, creating a substrate current I_{sub} which gives rise to a potential difference between the substrate back contact and the bulk. This voltage drop results in forward biasing of the source to bulk diode which in turn results in more carrier injection in the channel.

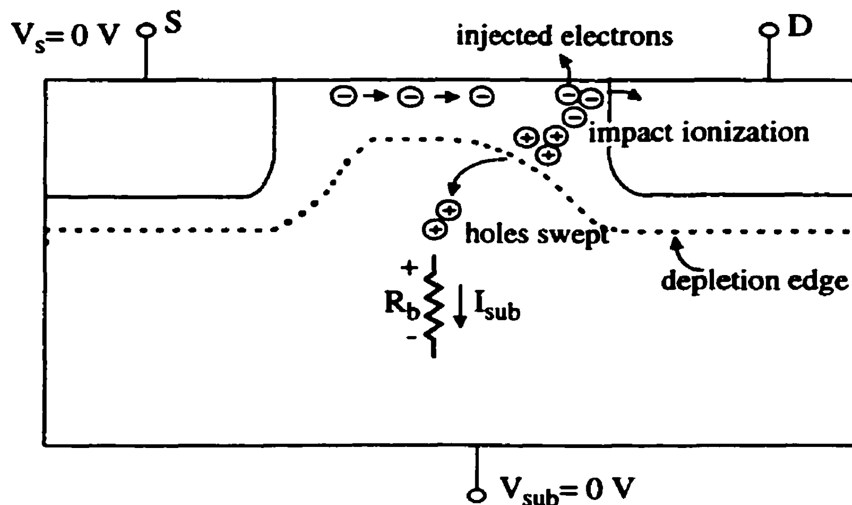


Fig. 2.5: Parasitic bipolar action in short channel MOSFETs

The injected channel carriers are accelerated towards the drain causing more e-h pair generations via impact ionization through regenerative feedback resulting in an increase in the drain current which if excessive can result in device failure. The mechanism resembles the operation of a bipolar transistor where the source acts as the emitter, the substrate as the base and the drain as the collector.

To alleviate HCI effects and parasitic BJT action, low doped drain junctions are inserted between the heavily doped drain and the channel. These LDD regions relax the lateral electric field distribution and spread it laterally, thus, lowering the maximum electric field[6-7]. The penalty in using LDD regions is the increase in the on-resistance, however, this penalty is imposed by the necessity to design a reliable device that can perform well over time.

2.4 Process Description

The process involved in the fabrication of the unit cell is described with reference to Fig. 2.6. Starting with a 18-20 Ω–cm, p-type wafers with <100> orientation, a p-well implant is carried out through a thermally grown 300Å screen oxide as shown in Fig. 2.6(a). The dopant impurities are then driven-in at 1000 °C for 150 minutes in nitrogen ambient.

Low pressure chemical vapor deposition (LPCVD) of silicon nitride film (1200Å) is performed and photolithography using mask #1 (active) is used to define the active regions as shown in Fig. 2.6(b). Local oxide (LOCOS) is grown at 950°C for approximately four hours in wet O_2 resulting in 7000Å of oxide everywhere except for the area protected by the silicon nitride (active region).

The nitride and the pad oxide are removed and a thin layer of sacrificial oxide (400Å) is thermally grown at 950°C to remove any silicon nitride (white ribbon) formed on the silicon surface due to the chemical reaction between NH_3 and the silicon surface during the lengthy LOCOS growth.

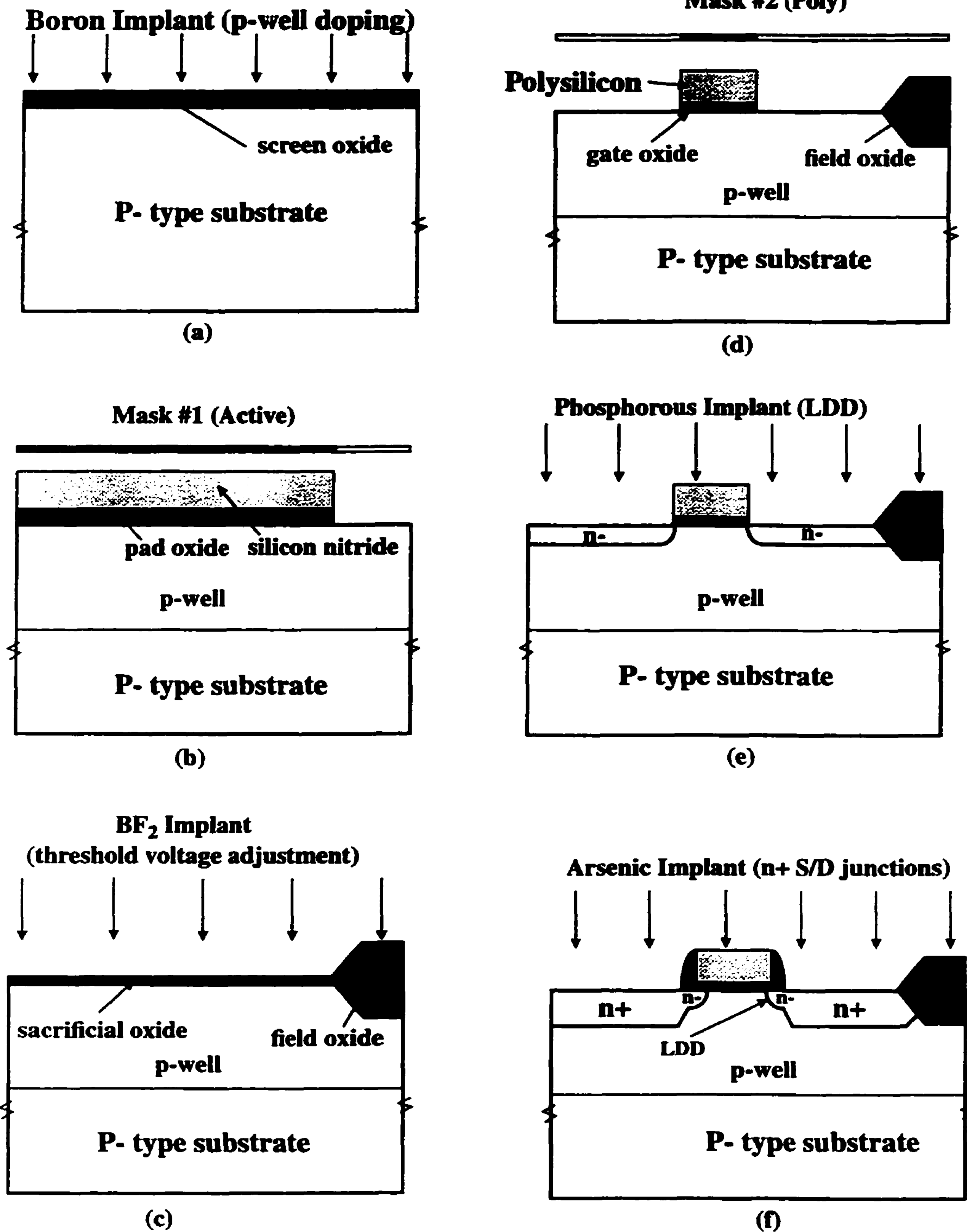
A threshold voltage adjustment implant using BF_2 with a dose of $8\times10^{13}cm^{-2}$ and energy of 25 keV is performed to raise the channel surface concentration, as shown in Fig. 2.6(c). BF_2 has low projected range making it more suitable for this specific process, compared to boron. The sacrificial oxide is then etched and the gate oxide is grown in dry oxygen (1100 °C, 6.5 minutes). The process incorporates 2% HCl to eliminate mobile charges (mainly positive alkali metal ions) in the gate oxide. The process is followed by a 30 minutes anneal in a N_2 ambient to reduce the fixed oxide charge and the interface trapped charge.

In-situ doped polysilicon with a thickness of 4500Å is then deposited by LPCVD. Wet etching of the polysilicon and the underlying oxide from the back side of the wafer is performed. The polysilicon is defined using mask #2 (poly) and etched by reactive ion etching (RIE) using clorine as shown in Fig. 2.6(d).

During RIE etching of the gate, some damage occurs to the gate oxide underneath the polysilicon and to the substrate[8]. Therefore, it is necessary to follow the RIE process by rapid thermal annealing (RTA) at 900°C for 1.5 minutes in an oxygen ambient. Thereafter, the LDD implant is performed using phosphorous (2.5×10^{13} cm^{-2}, 40 keV), as shown in Fig. 2.6(e). Next, fabrication of the side wall spacer (SWS) is carried out a 4500Å LPCVD oxide followed by oxide densification at 900°C for 40 minutes in a N_2 ambient[1] and finally directional RIE etching of the oxides is performed to define the side wall spacer.

The source/drain junctions are fabricated, by arsenic ion-implantation with a dose of 4.7×10^{15} cm^{-2} and energy of 70 keV through a 200Å deposited oxide. The implantation is self-aligned to the edge of the SWS rather than to the polysilicon causing the highly doped n+ junction to be positioned away from the channel end as shown in Fig. 2.6(f).

1. This annealing process drives-in phosphorous impurities under the gate.


Boron Implant (p-well doping)
screen oxide
P- type substrate
(a)
Mask #1 (Active)
pad oxide
silicon nitride
p-well
P- type substrate
(b)
BF2 Implant
(threshold voltage adjustment)
sacrificial oxide
field oxide
p-well
P- type substrate
(c)
Mask #2 (Poly)
Polysilicon
gate oxide
field oxide
p-well
P- type substrate
(d)
Phosphorous Implant (LDD)
n-
n-
p-well
P- type substrate
(e)
Arsenic Implant (n+ S/D junctions)
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p-well
P- type substrate
(f)

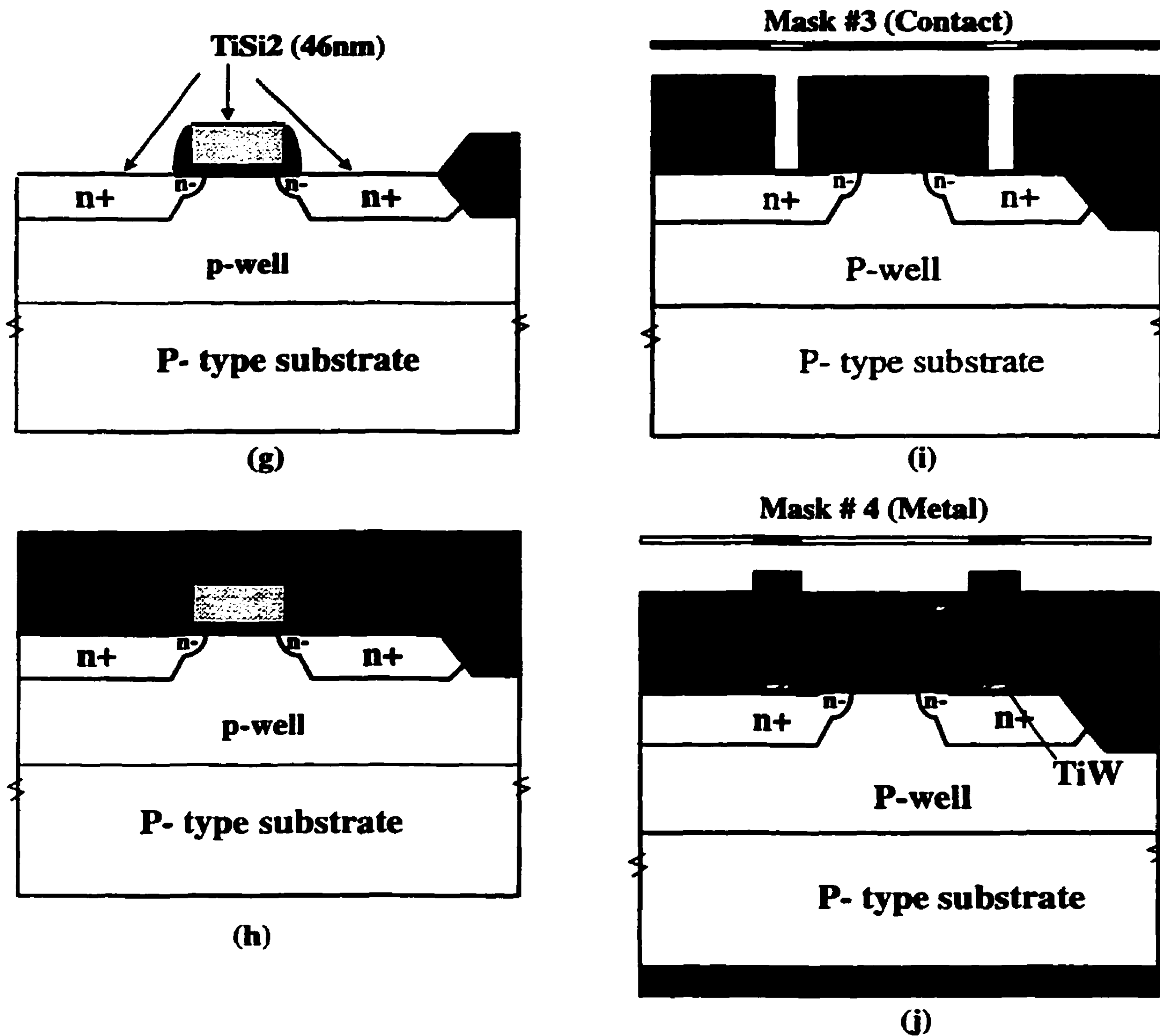

Fig. 2.6: 0.8 μm N-channel process flow

Thereafter, an 800Å oxide film is deposited using LPCVD and arsenic activation is carried out by RTA for 40 seconds at 1050 °C in N_2 ambient. The purpose of the oxide deposition is to prevent auto-doping during the RTA process.

Self-aligned titanium silicide (salicide) steps are carried out [9-10]. First the oxide is wet- etched from the top of the gate, source and drain areas. A thin film of titanium (50 nm) is blanket-sputtered on the surface, followed by a short RTA process (650 °C, 1 minute) in N_2 ambient. It is necessary to control carefully the temperature and time during this process to prevent lateral bridging between the gate electrode and the S/D junctions. The nitrogen helps to limit "silicon pumping" and to confine the chemical reaction to regions where titanium and silicon are effectively in physical contact.

Next, selective wet etching of the unreacted titanium is performed using H_2O_2: NH_4OH. The result at this stage is the high-resistance metastable phase of $TiSi_2$. Transformation to the low-resistance phase is done by a second RTA step at 850°C for 30 seconds. The cross-section of the structure after Salicide formation is shown in Fig. 2.6(g). A 3000 Å oxide layer is deposited, and the oxide is densified by RTA at 800°C for 2 minutes. Photolithography is performed using mask #3 (contact) to define the contact area and contact opening is carried out using RIE as shown in Fig. 2.6(i).

A blanket layer of titanium tungsten alloy (1000 Å) is sputtered and followed by sputtering of 1 μm layer of aluminum. The titanium tungsten is used to prevent aluminum spiking through the junctions.

Photoresist is patterned using mask #4 (metal). Aluminum is wet etched and the photoresist is removed. TiW is then selectively wet etched using H_2O_2 with the aluminum acting as a mask.

Annealing in forming gas is performed for 25 minutes at 450°C to reduce the contact resistance and the interface trapped charge. The cross-section of the device at the end of the process is shown in Fig. 2.6(j). The process flow used in the fabrication of the 0.8 μm process is summarized in Table 2.2.

Table 2.2: 0.8 μm process summary

Step	Process
Starting material	4" <100> p-type wafers, resisitivity=18 to 20Ω-cm
Screen gate oxide	1000°C, 28 min., dry O2, Thickness=300Å
P- well implant	Ion-implantation, boron, Dose=$4x10^{12}$ cm^{-2}, Energy=20keV.
Well dopant drive-in	1000°C, 150 min., nitrogen ambient
Screen oxide etch	Wet etching in 10% buffered HF
Pad oxide growth	1000°C, 28 min., dry O2, Thickness=300Å
Depositing of silicon nitride	LPCVD of nitride, thickness=1200Å
Patterning the nitride	Photolithography using mask #1, RIE of nitride and wet etching of the oxide
LOCOS growth	950°C, dry O2, 5 min. 950°C, wet O2, 240 min. 950°C, dry O2, 5 min. 950°C, nitrogen, 20 min., thickness=7000Å
Nitride and pad oxide removal	Oxide wet etching, 1 min. Nitride wet etching, 14:20 min. Oxide wet etching, 45 seconds
Sacrificial oxide growth	950°C, dry O2, 80 min., thickness=400Å, oxide wet etching
Gate oxide growth	1100°C, O2=8%, HCl=2%, N2=90%, 6.5 min, thickness=100Å 1100°C, N2, 30 min.(annealing)
Deposition of polysilicon gate	LPCVD of in-situ doped polysilicon, thickness=4500Å
Wet etching of the polysilicon and oxide layer from the back of the wafer	PR application on the surface of the wafer, wet etching of the polysilicon and oxide layers from the back
Deposition of oxide	LPCVD of oxide, thickenss=2500Å

Table 2.2: 0.8 μm process summary

Step	Process
Defining the gate structure	Photolithography (mask #2), RIE of oxide, and polysilicon layers
RTA annealing	900°C, 2 min., O2 ambient
Formation of LDD S/D junctions	Ion-implantation, phosphorous, Dose=2.5×10^{13} cm^{-2}, Energy=40keV.
Deposition of oxide	LPCVD of oxide, thickenss=4500Å
Densification of oxide and phosphorous dopant drive-in	900°C, 40 min., N2
SWS formation	Directional RIE of oxide
Deposition of screen oxide	LPCVD of oxide, thickenss=200Å
Formation of n+ S/D junction	Ion-implantation, arsenic, Dose=4.7×10^{15} cm^{-2}, Energy=70keV.
Deposition of oxide (auto-doping prevention)	LPCVD of oxide, thickenss=800Å
Arsenic activation	RTA: 1050°C, time=40 seconds, N2
Oxide etching (gate, S/D)	Directional RIE of oxide
Self-aligned silicide formation	Titanium sputtering, thickness=500Å, First RTA, 650°C, 1 min., N2, Wet etching of unreacted titanium: H2O2, NH4OH, -Second RTA, 850°C, for 30 seconds
Deposition of oxide	LPCVD of oxide, thickenss=3000Å
Densification of oxide	RTA, 800°C, 2 min.
Formation of contact windows to gate, S/D	Photolithography (mask #3)
Contact opening	RIE of oxide
Titanium tungsten application	Sputtering of TiW, thickness=1000Å
Metallization	Sputtering of Al layer, thickness=1μm
Metal patterning	Photolithography (mask#4) Aluminum and TiW wet etching(H2O2)
Aluminum sintering	450°C, 25 min. forming gas

2.5 Layout of 1 A Power Switch

The 1-A power MOSFET switch is constructed by connecting individual unit cells in parallel using specific layout techniques. The layout pattern used here is of a checkerboard type as illustrated in Fig. 2.7, each source/drain junction is shared by four surrounding transistors, thus maximizing the effective channel width per area ratio W/A.

The 1-A power switch was realized using a pattern consisting of an array of alternating source and drain junctions, self-aligned to a mesh of polysilicon-gate structure. The width of the polysilicon line is 0.8 μm.

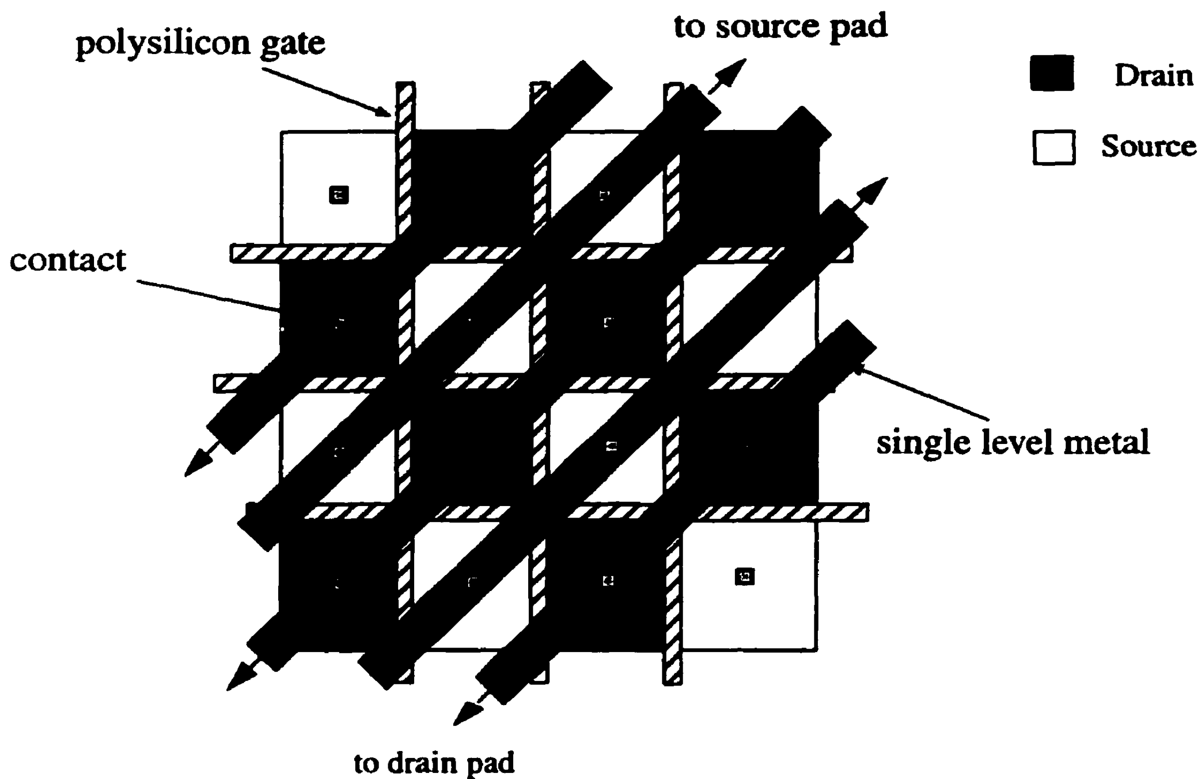

Fig. 2.7: Checkerboard layout pattern using single level metallization

Alternating source/drain metal runners are composed of one level of metal (aluminum) which run diagonally over the source/drain junctions to contact the pads via wide metal buses. Both the contact and the metal runners are oriented at 45° in order to achieve minimum cell pitch. The metal runner width is kept as narrow as possible to achieve minimum cell pitch but wide enough to avoid electromigration failure due to high current densities, this is especially true in the long metal runners at the centre of the structure.

2.6 Process Simulations

The process flow discussed in section 2.4 was arrived at by iterative simulations using TSUPREM-3 and TSUPREM-4[11] which were used to adjust the doping profiles of the p-well, channel, S/D junctions and LDD regions.

Since simulation of a 2-D structure defined with a fine mesh is very time consuming, 1-D simulations using TSUPREM-3 were initially used to arrive at the doping profiles, oxide layers thickness, ion-implantations doses and energies etc. Once the doping profiles and processing parameters are correctly obtained using 1-D simulations, 2-D simulations using TSUPREM-4 were carried out to account for 2-D effects such as lateral diffusion and to fine tune the final processing parameters. Further, doping profiles, device structure and mesh generated by 2-D simulations can be directly transferred to a device simulator such as MEDICI.

2.6.1 2-D Process Simulations Using TSUPREM-4[11]

The simulated structure is essentially the unit cell of the power MOSFET switch, which is the main building block of the switch. The top view along with a cross section of the unit cell are shown in Fig. 2.8. Aggressive layout design rules were developed in order to achieve the minimum cell pitch possible.

The minimum cell pitch for a given technology is determined by the minimum line width that can be resolved by this technology. In the MRL facilities this line width is 0.8 μm, the complete design rules used in the layout is given in Appendix A.

The simulated structure has a cell pitch of 4.1 μm. The process utilizes two levels of interconnects, a polysilicon layer and a single level of metallization. The net doping contours in the different regions of the unit cell structure together with the major process components are shown in Fig. 2.9 using TMA Visual[1].

The doping profiles in the channel, source/drain regions and in the LDD are shown in Fig. 2.10. The threshold voltage adjustment using BF_2 results in channel surface concentration of 8×10^{16} cm^{-3} corresponding to a threshold voltage of 0.322 V. The LDD regions has a junction depth of 0.18 μm and a maximum peak concentration of $2.6\times10^{18} cm^{-3}$, its width is determined by the SWS oxide lateral width which is 0.35 μm.

The S/D junction depth and doping profile are controlled by the arsenic ion-implant dose and energy and also by the thickness of the screen oxide. The surface concentration of the source/drain regions is $2.5\times10^{20} cm^{-3}$ with a junction depth of 0.22 μm.

While all ion-implantations are performed through a screen oxide to ensure amorphous scattering of dopants, a 7° tilt angle were used in the simulations since the commercial ion-implantation facilities uses 7° tilt angle as a standard procedure. In addition, temperature ramp-up and ramp-down of all diffusion steps were included in the simulations.

1. TMA Visual is a trademark of Technology Modeling Associates, Inc. (TMA)

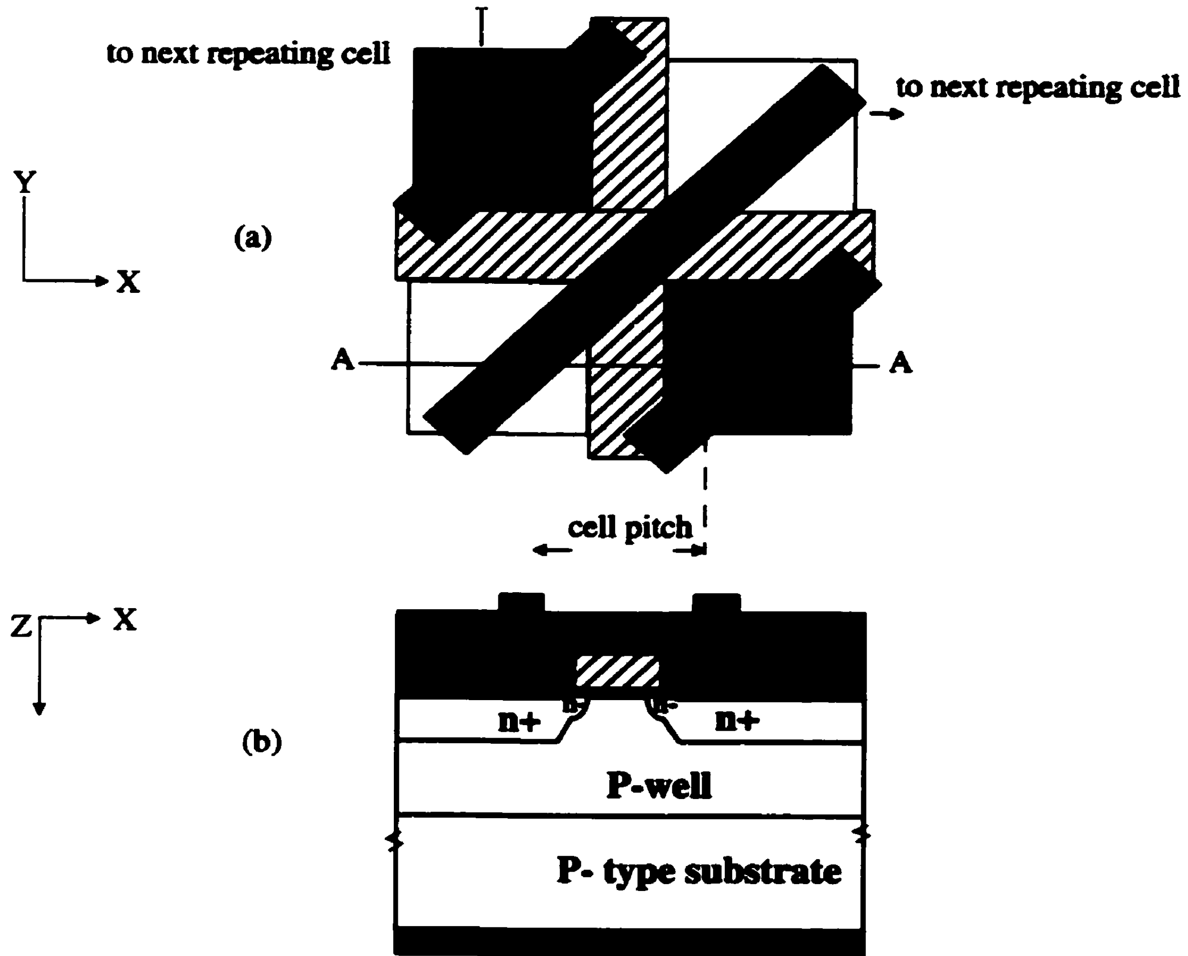

Fig. 2.8: Device structure: (a) top view (b) cross section of the unit cell

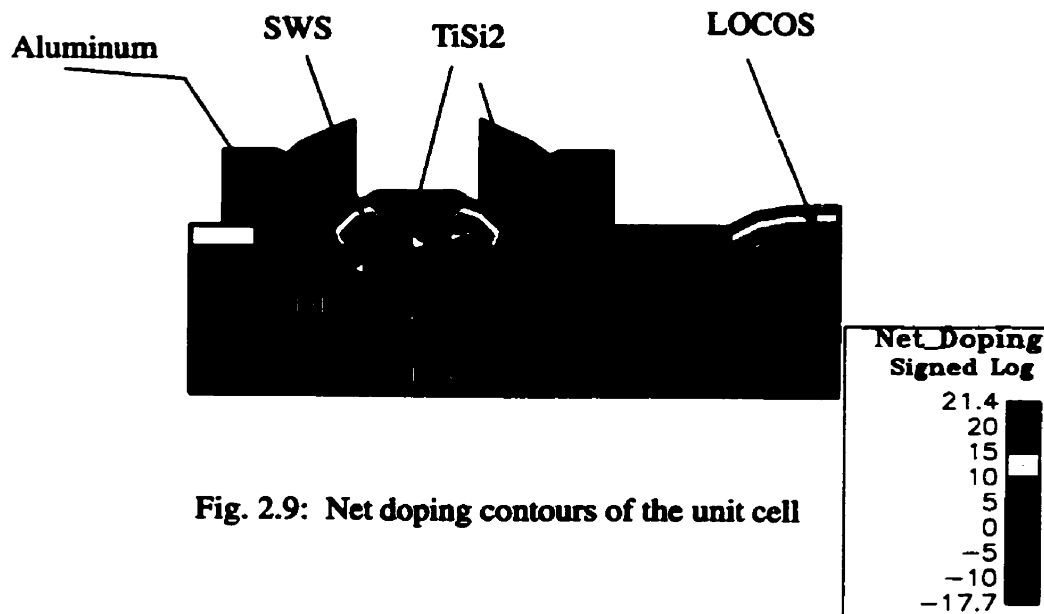

Fig. 2.9: Net doping contours of the unit cell

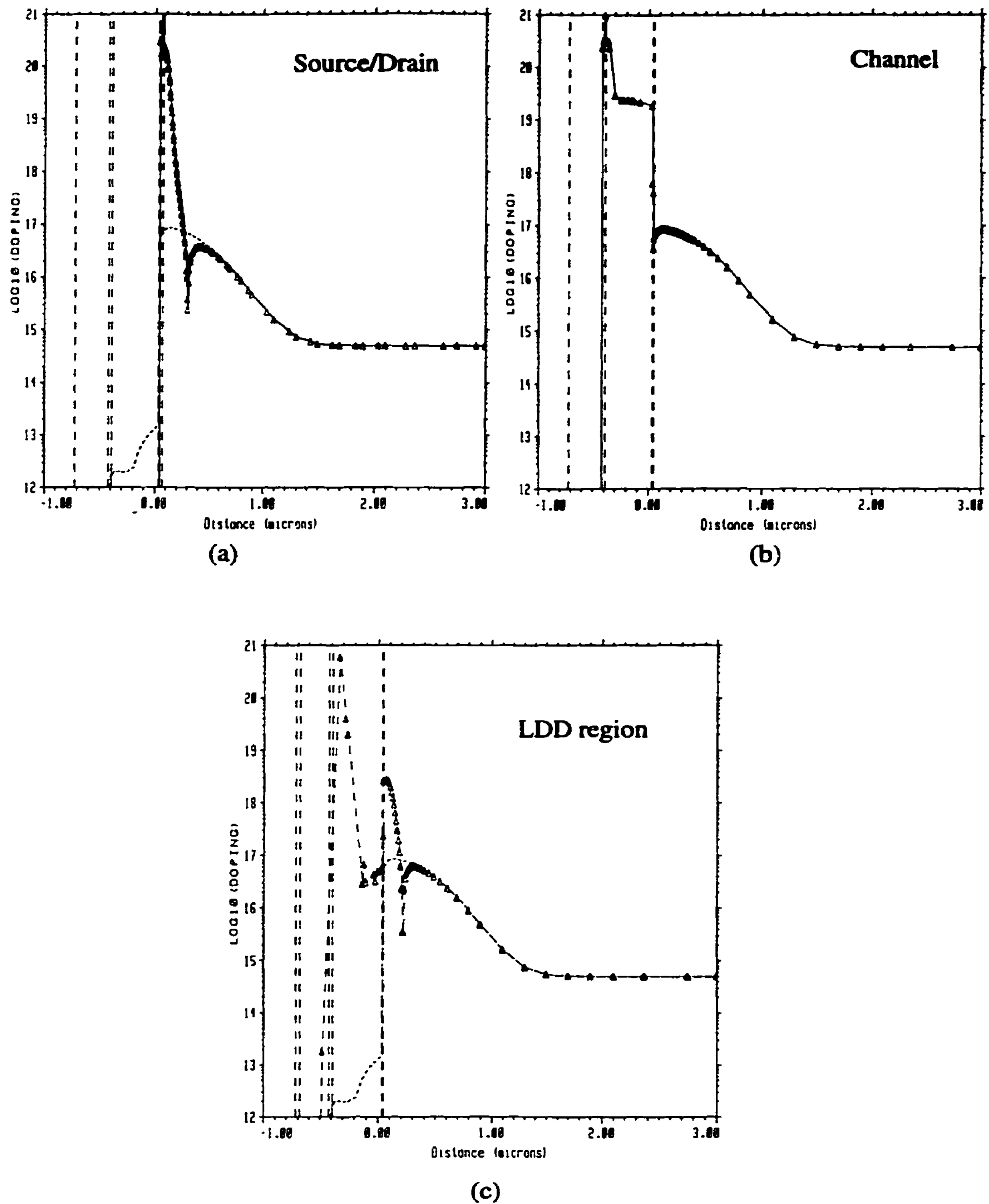

Fig. 2.10: Simulated doping profiles in (a) S/D region, (b) channel region and (c) LDD region

2.7 Device Simulations

Device simulations were carried out using MEDICI[12]. MEDICI simulations were done iteratively in conjunction with TSUPREM-4 to adjust and/or optimize the unit cell electrical characteristics such as threshold voltage, subthreshold swing, breakdown voltage etc. The empirical formula in Equation 2-5 was used to analytically confirm the minimum device length for long channel behavior. The calculated L_{min} is 0.423 μm which suggests that a 0.8 μm device will not suffer short channel effects. The subsequent simulations results are normalized on a per channel width basis (i.e W=1 μm).

2.7.1 I-V Characteristics

The transfer characteristic of the unit cell is obtained by sweeping the gate to source voltage from zero to 5 V in 0.1 V increments at V_{DS}= 0.1 V as shown in Fig. 2.11. The extracted threshold voltage is 0. 337 V and is defined as the intercept of the x-axis with a line extrapolated from the linear region of the I_{DS}-V_{GS} curve.

The value of the subthreshold swing S is extracted from the subthreshold transfer characteristics, as shown in Fig. 2.12, and is equal to 80.34 mV/decade at V_{GS}= 0.17 V. The device leakage current at zero gate voltage and V_{DS}= 0.1 V is 68.7 pA/μm. The unit cell effective channel length is 0.6225 μm.

The output characteristics are simulated by sweeping V_{DS} from 0 to 9 V at different V_{GS} values from zero to 5 V in 1 V increments as shown in Fig. 2.13.

The drain saturation current $I_{D\text{-}sat}$ is 862 μA/μm at V_{GS}= 5 V which indicates high current drive of the unit cell. This result translates into the following: (1) a power MOSFET switch implemented by paralleling this unit cell would require less total width, occupy less chip area which in turn results in lower input capacitance and total gate charge and (2) faster switching speeds for digital circuits implemented on-chip. In addition, the almost flat output

characteristics in the saturation region is very desirable in applications such as current mirrors.

The device specific on-resistance defined as the product of the inverse of the slope of the I_D-V_{DS} curve (normalized per channel width) in the triode region and the cell pitch is 117.46 $\mu\Omega.cm^2$ at V_{GS}=3.3 V.

The 1-A power switch can be realized using a pattern consisting of a 70x70 array of alternating source and drain junctions. The total width of the power switch is 31,878 μm corresponding to a current carrying capability of at least 1.0 A and a device on-resistance R_{on} of 90.1 mΩ at V_{GS}=3.3 V.

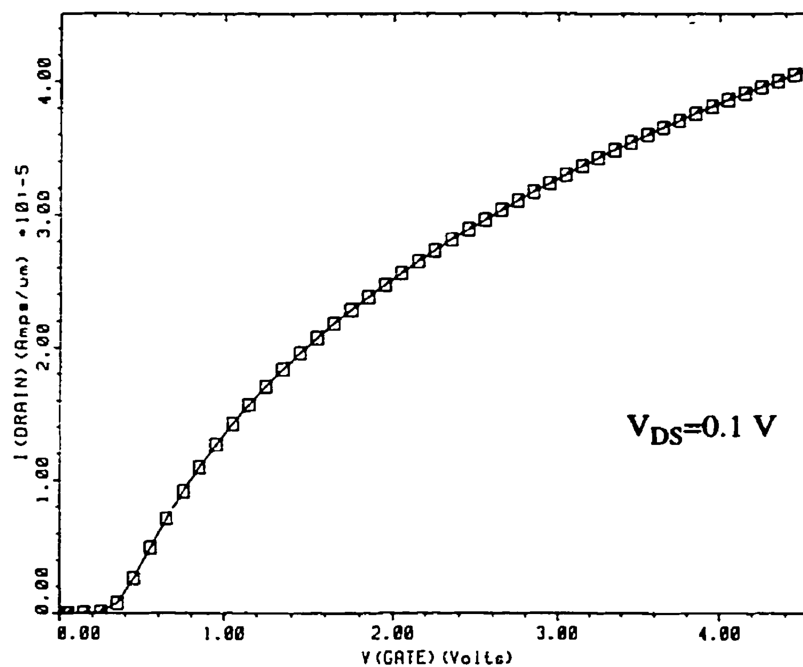

Fig. 2.11: Simulated transfer characteristics of the unit cell (L_{drawn}=0.8 μm, L_{eff}=0.6225 μm)

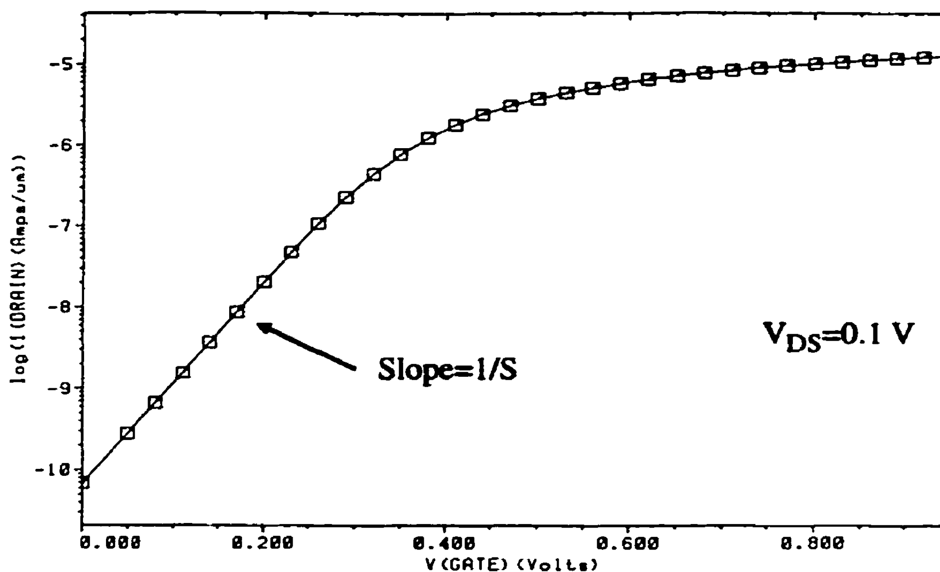

Fig. 2.12: Simulated subthreshold characteristics of the unit cell (L_{drawn}=0.8 μm, L_{eff}=0.6225 μm)

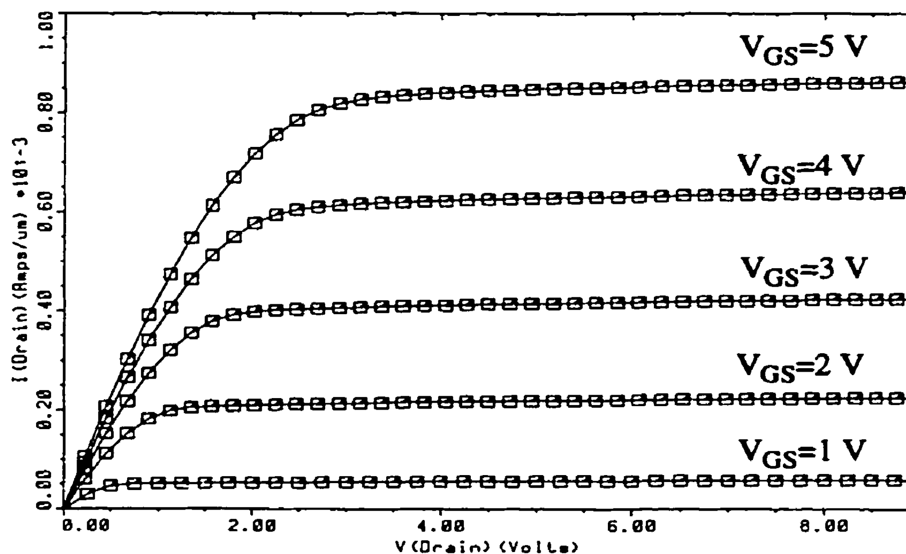

Fig. 2.13: Output characteristics of the unit cell (L_{drawn}=0.8 μm, L_{eff}=0.6225 μm)

2.7.2 Charge Transfer Characteristics & FOM

The charge transfer characteristics was obtained using MEDICI's Circuit Analysis Advanced Application Module (CA-AAM)[12]. The switch was simulated in a common source configuration as shown in Fig. 2.14 with a pulsed voltage source[1] applied to the gate of the switch and with the drain connected to a 10 V supply via 10 Ω load resistor. The simulated charge transfer characteristics is shown in Fig. 2.15. The total gate charge Q^*_g necessary to charge the input capacitance C_{iss} and raise its voltage to 3.3 V is 0.34 nC as illustrated in Fig. 2.15. The switch FOM defined as the product of the on-resistance and the total gate charge at V_{GS}= 3.3 V yields a value of 30.6 mΩnC. A summary of the key parameters of the power switch are listed in Table 2.3

Table 2.3: 0.8 μm power switch key parameters

Parameter/Units	0.8 μm/100 Å
Operating Voltage (V)	3.3
Forward blocking capability (V)	9
Current handling capability (A)	1.0
Active chip area (μmxμm) (excluding pads)	290x290
Total channel width (μm)	31878
Cell pitch (μm)	4.1
Source/Drain junction size (μmxμm)	3.3x3.3
Specific on-resistance (μΩ.cm^2) at V_{GS}=3.3 V	117.46
On-Resistance (mΩ)	90.1
Total gate charge (nC) at V_{GS}=3.3 V	0.34
FOM=R_{on}xQ_g (mΩ.nC)	30.6

1. when the device is tested experimentally a pulsed current source is used to plot the gate charge versus V_{GS}

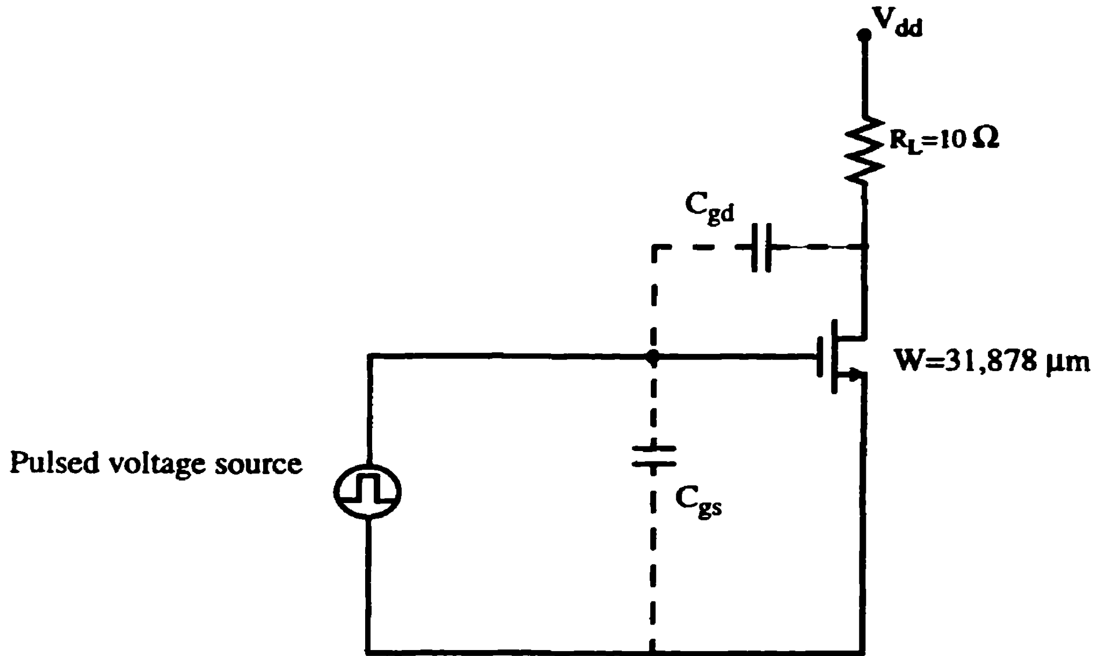

Fig. 2.14: Schematic of test circuit used in extracting charge transfer characteristics using CA-AAM

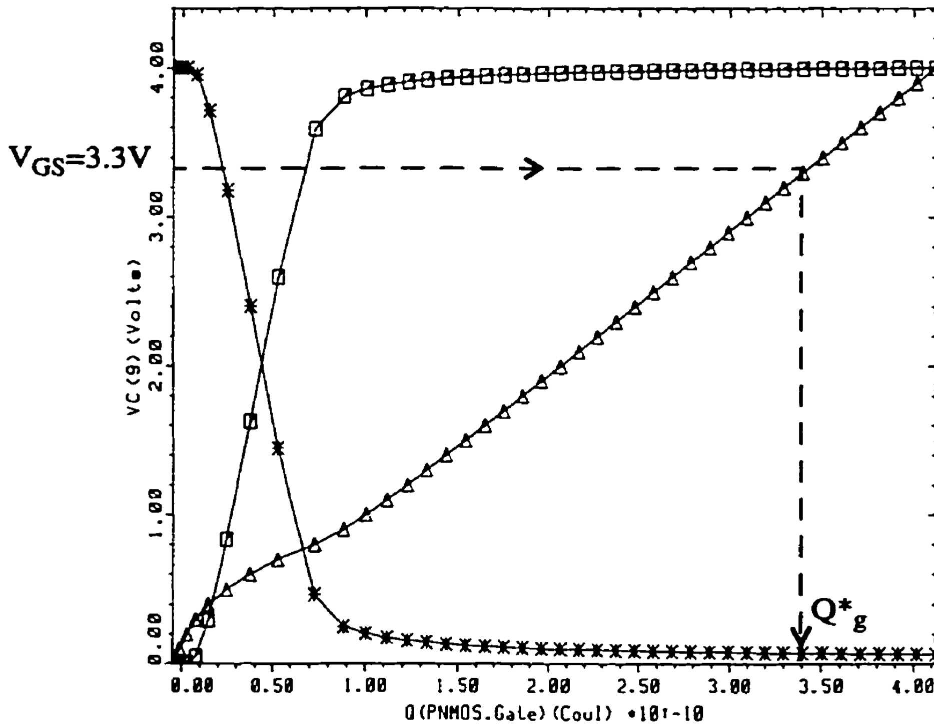

Fig. 2.15: Simulated charge transfer characteristics of the 0.8 μm switch (W=31,878 μm)

While the simulated FOM (30.6 mΩ.nC) for the 0.8 μm implies significant improvement in efficiency over vertical structures, the target specification to achieve a FOM of less than 10 mΩ.nC (corresponding to 95% efficiency) cannot be achieved using such process.

Furthermore, the simulated on-resistance does not account for the parasitic resistance of the metal runners (de-biasing effects) [13]. This resistance becomes significant in large devices. In order to reduce the resistance contribution of the metal to the on-resistance, layout patterns incorporating multilevel of metallization are necessary. Multilevel metallization also results in higher packing densities, especially, if the process features full stacking of contacts and via and/or borderless contacts are allowed [5]. Fig. 2.16 illustrates the area saving resulting from the use of stacked contacts and metal layers as well as borderless contacts.

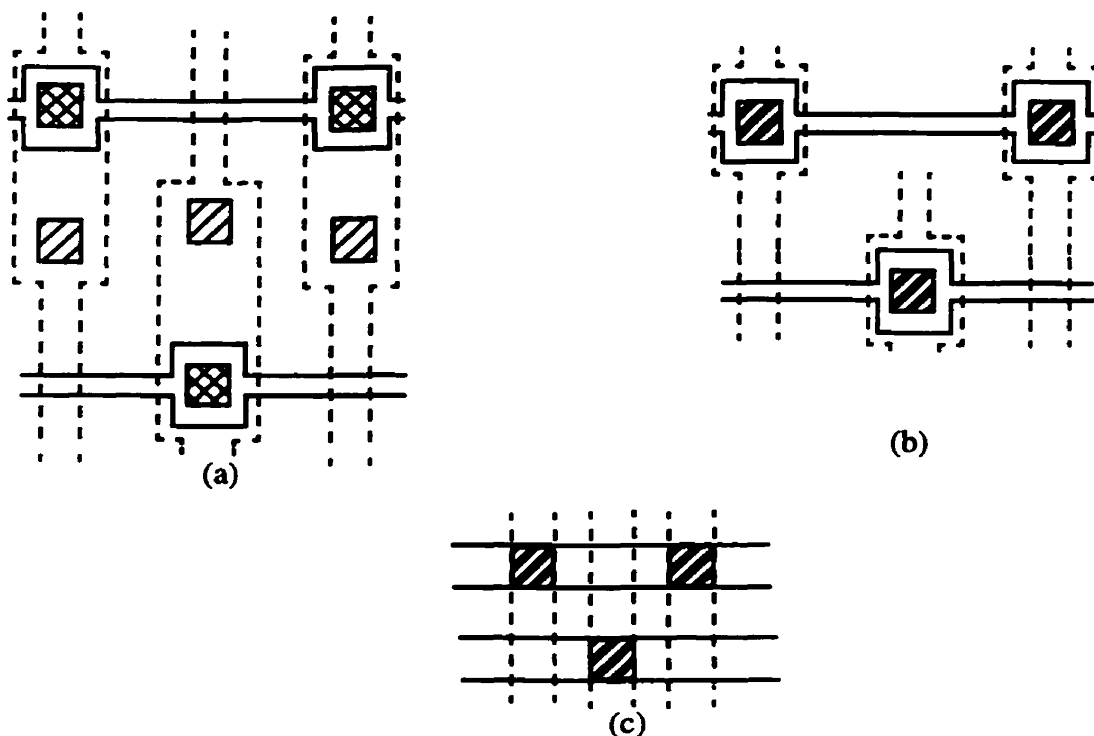

Fig. 2.16: Stacked contacts and borderless contacts: (a) No stacking and borders, (b) stacking and borders (c) stacking and borderless

These advances enable the use of narrow-stacked metal layers as metal runners, as a result they can accommodate high current densities without the need for wide metal runners.

Deep submicron processes available today offer multilevel metallization and features such as full stacking of metal layers, contact and via are becoming standard due to advances in contact fabrication processes. In addition, and most importantly they offer high current drive and high packing density. The 1-A power switch specifications can therefore be greatly improved by using deep-submicron CMOS process technology. In Chapter 3, a 1-A power MOSFET switch implemented in 0.25 μm-5 level metallization process is investigated in an effort to further improve the performance of the switch and to achieve a FOM less than 10 mΩ.nC.

2.8 Summary

This chapter presented the design of 1-A power MOSFET switch in low voltage CMOS technology. The design uses a 0.8 μm - single level metal process. Fabrication steps, design issues, layout techniques and simulation results were discussed. The switch was constructed using a checkerboard layout pattern to maximize the W/A ratio resulting in an active chip area of 290×290 μm^2 corresponding to a total width of 31,878 μm. Simulation results show a specific on-resistance of 117.46 $\mu\Omega.cm^2$. The switch FOM is 30.6 mΩ.nC which compares favorably with commercial devices based on vertical structures rated at 20-30 V, however, it fell short of achieving the targeted 10 mΩ.nC.

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CHAPTER 3

1-A Power MOSFET in 0.25 µm CMOS Technology

3.1 Introduction

The performance of the power switch presented in Chapter 2 and implemented in 0.8 µm base line and single level metallization can be significantly improved through device scaling and the use of multiple level metallization. Using an advanced deep-submicron technology can result in a substantial increase in the packing density due to the shorter channel length, the smaller contact areas and spacing as well as the use of contacts stacking and multi level metallization.

Associated with the increase in packing density is a smaller specific on-resistance and higher current drive. The higher the current drive the smaller the required total width of the power switch, resulting in reduced input capacitance and gate charge.

In this Chapter, the design and implementation of a 1 A N-channel power switch implemented in a 0.25 µm, 5 level metallization CMOS process is presented. Simulation of the 0.25 µm unit cell was carried out in order to predict the performance of a device fabricated in such technology. Experimental results are presented and the measured parameters are compared with simulation results.

3.2 The 0.25 μm MOSFET Unit Cell

To predict the performance of the 0.25 μm power MOSFET switch, process and device simulations were performed for the unit cell*. Simulations can provide a reasonable insight on the extent of performance improvements one might obtain by the scaled-down process.

Suppression of short channel effects (SCE) constitute the main design challenge in a scaled-down process. A solution to alleviate short channel effects is the use of lateral channel doping engineering such as pocket and halo implant which provide the possibility to effectively tailor the short-channel performance[1].

The pocket implant, illustrated in Fig. 3.1, raises the concentration of the p-well around the source and drain junctions without increasing the concentration in most of the channel region, hence, the depletion region widths, responsible for SCE, are reduced and the channel carrier mobility is not significantly degraded.

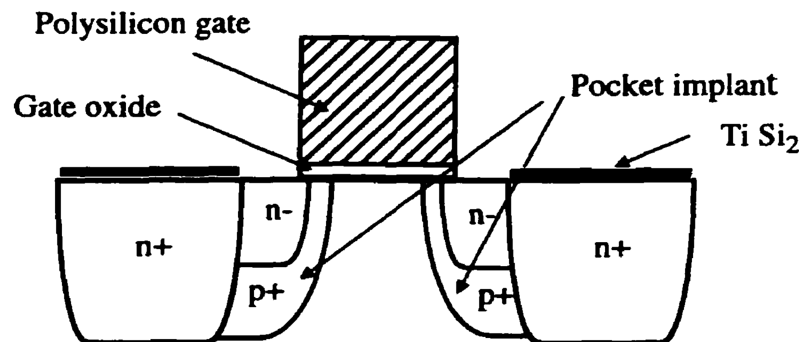

Fig. 3.1: Cross section of an LDD MOSFET including pocket implant

A technique used to implement the pocket implant involves the use of large-angle-tilt (LAT) implantation[2-3] in which the ion beam is oriented by a large angle, typically, 30° to 40° and the implantation is masked by the gate electrode and a $TiSi_2$ film. The stopping power of $TiSi_2$ is 1.5 times that of silicon, therefore, by adjusting the dose, energy and the

*. The manufacturer's documentation provided most of the information on the structure and the process used in this fabrication. This information is proprietary.

tilt angle of the ion-implant, very localized pocket profiles can be fabricated using this method. Process sequence of the pocket fabrication are illustrated in Fig. 3.2.

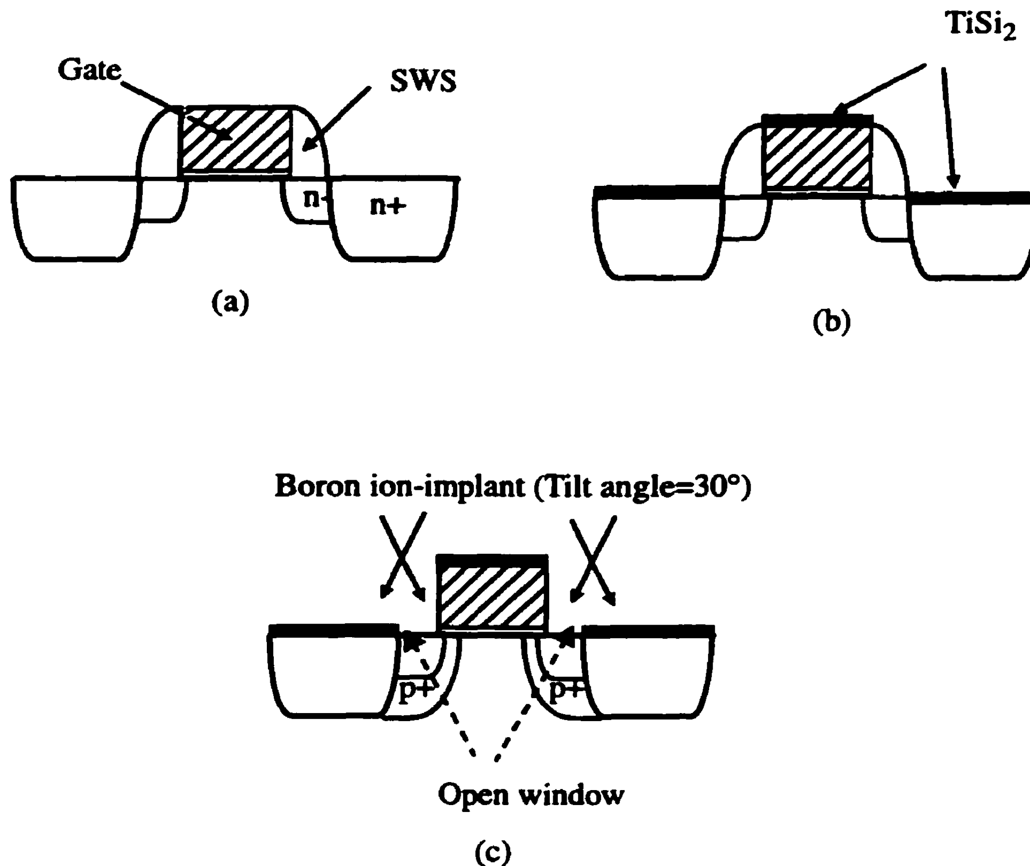

Fig. 3.2: Steps for pocket implant fabrication (a) LDD and S/D implantation (b) salicide formation (c) SWS removal and LAT ion-implantation

Process simulations were carried out for a unit cell of 1.85 μm cell pitch which was used in the layout of the power switch. The structure is the same as the one used for the 0.8 μm with the proper scaling of the gate length, source/drain junction depths, oxide thickness and p-well doping profile with the only major difference being the incorporation of the pocket implant.

3.2.1 Layout of the 0.25 μm Unit Cell

The layout of the unit cell is illustrated in Fig. 3.3a which is the main building block of the power switch. The channel length used in the layout of the unit cell is 0.25 μm. The ability to stack multiple contact and vias as well as metal layers resulted in a cell pitch of 1.85 μm. The minimum widths of the metal layers used in the layout are dictated by electromigration guidelines as suggested by the manufacturer. Using too thin metal runners may result in switch faliure.

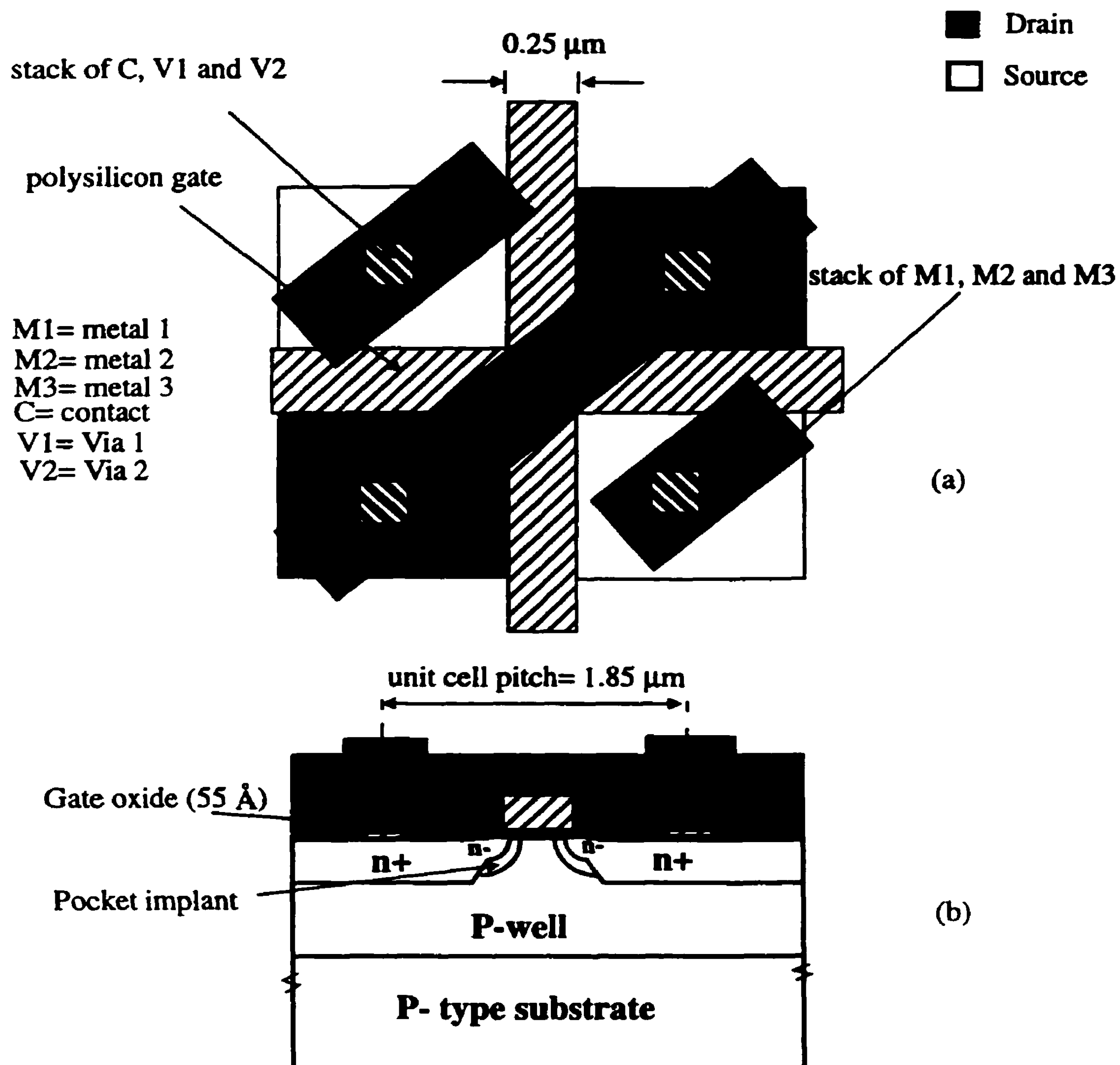

Fig. 3.3: Unit cell (a) layout (b) cross section

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(Section 3.2.2)

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3.3 0.25 μm Power MOSFET Switch Layout

A checkerboard layout pattern was used in the layout of the 1 A - 0.25 μm power MOSFET switch. The layout shown in Fig. 3.7, uses: (1) a stack of 3 metal layers to reduce the cell pitch and minimize the de-biasing effects and (2) a p+ substrate contact on the surface.

A power switch with a 1 A current carrying capability can be constructed using a 63×63 array of alternating source and drain junctions equivalent to a total channel width of 12,499 μm and exhibiting an on-resistance R_{on} of 61 mΩ.

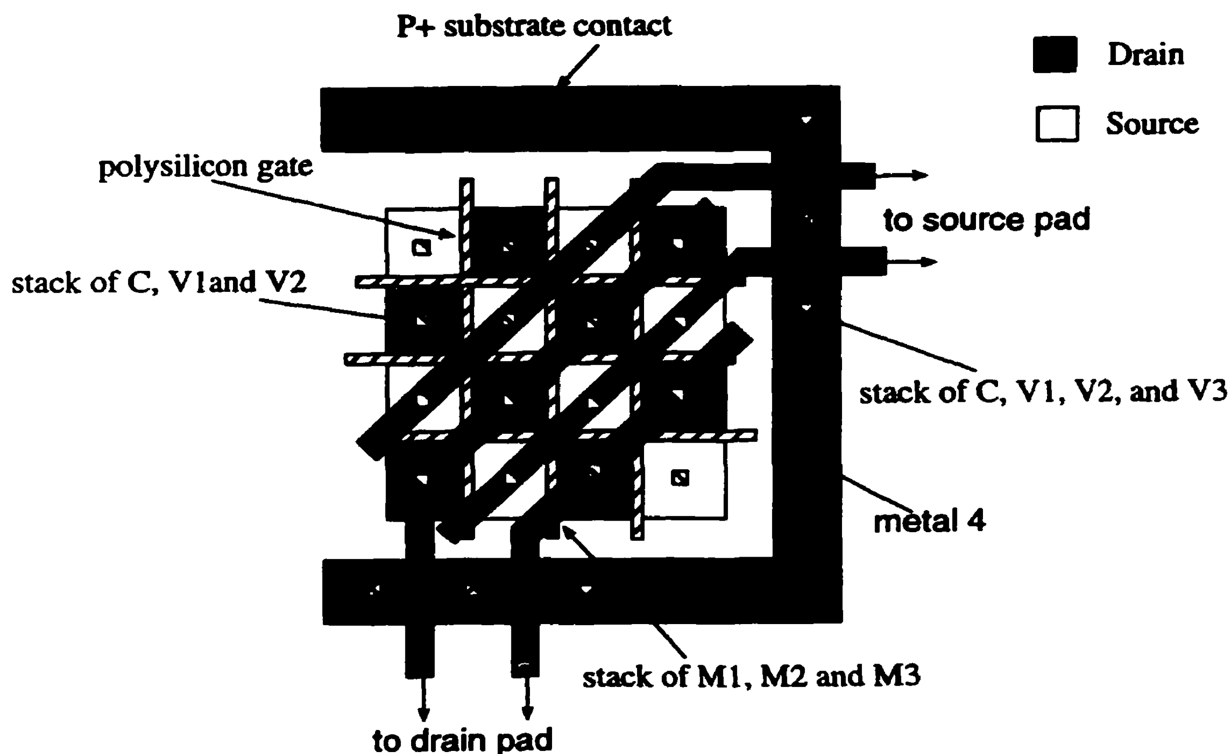

Fig. 3.7: Checkerboard layout pattern for the 0.25 μm switch

3.3.1 Charge Transfer Characteristics and Figure Of Merit (FOM)

The charge transfer characteristics of the device were obtained using the MEDICI CA-AAM software package and the circuit configurations is shown in Figure 2.14 and discussed in Section 2.7.

The input file to CA-AAM includes the device model generated by MEDICI and a netlist of the circuit configuration. The resulting charge transfer characteristics is shown in Fig. 3.8. The total gate charge Q_g necessary to charge the input capacitance C_{iss} and raise its voltage to 3.3 V is 0.074 nC which results in a FOM ($R_{on}xQ_g$) of 4.51 mΩ.nC.

The significant improvement of the FOM over that of the 0.8 μm device discussed in Chapter 2 is attributed to the higher packing density and current drive of the 0.25 μm process. This is clearly reflected in the relatively small device area required to implement a 1-A power switch. The key device parameters for the 0.25 μm switch are summarized in Table 3.1.

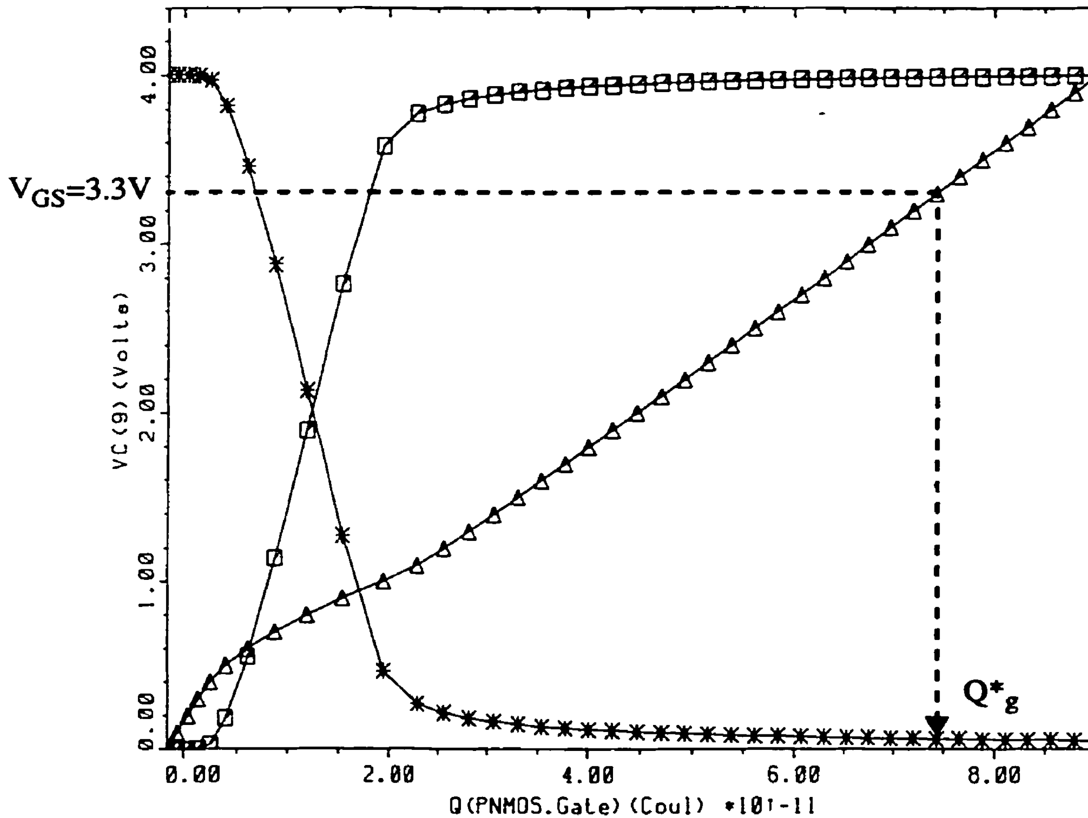

Fig. 3.8: Charge transfer characteristics of the 0.25 μm switch W=12,499 μm

Table 3.1: Key process and device parameters of the 0.25 μm switch (simulation)

Parameter/Units	0.25 μm / 55 Å process
Operating Voltage (V)	3.3
Forward blocking capability (V)	7
Current handling capability (A)	1.0
Chip size (μmxμm) (excluding pads)	130 x130
Cell pitch (μm)	1.85
Source/Drain junction size (μmxμm)	1.6x1.6
Specific on-resistance ($\mu\Omega.cm^2$) at V_{GS}=3.3 V	14.8
On-Resistance (mΩ) at V_{GS}=3.3 V	61
Total gate charge (nC) at V_{GS}=3.3 V	0.074
FOM=R_{on}xQ_g (mΩ.nC)	4.51

3.4 Experimental Results

The mask layout of the test chip is shown in Fig. 3.9 and includes the power MOSFET switch and other test structures to verify the electrical characteristics of the process.

A micrograph of the switch is shown in Fig. 3.10. The structure includes pads for probing, however, in actual on-chip implementation these pads are not included. Hand calculations of the parasitic capacitance associated with the pad structure predicts a rough value in the order of 10^{-13} Farad.

The DC measurements including output, transfer and breakdown characteristics as well as the on-resistance were performed by probing loose dice (on-wafer measurements), while gate charge, rise and fall times measurements were done on packaged devices.

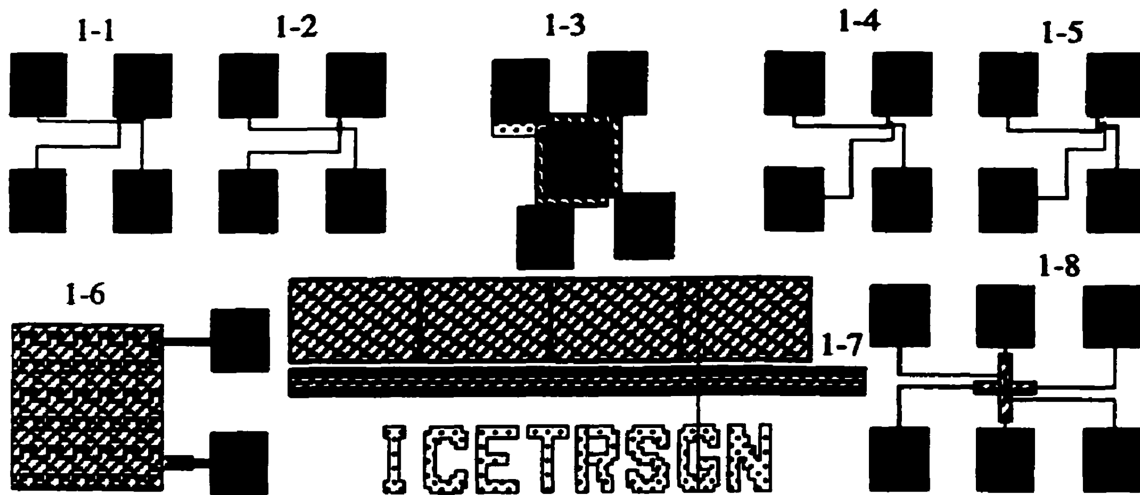

Fig. 3.9: Layout of the test chip

Table 3.2: List of test elements

Location	Description	Objective
1-1	Single-NMOS W/L=1.6/0.25 (μm/μm)	electrical characterization
1-2	Single-NMOS W/L=20/0.25 (μm/μm)	electrical characterization
1-3	Power MOSFET Switch W/L=12,499/0.25(μm/μm)	electrical characterization
1-4	2x2 Array-NMOS W/L=6.4/0.25 (μm/μm)	electrical characterization
1-5	4x4 Array-NMOS W/L=38.4/0.25 (μm/μm)	electrical characterization
1-6	300x300 μm^2 capacitance	C-V measurements
1-7	Structure for SEM inspection	SEM inspection
1-8	Kelvin structure	contact resistance measurement

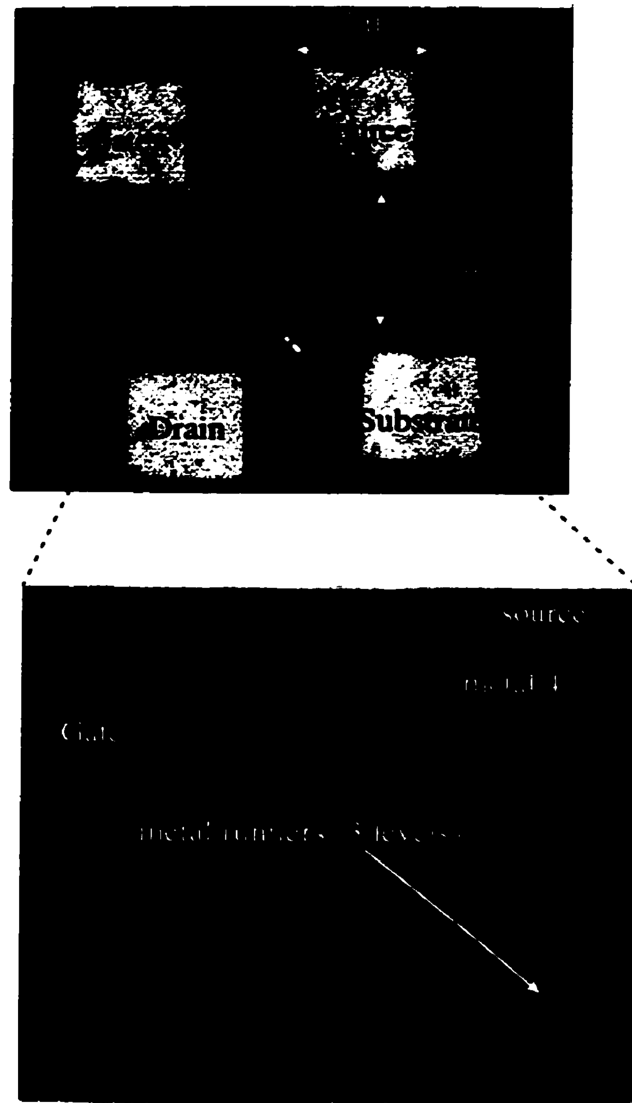

Fig. 3.10: Micrograph of the 0.25 μm switch

3.4.1 Output Characteristics

The output characteristics (I_D-V_{DS}) of the device are shown in Fig. 3.11. In these measurements two probes where used to sweep the drain voltage V_{DS} and another two probes connected to a high impedance voltmeter where used to measure the voltage difference between the source and the drain, as a result, the voltage drop at the probes contact were eliminated.

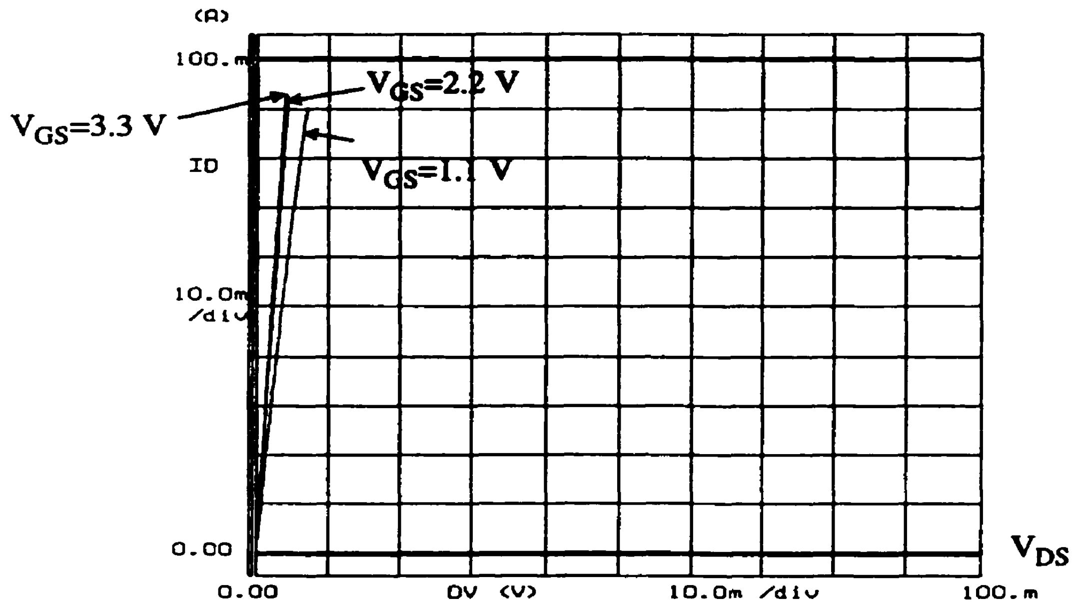

Fig. 3.11: Experimental output characteristics of the 0.25 μm switch

3.4.2 Transfer Characteristics

The transfer characteristic (I_D-V_{GS}) of the switch is shown in Fig. 3.12. From the figure the threshold voltage was extracted as the intercept of the x-axis with a line extrapolated form the linear region of the I_{DS}-V_{GS} curve. For the device tested, the extracted threshold voltage was 0.329 V. The measured threshold voltage is roughly 130 mV less than the expected value. This drop in threshold voltage is attributed to threshold voltage shifts caused by transient enhanced diffusion encountered in power MOSFETs with closed-cell checkerboard layout patterns[4]. Transient enhanced diffusion occurs due to the formation of interstitial sites at the surface of the device following ion-implantation which causes the

boron to pile up everywhere except at the device corners due to 3-D effects, hence, the device exhibits a threshold voltage that is lower than conventional MOSFETs.

The logarithmic transfer characteristic of the device is shown in Fig. 3.13. The device exhibits a subthreshold leakage current is 590 nA and a subthreshold slope of 78.13 mV/decade.

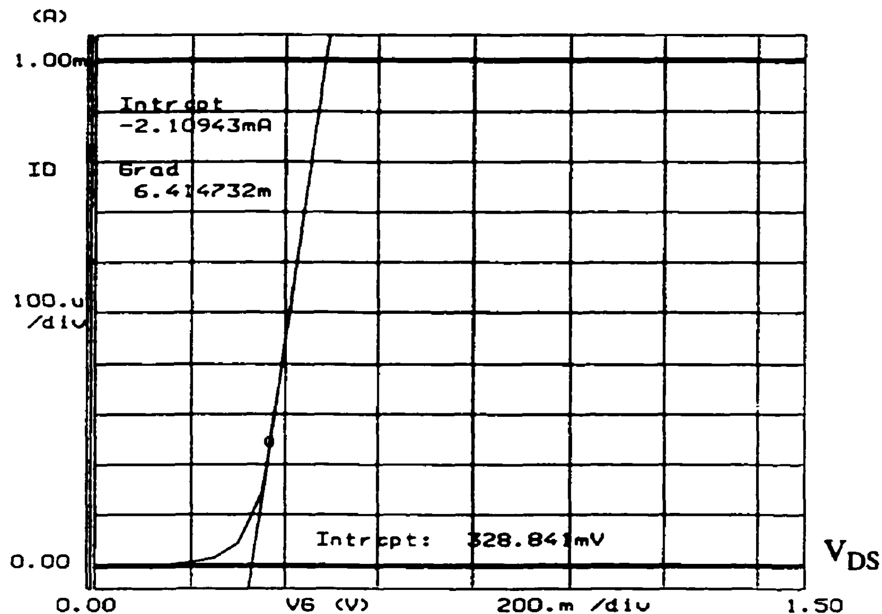

Fig. 3.12: Experimental transfer characteristics of the 0.25 μm switch

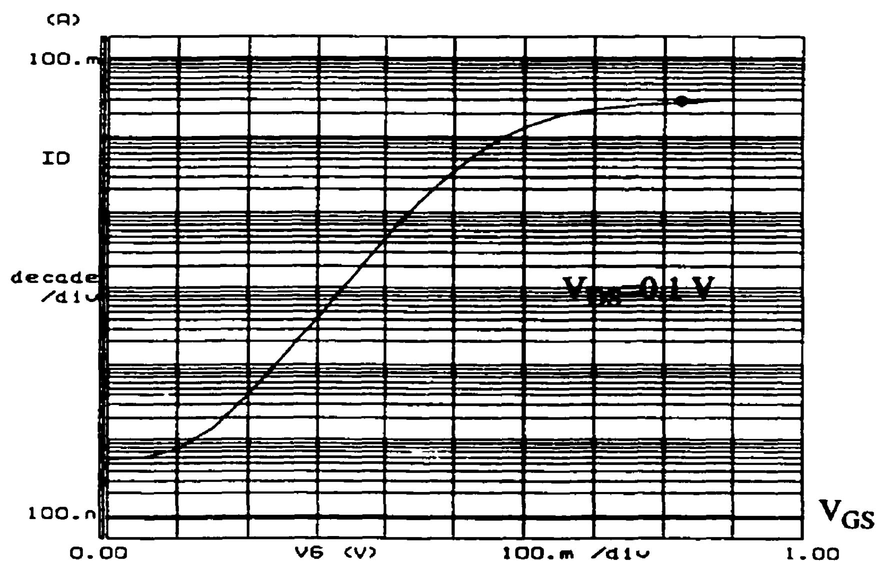

Fig. 3.13: Experimental subthreshold characteristics of the 0.25 μm switch

3.4.3 Breakdown Voltage (BV_{DS})

The breakdown voltage characteristics of the switch is shown in Fig. 3.14. Breakdown voltage measurements were performed to show the switch ability to withstand high input voltage (forward blocking capability). The value of the breakdown voltage is defined as the drain voltage at which a drain current of 10 μA flows. The measured breakdown voltage is approximately 7.1 V which is sufficient for the application on hand and in agreement with simulation and manufacturer's data specification.

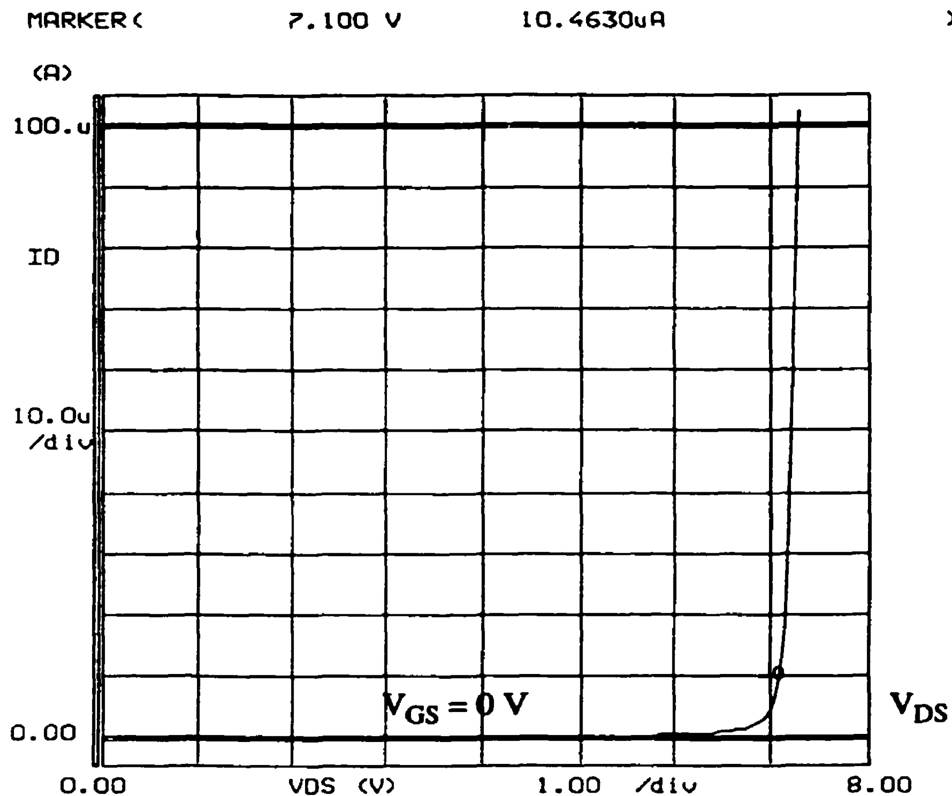

Fig. 3.14: Breakdown voltage measurements for the 0.25 μm switch

3.4.4 On-Resistance

The switch on-resistance was measured using the 5 point probe configuration, shown in Fig. 3.15 which is similar to the Kelvin structure measurement method[5]. A current I_f is forced between the outer two probes and the voltage difference ΔV is measured between the inner two probes using a high impedance voltmeter. Since the high impedance voltmeter allows very little current to flow in the probes, the voltage difference ΔV is solely due to the voltage drop across the switch on-resistance R_{on} [6-7], thus, eliminating any voltage drops across the probe contact resistance.

The switch on-resistance can then be calculated using the equation

$$R_{on} = \frac{\Delta V}{I_f} \qquad (3\text{-}11)$$

A plot of the switch on-resistance versus the gate voltage is shown in Fig. 3.16,. The measured on-resistance value at V_{GS}= 3.3 V is 40.37 mΩ corresponding to a specific on-resistance of 6.882 $\mu\Omega.cm^2$.

The measured on-resistance value is less than the simulated one (61 mΩ). This discrepancy can be attributed to the threshold voltage shift due to transient enhanced diffusion as discussed in Section 3.5.2.

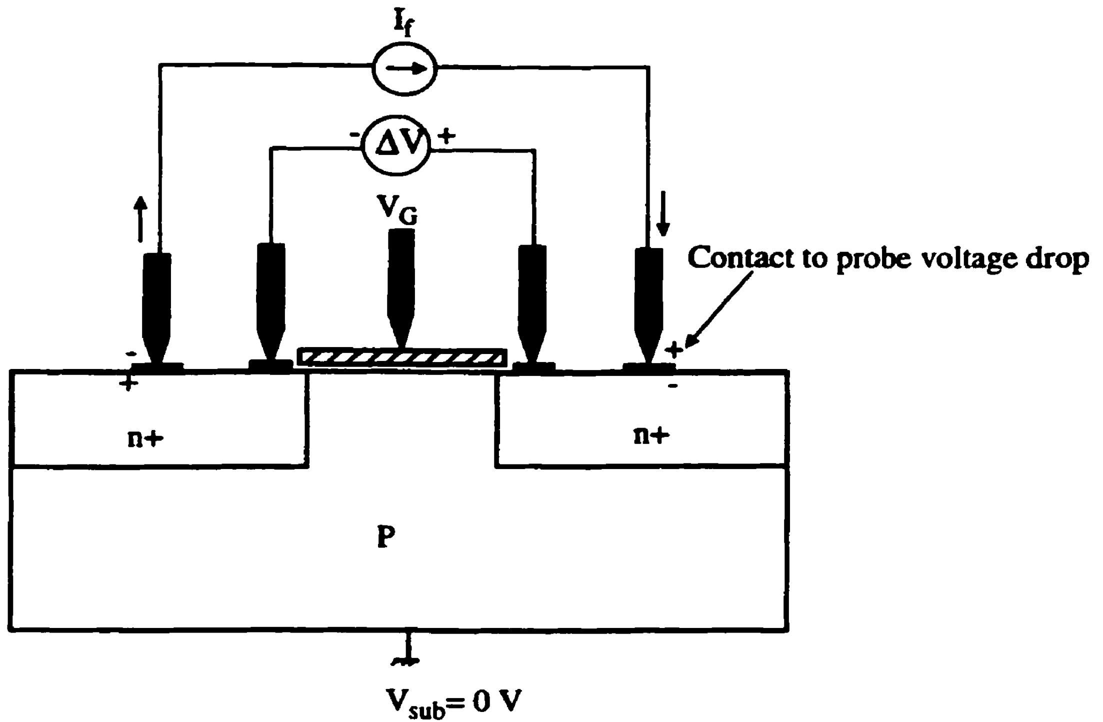

Fig. 3.15: On-resistance measurement setup

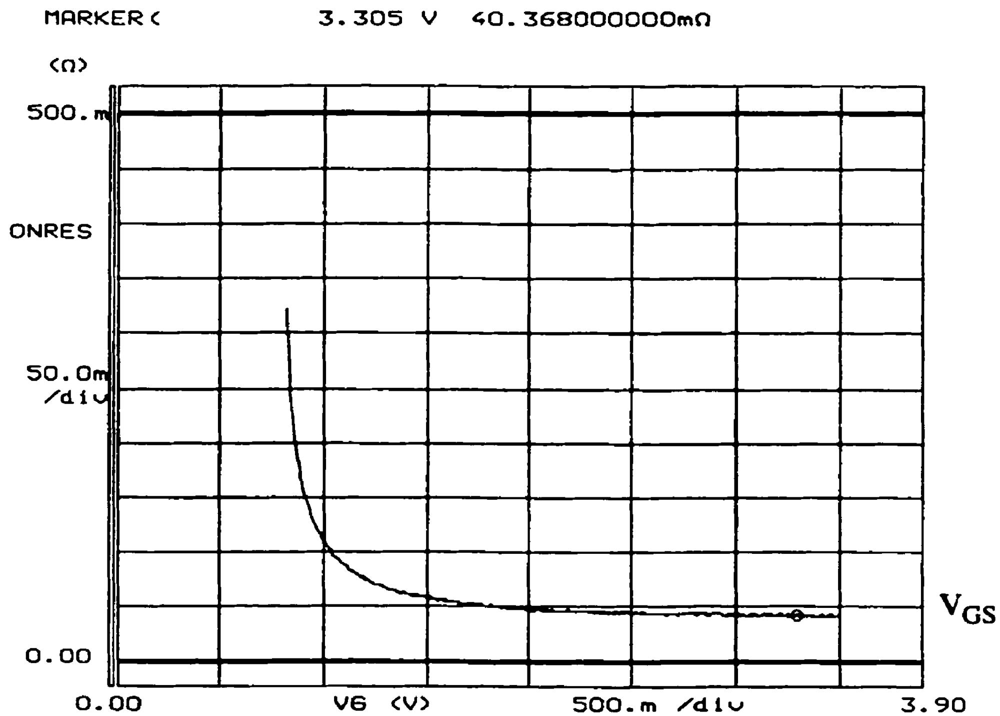

Fig. 3.16: Experimental on-resistance versus gate voltage for the 0.25 μm switch

3.4.5 Total Gate Charge Q_g and Figure Of Merit (FOM)

The total gate charge Q_g was obtained from the charge transfer characteristic (V_{gs}-Q_g). This characteristic was arrived at using the circuit illustrated in Fig. 3.17 by applying a current pulse to the gate of the device under test (DUT) and observing the gate to source voltage V_{gs} with respect to time. The duration of the current pulse must be large enough to charge the device input capacitance C_{iss} and raise the gate to source voltage to a predetermined value.

A typical gate to source voltage waveform versus time is shown in Fig. 3.18. The charge transfer characteristic is obtained by converting the time-axis in Fig. 3.18 to a charge-axis by multiplying the time scale by an appropriate scaling factor according to the relation

$$Q_g = I_{ch} \times t \tag{3-12}$$

where I_{ch} is the peak value of the current pulse and t is the time. The resulting charge transfer characteristic for the device under test is shown in Fig. 3.19.

Measurements show that the device exhibits a total gate charge of 0.105 nC at a gate voltage of 3.3 V. The simulated total gate charge of the switch is 0.074 nC. The difference between the measured and the simulated gate charge values is 0.031 nC which corresponds to the effective parasitic capacitances due to packaging, external wiring interconnects and the breadboard used in this test. The resulting Figure Of Merit FOM for the device is 4.24 mΩ.nC which satisfies our target specification.

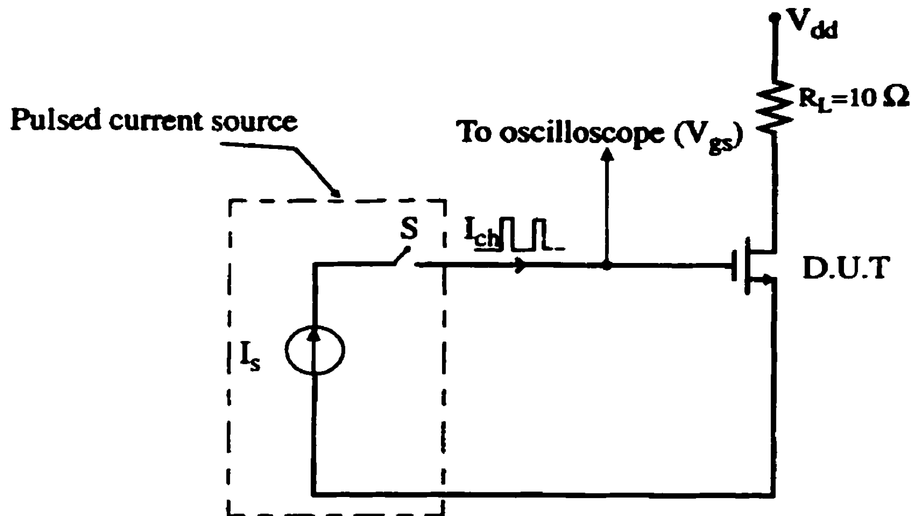

Fig. 3.17: Test circuit used to obtain charge transfer characteristic

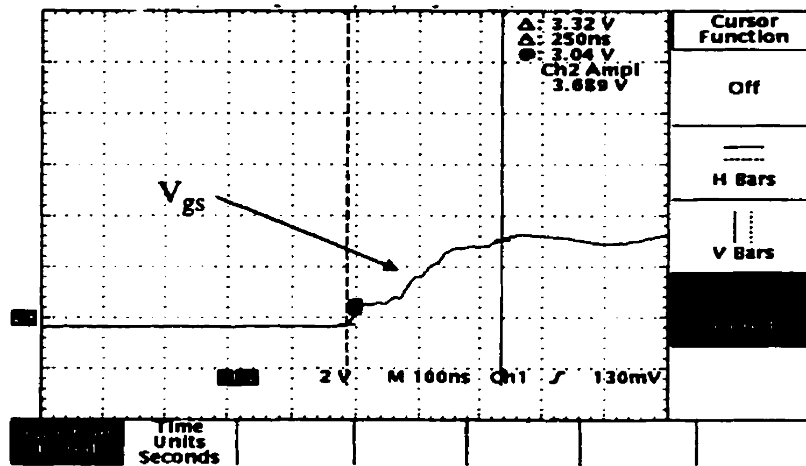

Fig. 3.18: Gate to source voltage waveforms during the charging of the input capacitance C_{iss} (current pulse 0.42 mA peak)

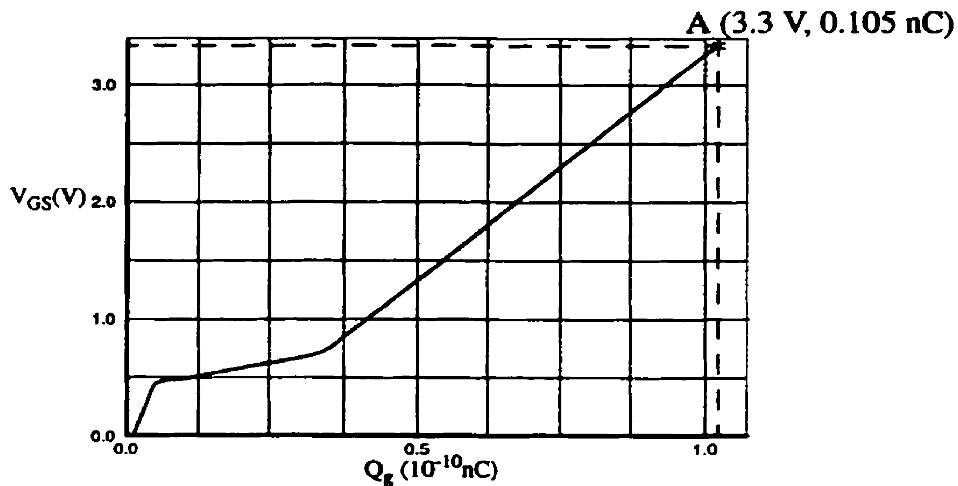

Fig. 3.19: Measured charge transfer characteristic for the 0.25 μm switch

3.4.6 Rise and Fall Time

The device rise and fall times were measured in a common source configuration under resistive loading conditions using the circuit in Fig. 3.20. The typical measured rise and fall times of the switch are 5.8 and 3.5 ns, respectively.

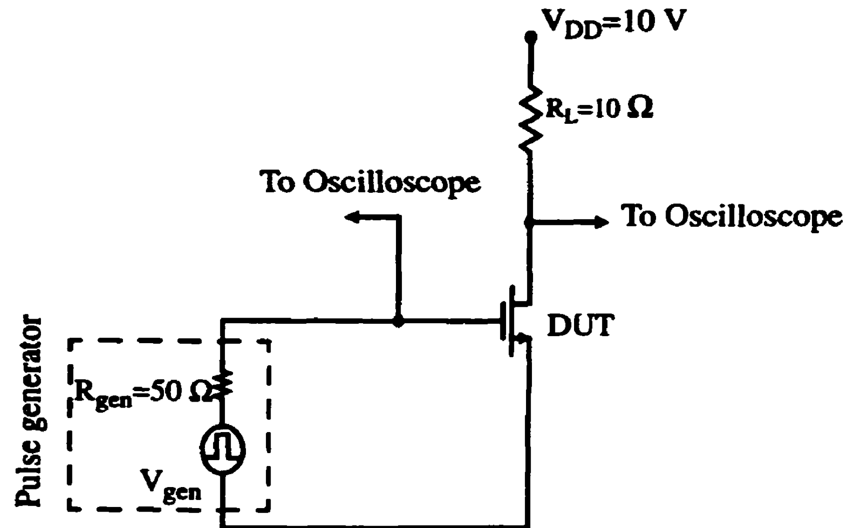

Fig. 3.20: Test circuit for rise and fall times measurements

3.5 Summary

In this chapter the design, implementation and characterization of a 1 A - power MOSFET switch were discussed. Simulations results were presented. The use of 0.25 μm design rules together with the full stacking capability of contacts and vias as well as multiple metal layers resulted in an extremely compact chip area of 16,900 μm^2 for 1 A current handling capability.

The switch was successfully tested and exhibited an on-resistance of 40.37 mΩ, a total gate charge of 0.105 nC corresponding to a FOM of 4.24 mΩ.nC.

The experimental results are in good agreement with simulations. The measured and simulated specifications of the power MOSFET switch are summarized in Table 3.3. All design specifications have been met. The FOM of the switch based on measurements satisfy the requirement for FOM<10 mΩ.nC which is necessary to achieve a converter efficiency of at least 95% at 10 MHz as mentioned in Chapter 1.

Table 3.3: Measured and simulated specifications of the 0.25 μm switch*

Parameter	Measured Value	Simulated Value
Current carrying capability (A)	1.0	1.0
Operating Voltage (V)	3.3	3.3
Forward blocking capability (V) at I_D=10 μA	7.1	7.0
Active area (μmxμm)	130x130	-
Total channel width (μm)	12,499	12,499
Specific on-resistance (μΩ.cm^2) at V_{GS}=3.3 V	6.882	14.8
On-Resistance (mΩ) at V_{GS}=3.3 V	40.37	61
Total gate charge (nC) at V_{GS}=3.3 V	0.105	0.074
FOM=R_{on}xQ_g (mΩ.nC) at V_{GS}=3.3 V	4.24	4.51
Fall time, t_f (ns)	3.5	-
Rise time, t_r (ns)	5.8	-

*. The above measurements represent typical values obtained on several chips. Variation from chip to chip ranged within ±5%

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CHAPTER 4

Conclusions

Motivated by the demand for low power losses in the semiconductor power switches in on-chip high efficency portable switch mode DC/DC converters, two low-voltage power MOSFETs were investigated.

In Chapter 2 the design issues of a 1 A power MOSFET switch using a low-voltage 0.8 μm - single level metallization CMOS compatible process were discussed. In order to achieve low $R_{on} \times Q_g$ product, the device structure, doping profiles and the unit cell layout were optimized for minimum specific on-resistance. A cell pitch of 4.1 μm was used for the unit cell simulation. Simulation results of the unit cell yields a specific on-resistance of 117.46 $\mu\Omega.cm^2$. A power switch with current carrying capability of 1 A can be constructed using a device with total width of 31,878 μm corresponding to an active chip area is 290×290 μm^2. The simulated FOM of the switch is 30.94 mΩ.nC which is larger than the targeted value (10 mΩ.nC). Although the FOM indicates significant performance improvements over vertical power MOSFETs, the performance is limited by the minimum line width and the number of metal layers used in the 0.8 μm process.

A second switch was designed and implemented experimentally in a 0.25 μm - 5 level metallization process. The aggressive layout design rules and the ability to stack multiple contacts and metal layers resulted in a cell pitch of 1.85 μm. A specific on-resistance of 6.822 $\mu\Omega.cm^2$ was achieved. The low specific on-resistance is attributed to the process high current drive and high packing density. 1 A switch was implemented using a device with a total width of 12,499 μm corresponding to a very compact active chip area of 130×130 μm^2.

Experimental results show that the switch is able to achieve a rise and fall time of 5.8 and 3.5 ns, respectively, an on-resistance of 40.37 mΩ, a total gate charge of 0.105 nC and a FOM of 4.24 mΩ.nC which meets the target specifications necessary to achieve a converter efficiency of 95%.

The low on-resistance, gate charge and fast switching times reported here in this thesis clearly demonstrate the advantages of the implementation of the switch in a ULSI based process, making the switch a suitable candidate for on-chip, high-frequency switch mode DC/DC converters.

Future work can take advantage of new developments in interconnects and contact processes by incorporating Cu interconnects to reduce de-biasing effects and make use of borderless contacts to increase the packing density. Consideration can also be given to reduce the gate resistance using special silicide materials and new layout techniques to further reduce the chip area for a given current carrying capability.

Appendix A

Layout Design Rules for the 0.8 μm Process

The layout design rules for the 0.8 μm process are based on a minimum alignment tolerance of 1.5λ and minimum line width of 2λ, where 2λ = 0.8 μm. The total number of masks are 4 (for N-channel MOSFET). The rules are listed below:

A. Active (Mask # 1, Active)

a.1 minimum width= 6λ

a.2 minimum spacing=3λ

B. Polysilicon gate (Mask # 2, Poly)

b.1 minimum width= 2λ

b.2 minimum spacing= 2λ

b.3 minimum overlap with active= 3λ

C. Contact (Mask # 3, Con)

c.1 minimum width= 2λ

c.2 minimum spacing to poly= 2λ

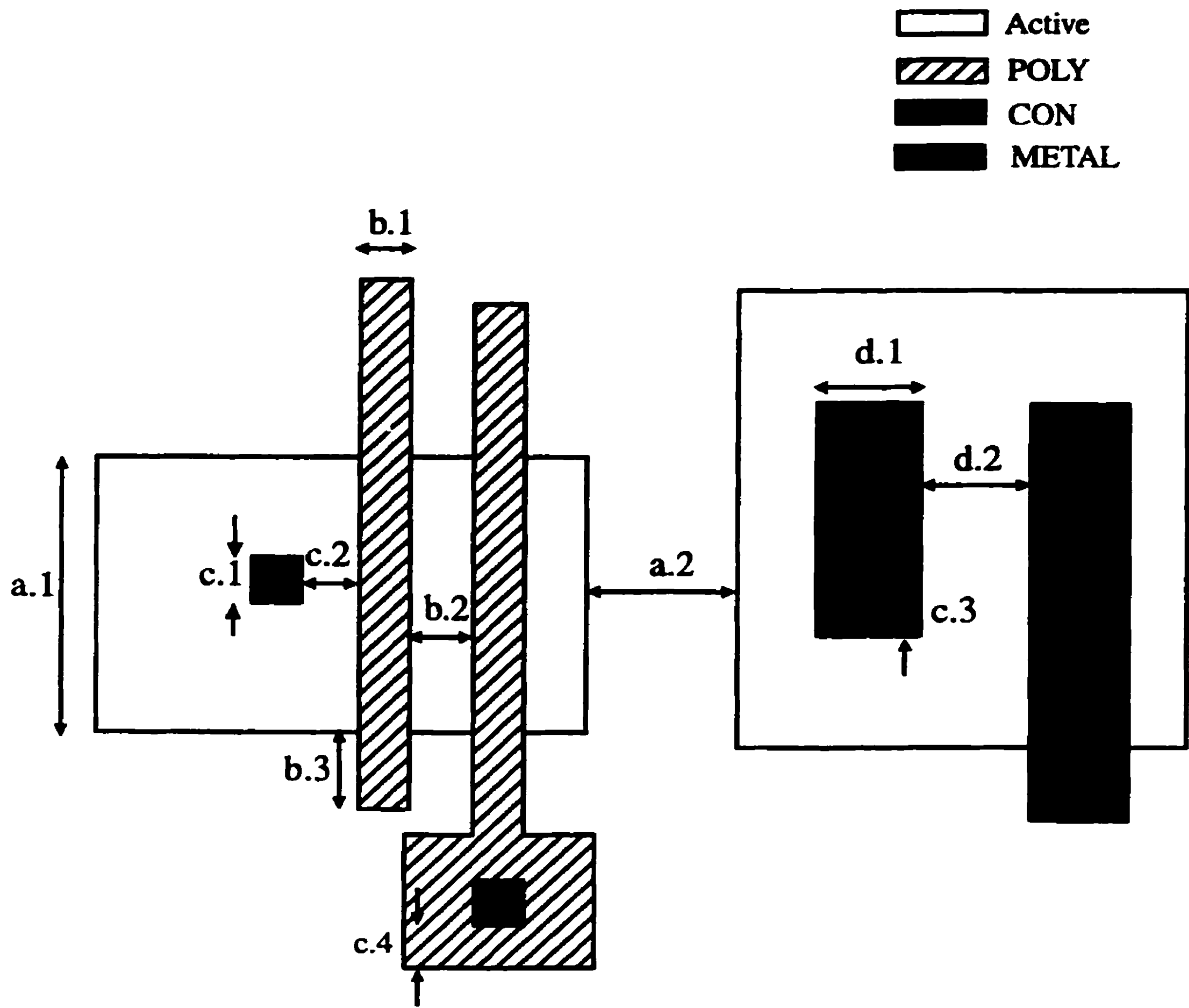
c.3 minimum overlap of metal= λ

c.4 minimum overlap of poly= 2λ

D. Metal (Mask # 4, Metal)

d.1 minimum width= 3λ

d.2 minimum spacing= 3λ


Active
POLY
CON
METAL
b.1
d.1
d.2
a.1
c.1
c.2
b.2
a.2
c.3
b.3
c.4