A Systematic Methodology to Improve CMOS Transconductors for Low Power and Wideband Operation

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ABSTRACT

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A CMOS transconductor is a functional block which can transfer voltage signals to current signals. Thus, it is a commonly used interface between the physical world and the current signal processing systems. In order not to affect the performances of the main current signal processing system, high-performance transconductor structures need to be designed. The major concerns of modern analog systems include lower power dissipation and wider bandwidth in addition to the application related performances, such as, high gain, high linearity and so on.

Unlike most researches that have been conducted on improving the single performance of a transconductor structure, a systematic methodology which targets on the performance-power ratio of CMOS transconductors is proposed in this work. The objective function defined for optimizing the performance-power ratio is a transconductor's frequency versus power ratio. The significance of the frequency-power ratio is that it represents how much bandwidth a structure can achieve while consuming unit DC power. A transconductor structure with maximal frequency-power ratio provides wider bandwidth than the structure with non-maximal frequency-power ratio when both consume the same DC power; or on the other hand, the structure with maximal frequency-power ratio consumes less DC power than the non-maximized structure when both operate at the same bandwidth.

Theoretical derivations, numerical calculations as well as HSPICE simulations on various transconductor structures are conducted to prove the effectiveness of the proposed optimization methodology. Two test chips are also fabricated and measured to verify the analyses. A few transconductor-based analog systems are studied to illustrate the impact of the transconductor optimization on the system. Other important design issues, such as, environmental variations, are also discussed in the work.

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List of Symbols and Abbreviations

g_{ac}	AC transconductance
P_{diss}	DC power dissipation
Io	Output current
W	Channel width of a MOS transistor
L	Channel length of a MOS transistor
V_{th}	Threshold voltage of a MOS transistor
μ	Mobility of carriers
λ	Channel length modulation factor
V_{dd}	Positive supply voltage
V_{ss}	Negative supply voltage
I_{out}	Output current
CMOS	Complementary MOS
CMRR	Common mode reject ratio
THD	Total harmonic distortion
BPF	Band pass filter
LPF	Low pass filter
HPF	High pass filter
SNR	Signal noise ratio

Chapter 1

Introduction

1.1 Low-power Low-voltage signal processing

Conventionally, analog signal processing has been dominated by processing signals as voltages. Transistors have been routinely assembled into voltage oriented circuits and current signals transferred into voltages before next phase of signal processing takes place. However, researchers did realize that current signals can also be employed as design variables and current mode signal processing provides some advantages over its voltage mode counterpart such as increased bandwidth, higher dynamic range, simpler circuitry and lower power dissipation [1]. Theories for current mode circuits had already been studied in 1960's. Elegant current signal processing building block (although their significance was not recognized at the beginning), such as current conveyor [2], was invented in 1960's. Nevertheless, the wide spread use and acceptance of current-mode signal processing was not considered seriously by researchers until the era of sub-micron IC technological processes flourished.

In the past two decades, semiconductor technology has experienced a very rapid developing period. The continuously shrinking transistor feature size enables ultra large scale integration. The state-of-art integration level has reached millions of transistors on a single chip. However, the large integration level results in increasing power consumption. Therefore, low power consumption becomes a major concern of modern electronic designs. An effective approach to reduce power dissipation is decreasing supply voltages. However, for voltage-mode analog designs, lower supply voltage will result in reduced signal swing and lower signal-to-noise ratio (SNR). On the contrary, current-mode analog circuits do not suffer from these performance degradations when supply voltage drops. As the advan-

tages of current-mode signal processing become more and more obvious. While the semiconductor technology is capable of implementing current-mode systems successfully, designers and manufacturers are starting to re-consider the possibility of current-mode implementation of signal processing systems. Current-conveyors are already commercially available (e.g. AD844) and have found applications in many different signal processing systems.

1.2 CMOS Voltage-to-current converter (transconductor)

Although current-mode signal processing can provide solutions to many problems which were carried out as voltage-mode signal processing, in reality, information in the physical world is usually available in the form of voltage signals. Most existing and well-developed analog electronic systems deal with voltage variables. Therefore, it is indispensable for current-mode signal processing systems to communicate with outside world through some form of interface circuits. Two kinds of interface circuits are needed. They are: voltage-to-current converter and current-to-voltage converter. Figure 1.1 shows the block diagram of a general current mode signal processing system and the necessary interface circuits [3].

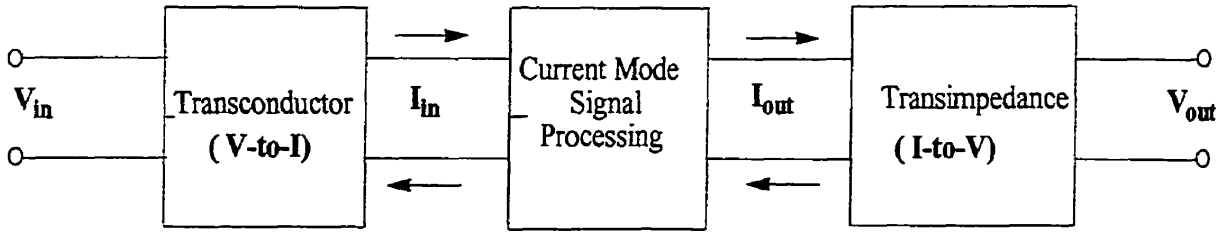


Fig. 1.1 Current-mode Signal Processing System

The interface which precedes the current-mode signal processing block is named transconductor. The interface which follows the current-mode signal processing block is called transimpedance.

The functions of transconductors and transimpedances are reversed. Their topologies are related. Given one topology, the other one can be implemented using the dual topology of the given topology.

Being the "front end" of a current-mode signal processing system, transconductor is usually a crucial part of the system. The overall performances of the system, such as linearity, frequency response and noise, are limited by the performances of the transconductor. Ideally, a transconductor structure should provide high linearity, low noise, wide bandwidth, low power dissipation and insensitivity to the environment variations. A lot of researchers have made contributions to develop high performance transconductor structures since 1980's. Like other circuits, transconductors can be realized using MOS or BJT transistors. Different device types (MOS or BJT) result in transconductors which are appropriate for different applications. Since CMOS technology is dominant in digital system implementation, it is desirable to realize analog systems using CMOS technology as well. The reason is that employing the same technology, a system which consists of both analog and digital circuits can be integrated into one single chip (system-on-chip).

1.3 Research Objective and Outline

The objective of present research is to focus on certain aspects of CMOS transconductors and effect some improvements that have not yet been addressed by other researchers in this area. While transconductors that are meritorious in several aspects, such as low power, low voltage, wide bandwidth, high linearity and so on [3,9,14-22] have been introduced in the circuits and systems area, a key performance measure, that is, desired functionality versus dc power consumption, has not been addressed at length yet. In the research results presented in this thesis, the bandwidth of operation has been chosen as the desired functionality of a transconductor. A methodology which will improve the efficiency of dc power consumption to achieve a given operational bandwidth and vice versa has been

developed from the research.

The focus of this research is thus to improve the frequency-power efficiency of CMOS transconductors. But the efficiencies of other performances versus power dissipation could also be addressed in similar manner. In this research, the frequency-power-efficiencies of various CMOS transconductors are analyzed and optimized. By doing frequency-power efficiency optimization, one can improve the frequency performance of a transconductor when the power consumption is fixed or reduce the power dissipation of the transconductor when the bandwidth characteristic is fixed.

The outline of this thesis is as follows. In chapter 2, transconductors are classified into several categories according to the operating region of the input transistors. Typical CMOS transconductor structures in the literature and their advantages and drawbacks are reviewed. Chapter 3 introduces and explains the idea of frequency-power optimization. The optimization leads to efficient frequency-power performance. Transconductor structures in each category of Chapter 2 are studied and simple single variable optimization on the frequency-power characteristic of the transconductors are performed using analytical approach. This, however, restricts the technique to single variable optimization. The theoretical predictions in Chapter 3 are verified by simulations and experimental tests and the results are presented in chapter 4. Chapter 5 investigates second order effects on the optimization methodology. Analytical formulas obtained in Chapter 3 are reviewed. Based on the results of chapter 5, in Chapter 6, a more general algorithm is employed for the frequency-power analysis using multivariable and constrained optimization. This makes it possible to include factors such as mobility reduction and mismatches in the optimization. Having optimized the transconductors, it appeared interesting to examine its significance on the performances of a transconductor-based system. Therefore, in Chapter 7, the case of a transconductor-C filter, based on optimized transconductors, is considered. Simulations and experiments are also carried out. In order to evaluate the robustness of the proposed optimization technique, the characteristics of the environment are also considered. Envi-

ronment variations, process variations as well as noise characteristic are studied in Chapter 8. Short-channel and narrow-channel effects are also briefly discussed in Chapter 8. Since long-channel models are well-established and understood, long-channel transistors have been used to establish the feasibility of the optimization techniques. Chapter 9 provides conclusions of the thesis.

Chapter 2

CMOS Transconductor Review

Linear transconductors (or voltage-to-current transducers) are fundamental building blocks of analog signal processing system. Their applications include interface circuits, continuous-time filters, A/D, D/A converters, to name a few. Interests on developing high performance MOS transconductor structures date back to the early 1980's. In about two decades, a lot of structures have been proposed and the designs were focussed towards high linearity, high frequency operation and low power dissipation. Although each published transconductor structure employs design technique which reflects the distinctive thinking of the developer, common principles do exist among several different structures. This is because the operation models of MOS transistors, which are the basic devices for any MOS transconductor, are common. In this chapter, we will give a brief review of the existing MOS transconductor structures, explain the basic principles supporting various transconductor structures and illustrate the conceptual structures.

Before discussing the basic transconductor structures, it is worthwhile to have a look at the operation models of MOS transistors. MOS transistors can be biased at accumulation region, depletion region or inversion region according to the different gate-to-source voltage (v_{GS}) range. When operating in inversion region, MOS transistors present specific drain-current versus gate-voltage transfer characteristics and hence are able to implement important signal processing functions. The inversion region can be further divided into three subregions: strong inversion, moderate inversion and weak inversion [4]. Among the three subregions, the moderate inversion region appears to be the most complex region. Distributed circuit theory is often needed to model transistors operating in this region [5]. Because of the absence of proper model, moderate inversion region is rarely used for cir-

cuit design and hence will not be discussed in this review.

The widely employed MOS operation region is the strong inversion region. The models of MOS transistors in the strong inversion region are well-established. There are simple models and more accurate but complex models. Using parameters of different complexity levels, the designers are able to analytically predict the performances of their design to different degrees of accuracy. Transconductors based on strong inversion MOS transistors will be discussed in section 2.1.

The operation model of MOS transistors in weak inversion is properly defined and the complication level is moderate. Since the transistors operating in weak inversion region can only process very small voltage and current signals, their applications are limited to a few specific fields where very weak signals are expected, for example, biomedical equipments. Section 2.2 will review the transconductor structure which is based on transistors in weak inversion. Section 2.3 summarizes the review.

2.1 MOS operating in strong inversion region

The transfer characteristic, that is, I_D versus V_{GS}, for a strongly inverted MOS transistor can be expressed by one of the following two equations [6] depending on the actual operation region of the transistor.

$$I_D = (\mu C_{ox} W/2L)(v_{GS} - V_{th})^2(1 + \lambda V_{DS}) \quad ; \quad V_{GS} > V_{th} ; \; V_{DS} \geq V_{GS} - V_{th} \tag{2.1}$$

$$I_D = (\mu C_{ox} W/L)(V_{GS} - V_{th} - V_{DS}/2)V_{DS}(1 + \lambda V_{DS}) \; ; \quad V_{GS} > V_{th} \; ; \quad V_{DS} < V_{GS} - V_{th} \tag{2.2}$$

where μ is the mobility of carriers, C_{ox} is the gate capacitance per unit area, W and L are the channel width and length parameters, V_{GS}, V_{DS} represent gate-source, drain-source and substrate-source voltages respectively, V_{th} is the threshold voltage of the transistor. Assuming the channel length modulation is negligible, λ in eqns. (2.1)-(2.2) becomes zero. Equation (2.1) is usually named "square-law of MOS transistor" and the transistors

possessing this transfer property are called "saturated". Transistors whose transfer characteristic can be expressed by eqn.(2.2) are called "linearly operating" or in "triode" operation region.

2.1.1 Transconductors with input MOS transistors in saturation region

Several transconductors which use MOS operation in saturation region have been developed in the literature. Transconductors in this category have high values of the transconductance factor (g_m). With high g_m, the transconductor is able to handle large drain-current and the operating frequency of the transconductor can be high. The basic structure in this category is source-coupled differential transistor pair. The conceptual circuit is shown in Fig. 2.1[1].

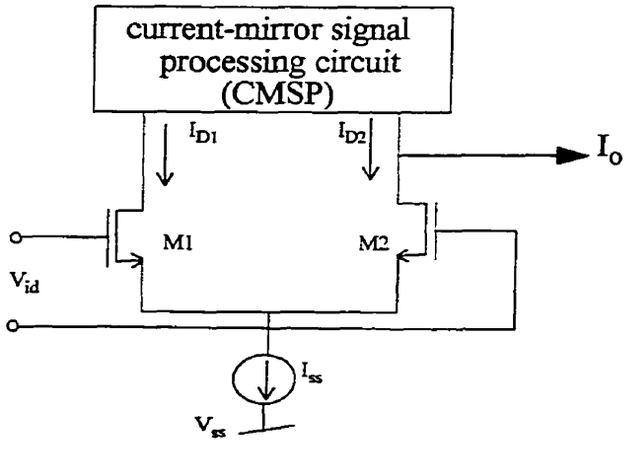


Fig. 2.1 Source Coupled differential pair transconductor

Assume M1 and M2 are perfectly matched and saturated. Using the square-law for M1 and M2, the output current of Fig. 2.1 is given by

$$I_o = I_{D1} - I_{D2} = \begin{cases} \sqrt{2I_{ss}K}V_{id}\sqrt{1-\frac{K}{2I_{ss}}V_{id}^2} & |V_{id}| \le \sqrt{\frac{I_{ss}}{K}} \\ I_{ss}sgn(V_{id}) & |V_{id}| \ge \sqrt{\frac{I_{ss}}{K}} \end{cases} \quad (2.3)$$

where $K = \frac{\mu C_{ox} W}{2 L}$. Several features of the source coupled differential pair transconductor are discussed below.

a. *Linear range.* Analysis of eqn.(2.3) reveals that to achieve less than 1% nonlinearity, V_{id} must be restricted to $|V_{id}| \leq 0.2\sqrt{I_{SS}/K}$. Defining $\sqrt{I_{SS}/K}$ as the total dynamic V_{id} range of M1 and M2 , the linear dynamic range given above is only 20% of the total dynamic range.

b. *Frequency response.* The frequency domain ($s = j\omega$, ω in radian/sec, $j = \sqrt{-1}$) transfer function of Fig. 2.1 is given by

$$\frac{I_o(s)}{V_{id}(s)} = \left.\frac{-g_m(1 - sC_{gd}/g_m)}{sR_s(C_{gs} + C_{gd}) + 1}\right|_{R_L = 0} \tag{2.4}$$

where g_m is the transconductance, R_s is the source resistance, C_{gs}, C_{gd} are parasitic capacitances from gate to source and gate to drain respectively. For modern processes, C_{gs} and C_{gd} can be very small and hence very high frequency performance can be obtained.

c. *Noise performance.* Consider only thermal noise. The equivalent input referred voltage noise is given by

$$\frac{V_{eq}^2}{\Delta f} = \frac{16}{3}\frac{kT}{g_m}\left(1 + \frac{g_{mb}}{g_m}\right)(1 + N_1) \tag{2.5}$$

where N_1 is a constant depending on the topology and the W/L ratio of the transistors in the current mirror circuit.

Although the source coupled differential pair transconductor can provide high frequency performance, its extremely small linear range prevents it from being widely used. Efforts have been put to develop transconductors possessing wider linear range as well as acceptable frequency response and noise performance. Several such linearization techniques are discussed in the following sections.

2.1.1.1 Adaptive biasing technique [7]-[9]

The principle of adaptive biasing technique is to replace the DC current source I_{ss} in Fig.

2.1 by an input dependent current source. Figure 2.2 illustrates the conceptual circuit of adaptively biased transconductor. The tail current of Fig. 2.2 consists of a DC constant current term and an extra term which is proportional to the square of input differential signal.

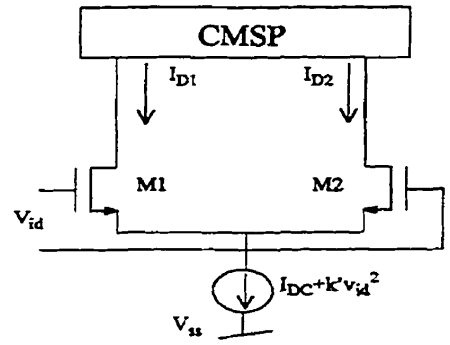


Fig. 2.2 Adaptively biased source coupled differential pair transconductor

The output current of Fig. 2.2 is given by

$$I_o = I_{D1} - I_{D2} = \begin{cases} \sqrt{2KI_{DC}}V_{id}\sqrt{1-\frac{(K-2k')}{2I_{DC}}V_{id}^2} & |V_{id}| \le \sqrt{\frac{2I_{DC}}{K}} \\ I_{DC} + k'V_{id}^2 & |V_{id}| \ge \sqrt{\frac{2I_{DC}}{K}} \end{cases} \quad (2.6)$$

When $k' = K/2$, the transconductor is perfectly linear. In addition, the linear range of each transistor is increased by a factor $\sqrt{2}$ compared to that of Fig. 2.1 with $I_{DC} = I_{ss}$. The trade-off of this technique is the degraded high frequency response.

2.1.1.2 Cross coupling technique [8],[10]

Figure 2.3 shows the cross-coupled differential pair structure.

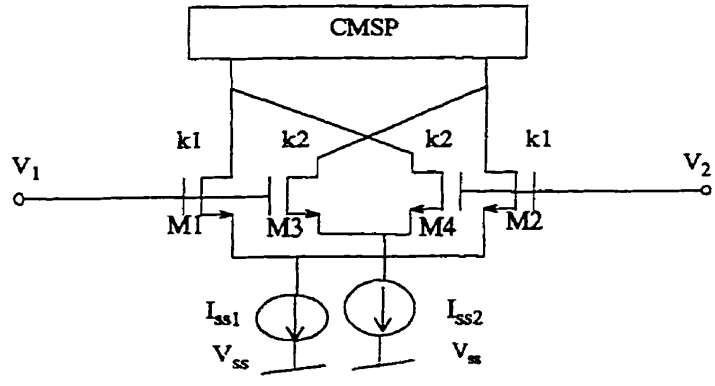


Fig. 2.3 Cross-coupled differential pair transconductor

The cross-coupled differential pair achieves higher linearity through the cancellation of the odd order nonlinear terms of the two source coupled differential pairs. Analysis shows that the odd order distortion term is proportional to $K^{3/2}/\sqrt{I_{ss}}$. The nonlinearity cancellation is accomplished by scaling the W/L ratios and tail currents of the two pairs according to

$$\left[\frac{(W/L)_1}{(W/L)_2}\right]^{3/2} = \left[\frac{I_{ss1}}{I_{ss2}}\right]^{1/2} \qquad I_{ss1} \neq I_{ss2},\ (W/L)_1 \neq (W/L)_2 \tag{2.7}$$

The linear transconductance of Fig. 2.3 is given by

$$g_m = g_{m1} - g_{m2} = \sqrt{2K_1 I_{ss1}} - \sqrt{2K_2 I_{ss2}} \tag{2.8}$$

where g_{m1} and g_{m2} are the transconductance of outer and inner transistor pair respectively. Therefore the transconductance of cross-coupled differential pair is lower than that of single differential pair. Other performances such as frequency and noise of cross-coupled differential pair are almost the same as those of single differential pair.

2.1.1.3 Class AB operation [11],[12]

The principle of class AB transconductors is based on the square law characteristic of MOS transistors. Consider the two MOS transistors in figure 2.4.

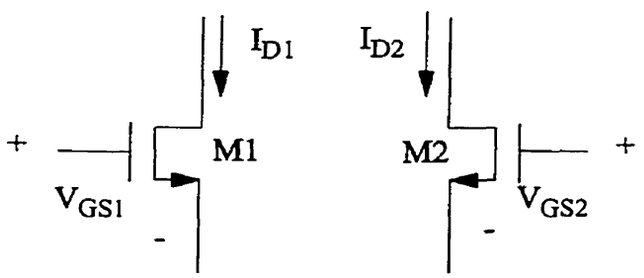


Fig. 2.4 Class-AB operation principle illustration

Assume M1 and M2 are perfectly matched and are operating in saturation region. Under

the condition of constant sum of gate-source voltages, that is, $V_{GS1} + V_{GS2} =$ constant, Fig. 2.4 possesses the following characteristics.

a. The differential drain current $I_{D1} - I_{D2}$ is linearly proportional to the difference of the gate-source voltages;

b. The sum of the drain current $I_{D1} + I_{D2}$ is quadratically related to the difference of the gate-source voltages.

For Fig. 2.4, the differential current is expressed by

$$I_o = I_{D1} - I_{D2} = 2K(V_{GS1} + V_{GS2} - 2V_{th})(V_{GS1} - V_{GS2}) \tag{2.9}$$

The sum of the gate-source voltages in eqn.(2.9) reflects the common-mode input level. In order to achieve constant common-mode level, fully-balanced differential-mode input signal is required for the transconductor. For the cases when such input drive is unavailable or difficult to obtain, the linear transfer characteristic will not be reached. The modified structure in figure 2.5 can alleviate the requirement of fully-balanced differential-mode inputs.

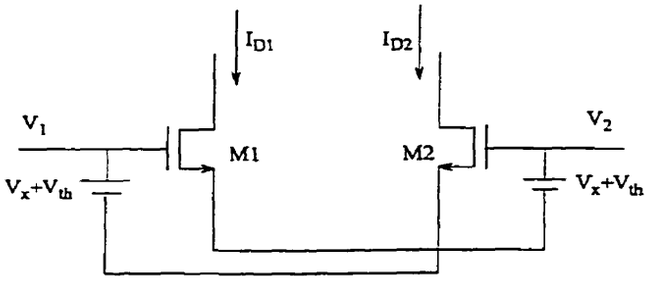


Fig. 2.5 An alternative class-AB transconductor

The output current of Fig. 2.5 is given by

$$I_{D1} - I_{D2} = 4K(V_X + V_{th})(V_1 - V_2) \tag{2.10}$$

From eqn.(2.10), one can see that the linear transconductance can be attained regardless of

whether or not the input signals are fully-balanced. In addition, the sum of the gate-source voltage is no longer relying on the common-mode signal. Consequently, the performances of the transconductor will not be affected by the common-mode input level. The transconductance of Fig. 2.5 is expressed by

$$g_m = 4K(V_X + V_{th}) \tag{2.11}$$

and can be adjusted by changing the bias voltage V_X.

2.1.1.4 Cross-coupled class-AB technique [11]-[14]

We have known that cross-coupling source-coupled differential pair transconductor will improve the linearity. Similarly, cross-coupling class-AB operating transconductor will result in enhancement of linearity. Figure 2.6 illustrates the conceptual circuit of cross-coupled class-AB transconductor.

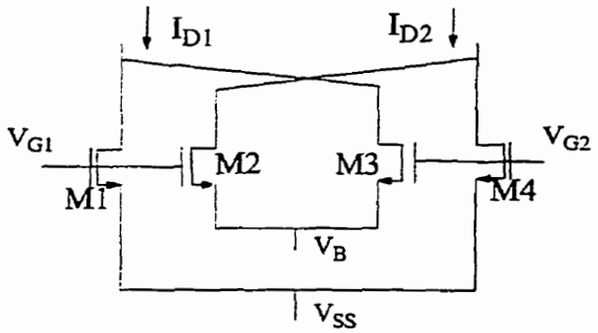


Fig. 2.6 Conceptual circuit of cross-coupled class-AB transconductor

Assume the four transistors (M1,...,M4) are perfectly matched. The output current of Fig. 2.6 is given by

$$I_{out} = I_{D1} - I_{D2} = 2K(V_B - V_{SS})V_{id} \tag{2.12}$$

where $K = \frac{uC_{ox}W}{2\ L}$ is the aspect ratio of the transistors. Cross-coupled class-AB transcon-

ductor does not rely on the common-mode input level. If negative resistive load is used, the CMRR (common-mode rejection ratio) can be very high. Another feature of cross-coupled class-AB transconductor is the easy tuning capability. Transconductance can be adjusted through changing V_B. The drawback of this technique is the low PSRR (power supply rejection ratio) because of the direct relation between transconductance and the supply voltage (V_B and V_{SS}).

2.1.1.5 CMOS double pair structures [10],[17],[18]

The MOS transistors in the aforementioned transconductor structures can be replaced by CMOS double pair (shown in Fig. 2.7).

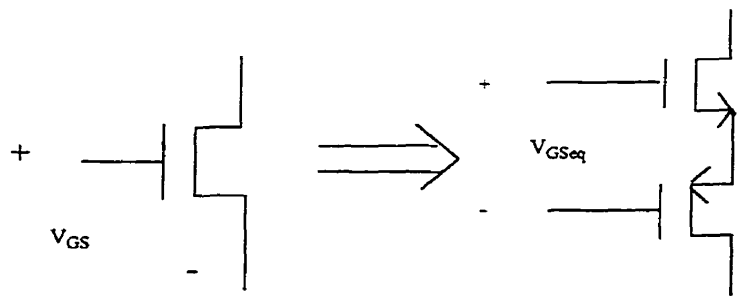


Fig. 2.7 Replace a single MOS by a CMOS double pair

The output current expression of a transconductor with MOS transistors being replaced by CMOS double pair is identical to that of its original structure. However, the K and V_{th} in the original equation should be replaced by K_{eq} and V_{theq} respectively. The K_{eq} and V_{theq} are defined by

$$K_{eq} = \frac{K_p K_n}{(\sqrt{K_p} + \sqrt{K_n})^2} \tag{2.13}$$

$$V_{theq} = |V_{thp}| + V_{thn} \tag{2.14}$$

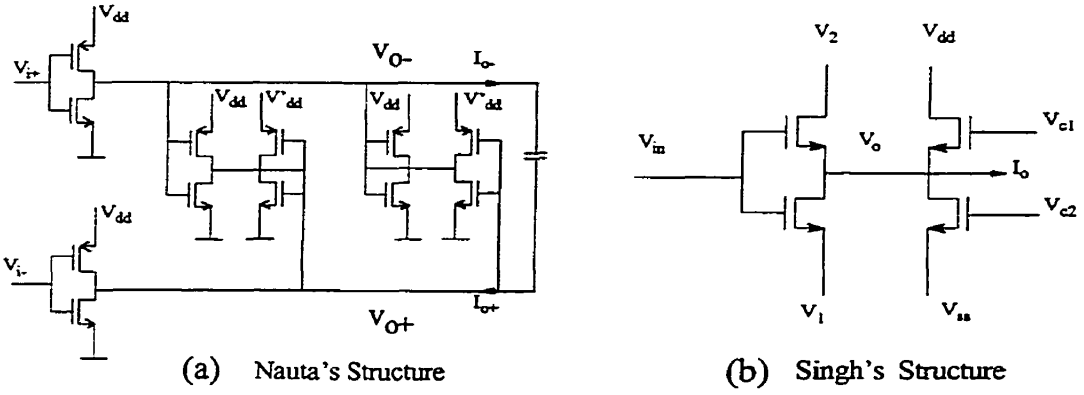
where $K_p = (uC_{ox}W/2L)|_{PMOS}$, $K_n = (uC_{ox}W/2L)|_{NMOS}$, V_{thp} and V_{thn} are the threshold voltages

of PMOS and NMOS transistors respectively.

We have mentioned that some linearization techniques (e.g., Fig.2.5) need tunable dc gate-to-source voltage. When the source terminals of the pertinent transistors are connected to the power supply, poor PSRR characteristic of that power supply will be resulted in. While replacing single channel MOS transistor by a CMOS double pair, the gate-source voltage of the original structure is replaced by the voltage between the two gate terminals of the CMOS pair. The gate-gate bias voltage adjustment of a CMOS pair will not affect its supply voltages, which are connected to the drain terminals of the input MOS transistors, any more (because of the large gate-source resistance). Therefore higher PSRR can be achieved for the CMOS pair based transconductor. The disadvantage of CMOS pair based transconductor is the reduction of input linear range due to the increase in the threshold voltage (V_{theq}).

2.1.1.6 Frequency response improvement technique [19],[20]

The principle of improving frequency performance of a transconductor is to reduce (or eliminate if possible) the internal nodes. Without any internal nodes, the frequency response of the transconductor will be determined by the capacitances at the input/output nodes and the transconductor is able to operate probably up to f_T, that is, the unity gain frequency of MOS transistors. Circuits given in Fig. 2.8 are two examples of high frequency transconductor.



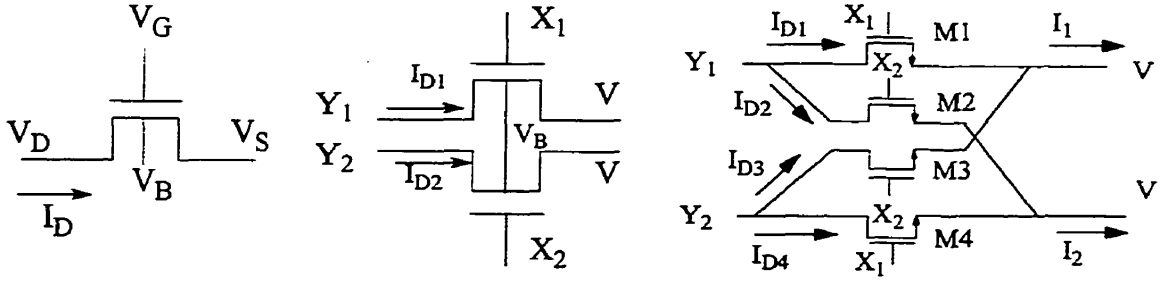
(a) Nauta's Structure (b) Singh's Structure

Fig. 2.8 High frequency transconductor structures

Fig. 2.8(a) has differential input and differential output. It is noticeable that except the two input nodes (V_{i+} and V_{i-}), all the other nodes are either connected to the output node V_{o+} or connected to V_{o-}. Fig. 2.8(b) has single input and single output. The parasitic capacitances that could affect the frequency performance are all connected with the input and output nodes. By avoiding internal nodes, both Fig. 2.8(a) and (b) achieve high frequency operation.

2.1.2 Transconductors based on input transistors in linear region

So far we have been discussing transconductors with input-MOS transistors operating in saturation region. Transconductors can also be implemented using MOS transistors operating in the linear region. The model equation was given in eqn.(2.2). Such type of transconductor has simple circuitry, easy tunability and zero quiescent power dissipation [1].



(a) triode operating MOS (b) Two-MOS structure (c) Four-MOS structure

Fig. 2.9 Transconductors based on linearly operating MOS

Consider Fig. 2.9(a). The drain current I_D of a linearly operating MOS transistor is proportional to its drain-source voltage V_{DS} (see eqn.(2.2)) and can be adjusted by the gate-source voltage V_{GS}. Using more accurate transistor model, the drain current of Fig. 2.9(a) can be related to the drain and source voltages of the transistor by

$$I_D = G(V_D - V_S) - g(V_D) + g(V_S) \tag{2.15}$$

where G is the inverse of $\mu C_{ox}(W/L)V_{GS}$, $g(\ )$ is a nonlinear function and can be further expressed by $g(x) = g_e(x) - g_o(x)$. $g_o(\ )$ and $g_e(\ )$ represents odd function and even function respectively. Fig. 2.9(a) sometimes is inserted in the source terminals of a source coupled differential pair transconductor as an active resistor to improve the linearity of the transconductor (source degeneration) [21],[22]. Fig. 2.9(b) and (c) can achieve a linear transconductor themselves if designed properly. For Fig. 2.9(b), assuming $Y_1 = -Y_2$, $X_1 = X_2$, and the two transistors are perfectly matched, the differential drain current is given by

$$I_{out} = I_{D1} - I_{D2} = (-2)\mu C_{ox}\frac{W}{L}(X_1 - V_{th})Y_1 + 2g_o(Y_1) \tag{2.16}$$

where $g_o(\ )$ is the odd part of $g(\ )$. Obviously, the even order nonlinear terms are cancelled out in this structure. For Fig. 2.9(c), assuming M1 and M2 are matched, so are M3 and M4, the differential current of Fig. 2.9(c) can be expressed by

$$I_{out} = I_1 - I_2 = \mu C_{ox}\frac{W}{L}(X_1 - X_2)(Y_1 - Y_2) \tag{2.17}$$

Fig. 2.9(c) possesses the following features:

a. Both even and odd nonlinear terms are eliminated.

b. Either X terminals or Y terminals can be used to input ac signals.

c. No fully-balanced requirement for the input ac signals.

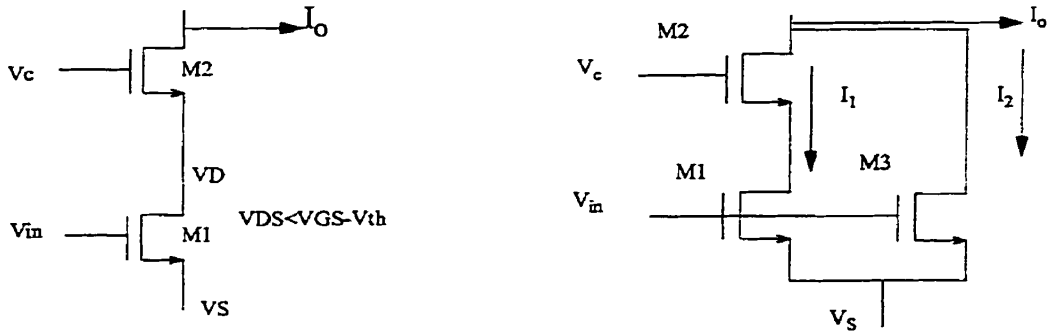
d. The transconductance can be tuned by changing the DC bias voltages on X or Y terminals.

The transconductors discussed in sections 2.1.1 and 2.1.2 are based on transistors that are operating in the same region, that is, either saturation or triode region. It is also possible to employ transistors of different operation region in a transconductor structure. Since such implemented transconductors have distinctive I-V transfer characteristic and linearity performance, it is better to consider them as a new transconductor class that is different from

those described in sections 2.1.1 and 2.1.2.

2.1.3 Transconductors based on MOS transistors operating in saturation and linear regions [23]-[25]

The conceptual structure of the transconductors which employ transistors operating in both saturated and linear regions is given in Fig. 2.10(a). It consists of two stacked transistors, M1 and M2. The upper transistor (M2) is operating in saturation region. The lower transistor(M1) is in linear region. Input signal is fed into the gate terminal of M1, therefore M1 is the dominant transistor of the structure. The transistor M2 is indispensable for the structure because it controls the drain voltage of M1 via adjusting the dc voltage at its gate terminal (i.e., V_c). By properly choosing V_c, the drain-source voltage of M1 can be limited to $V_{DS} < V_{GS1} - V_{th}$ and hence the linear operation of M1 is attained.



(a) Cascode structure (b) Coben's structure

Fig. 2.10 Conceptual circuit of transconductors with input-MOS in mixed operating regions

In addition, after inserting M2, the output node becomes the drain of M2, thus the output resistance of the transconductor can be greatly increased. Employing two identical Fig. 2.10(a) structures and using fully-balanced ac inputs to implement a transconductor, better linearity can be achieved. The structures shown in Fig. 2.10(b) can provide higher linearity than that of Fig. 2.10(a). In Fig. 2.10(b), M1-M2 branch is identical to Fig. 2.10(a), M3

is parallel with M1-M2 branch and operating in saturation region. The higher linearity results from the fact that the distortion terms of saturated and linearly-operating transistors have opposite polarity [25]. Since the output current I_o is the summation of the current of M1-M2 branch and M3 branch, the distortion of I_o will be lower than that of each single branch. Cross-coupled connection of two units as in Fig. 2.10(b) and employing fully-balanced input ac signals will result in even better linearity performance.

2.2 MOS operating in weak inversion region

The transfer characteristic of a MOS transistor in weak inversion region is given by

$$I_D = \frac{W}{L} I_{D0} e^{-V_{BS}[(V_t/n)-(1/V_t)]} (1 - e^{-V_{DS}/V_t}) e^{(V_{GS}-V_{th})/(nV_t)} \tag{2.18}$$

where I_{D0} and n are process parameters. $I_{D0} \equiv \mu C_{ox} 2(nV_t)^2/e^2$, the typical value for n is 2. $V_t = \frac{kT}{q}$ in which k is the Boltzman constant, T is the temperature in Kelvin and q is the charge quantity of an electron. V_{th} is the threshold voltage. V_{BS}, V_{DS} and V_{GS} are bulk to source, drain to source and gate to source voltage respectively. W and L are the channel width and length parameters.

Considering eqn.(2.18), one can see that the transfer characteristic of weakly inverted MOS is similar to that of a BJT transistor. Thus by replacing BJT transistors in a circuit with a weakly inverted MOS transistor, similar transfer function can be achieved. A simple structure is source coupled differential pair of Fig. 2.11.

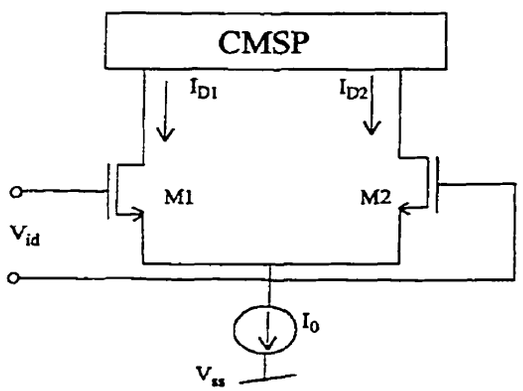


Fig. 2.11 Transconductor with weakly inverted input-MOS

Although Fig. 2.11 looks exactly the same as Fig. 2.1, the transfer characteristic of M1 and M2 are completely different for Fig. 2.1 and Fig. 2.11. The former follows eqn.(2.1) whereas the latter follows eqn.(2.18). The differential output current for Fig. 2.11 is given by [26]

$$I_{out} = I_0 \tanh \frac{V_{id}}{2nV_t} \tag{2.19}$$

where V_{id} is the differential input voltage, n and V_t are the same as those in eqn.(2.18). If V_{id} is less than $3nV_t$, I_{out} can be approximately expressed by $I_0 \frac{V_{id}}{2nV_t}$ and hence is linearly related to the differential input voltage V_{id}.

2.3 Summary

In this chapter, various linear MOS transconductor structures existing in the literature have been reviewed. The transfer characteristics of input-MOS transistors are employed as the basis of transconductor classification. The emphasis is put on the transconductors with input transistors working in strong inversion region. This is because the models of MOS transistors in this region are well-established and transconductors based on MOS transistors in strong inversion region are widely used in practical applications. As a consequence, the following chapters will focus principally on the transconductors built from MOS transistors in strong inversion.

Chapter 3

Transconductor Frequency-Power Efficiency Optimization I: Unconstrained Single variable Optimization

With the development of semiconductor technology, the component densities on a single integrated chip are increasing dramatically. Currently, the integration level has reached more than 15 million transistors per chip (Alpha 21264, 1996). Implementing a complete system on a single chip (i.e., system-on-a-chip) is no longer a dream. However, the large component count on a single chip will naturally lead to increased power dissipation of the chip. It has been found that when power dissipation is over a particular limit, portability will be a problem. This is because the power dissipation will result in heat accumulation which will either make the chip malfunction or greatly reduce the lifetime of the chip. Therefore, cooling component, which usually has big volume and heavy weight, must be attached with the chip. The effective way of employing highly integrated chips without losing the portability is either reducing the absolute power dissipation or improving the power efficiency so that better performance can be achieved for certain amount power consumption. There are two phases to accomplish the power dissipation reduction. One is to develop completely new circuit topology in which low power is the major concern, for instance, micropower systems. The other is to optimize the existing circuit topologies in terms of power dissipation. Phase one is very promising because it can effectively exploit the advanced features that the modern semiconductor technology can provide. But it usually requires longer design and test cycle before becoming a commercial product. On the opposite, optimizing the existing designs may not lead to such a good result as method one can achieve, but it has the advantages of low cost and short time-to-market. In addition, a

systematic optimization methodology can be applied to newly developed topologies as well.

What we are interested in here is the second phase: optimizing CMOS transconductors in terms of their power dissipation. The objective of the optimization is the frequency-power efficiency of CMOS transconductors. Section 3.1 introduces the criterion proposed for the optimization. Section 3.2 presents the mathematical expressions and general results of the optimization. Sections 3.3, 3.4 and 3.5 apply the optimization methodology to CMOS transconductor structures with two- , four- and eight-input MOS transistors respectively. While optimizing the transconductor structures, physical aspects are also taken into consideration. For each transconductor structure, only one of the design variables is used for optimization and no constraints are set for the optimization. Therefore the optimization is said to be unconstrained single variable optimization. Section 3.6 summarizes the conclusion.

3.1 g_{ac}/P_{diss}: frequency-power efficiency of transconductors

Optimizing CMOS transconductors with respect to a particular performance is not a new idea. Some researchers have already taken optimization into consideration when they proposed a transconductor structure[27]. However, none of the systematic CMOS transconductor optimization method discussed here has been reported in the literature.

It is known that delay-power product is a very important feature of a digital design. Minimizing delay-power-product is always a goal no matter which digital system is under consideration. Similarly, we can consider a specific performance parameter of the transconductor structure with its power dissipation and define an optimizable figure of merit. For example, one can define frequency-power ratio, linearity-power ratio and noise-power product as design criteria. Then the right direction of performance improvement will be maximizing the first two ratios and minimizing the last product. Our research is

dealing with the criterion of frequency-power ratio which describes the frequency-power-efficiency of a transconductor. The intrinsic operating bandwidth of an unloaded transconductor is determined by the ratio of its ac transconductance (g_{ac}) and the parasitic capacitances associated with the output transistors. The parasitic capacitances of a fixed size transistor depend only on the technology parameters, such as gate-drain or gate-source overlap capacitors, and hence can be taken as a constant value. Therefore, the bandwidth of a transconductor is eventually decided by its ac transconductance. So the frequency-power-ratio of a transconductor can be represented by g_{ac}/P_{diss} ratio. Assuming certain amount of power dissipation, the transconductor with high g_{ac}/P_{diss} can achieve wider bandwidth than the one with low g_{ac}/P_{diss}; alternatively, assuming certain operating bandwidth is required, the transconductor with high g_{ac}/P_{diss} will consume less power than the one with low g_{ac}/P_{diss}. Maximizing the g_{ac}/P_{diss} will result in highest frequency-power efficiency, which is a very desirable feature of a transconductor.

3.2 General view on g_{ac}/P_{diss} characteristic of CMOS transconductors

Assume the availability of a voltage or current variable (say, χ) which determines g_{ac} and P_{diss}. By adjusting χ optimally, the function $f(\chi)=g_{ac}/P_{diss}$ can be maximized. Since in a MOS transistor, the transconductance is proportional to the square root of the dc current (saturated operation) or linearly proportional to the dc current (linear operation), and the dc current is proportional to the square or higher power of voltages applied to the gate terminal (i.e., V_{GS}-V_{th}), so the transconductance will most naturally be proportional to the voltage variable (i.e., χ). Similarly, being the product of a dc voltage and a dc current, the P_{diss} will be proportional to the square or higher power of χ. Thus it is very reasonable to assume that the dependence of P_{diss} on χ will be at least one degree higher than that of g_{ac}. In other words, the degree of the numerator of $f(\chi)$ will be less than that of the denomina-

tor by one or a higher number. Let us consider a few conceptual possibilities.

Case 1. Consider that $f(\chi)= \varepsilon/(\alpha\chi+\beta)$. Such expression occurs when the g_{ac} is a linear function of the variable χ (i.e., $g_{ac} = \varepsilon\chi$) while the P_{diss} has the form of $P_{diss} = \alpha\chi^2+\beta\chi$. α, β and ε are constants. Following the routine of function maximization with respect to χ, it turns out that the extremum of $f(\chi)$ is $\pm\infty$ at $\chi = -\beta/\alpha$.

Case 2. Consider $f(\chi)= (\delta\chi+\varepsilon)/(\alpha\chi^2+\beta\chi+\gamma)$, where $\alpha, \beta, \gamma, \delta$ and ε are constants. Mathematical optimization shows that the two extremums of $f(\chi)$ are located at $\chi = \frac{-\alpha\varepsilon \pm \sqrt{(\alpha\varepsilon)^2 - \alpha\beta\delta\varepsilon + \alpha\gamma\delta^2}}{\alpha\delta}$. The χ which has the positive sign before $\sqrt{}$ symbol corresponds to the maximum $f(\chi)$. The other one leads to the minimum $f(\chi)$. If $\varepsilon = 0$, the extremums appear at $\chi = \pm\sqrt{\frac{\gamma}{\alpha}}$. When $\alpha\delta$ is positive, $\chi = \sqrt{\frac{\gamma}{\alpha}}$ will lead to the maximum of $f(\chi)$. Otherwise $\chi = -\sqrt{\frac{\gamma}{\alpha}}$ will lead to the maximum.

Case 3. Consider $f(\chi)= (\varepsilon\chi^2+\eta\chi+\lambda)/(\chi^3+\beta\chi^2+\gamma\chi+\delta)$. An example of the transconductor structure which has such g_{ac}/P_{diss} characteristic is the drain/source-biased saturated input-MOS transconductor. Detailed analysis on such structure will be given in later sections. Equating the first order derivative of $f(\chi)$ to zero, we find that the extremums of $f(\chi)$ happen at the solutions of the following equation:

$$\varepsilon\chi^4 + 2\eta\chi^3 + (3\lambda+\eta\beta-\varepsilon\gamma)\chi^2 + (2\beta\lambda-2\delta\varepsilon)\chi + (\gamma\lambda-\delta\eta) = 0 \qquad (3.1)$$

The real roots (positive or negative) of eqn.(3.1) will be acceptable solutions. $f(\chi)$ could be maximum or minimum when χ equals to one of the solutions.

The above analyses are at abstract level. Depending upon which of the three abstract cases arises during the analysis of a particular transconductor structure, its optimization result can be easily obtained by replacing the symbols in the abstract formulas with proper design variables of the transconductor.

3.3 Optimizing g_{ac}/P_{diss} for two-input-MOS transconductors

Now let us consider the linear transconductor structures, that is, the transconductors which have linear voltage-current transfer characteristic. The simplest linear CMOS transconduc-

tors are based on two-input-MOS transistors, for example, the source coupled differential pair transconductor. The input transistors can operate in strong or weak inversion regions (Chapter 2). Consequently, there can be four possible modes of operation: (i) saturated two-input-MOS transconductor; (ii) linear-operating two-input-MOS transconductor; (iii) weakly-inverted two-input-MOS transconductor and (iv) mixed-operating two-input-MOS transconductor. In this section we will optimize the g_{ac}/P_{diss} for various two-input-MOS transconductors.

3.3.1 Transconductors with gate-biased input MOS operating in saturation region

Figure 3.1 shows the network under consideration.

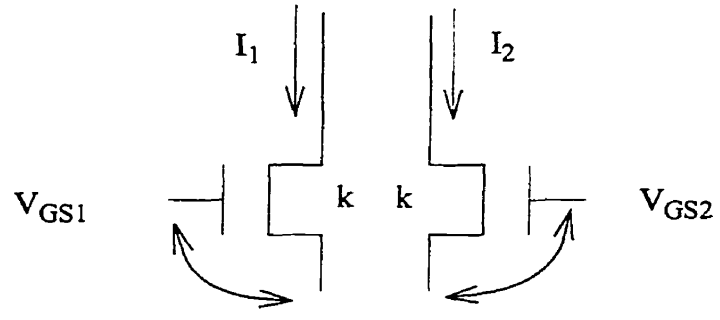


Fig. 3.1 Conceptual diagram of the transconductor

The transconductor with this configuration has the following I_{out} and P_{diss} expressions (ignoring channel length modulation):

$$I_{OUT} = I_1 - I_2 \quad = K(v_{GS1} + v_{GS2} - 2V_{th})(v_{GS1} - v_{GS2}) \tag{3.2}$$

where $K = \frac{1}{2}\mu C_{ox}(W/L)$, V_{th} is the threshold voltage, v_{GS1} and v_{GS2} are the instantaneous signals (ac plus dc), i.e.

$$v_{GS1} = V_{GS1} + v_{gs1} \qquad v_{GS2} = V_{GS2} + v_{gs2} \tag{3.3}$$

where V_{xyz} are the dc components and v_{xyz} are the ac components.

$$P_{diss} = K[(V_{GS1} - V_{th})^2 + (V_{GS2} - V_{th})^2](V_{dd} - V_{ss}) \tag{3.4}$$

where V_{dd} and V_{ss} are positive and negative power supplies respectively.

3.3.1.1 Equal input common-mode signal

Assume $V_{GS1} = V_{GS2} = V_{GS}$, $v_{gs1} = -v_{gs2} = v_{id}/2$. Using eqns.(3.2)-(3.4) we can derive

$$g_{ac} = \partial I_{out}/(\partial v_{id}) = 2K(V_{GS} - V_{th}) \tag{3.5}$$

$$P_{diss} = 2K(V_{GS} - V_{th})^2(V_{dd} - V_{ss}) \tag{3.6}$$

Therefore

$$\frac{g_{ac}}{P_{diss}} = \frac{1}{(V_{GS} - V_{th})(V_{dd} - V_{ss})} \tag{3.7}$$

Taking V_{GS} as independent variable χ, eqn.(3.7) has the same form as that of the abstract Case 1. It has been known that for a MOS transistor to work in strong inversion region, its gate-source voltage must be greater than the threshold voltage (i.e., $V_{GS} > V_{th}$). Therefore, eqn.(3.7) will monotonically decrease as V_{GS} increases. When V_{GS} approaches V_{th}, the g_{ac}/P_{diss} goes toward infinity. Although the theoretical maximum of eqn.(3.7) (i.e., infinity) is not physically reachable, it gives us an idea that for this kind of transconductor structure, higher g_{ac}/P_{diss} can be expected when V_{GS} is getting closer to V_{th}.

3.3.1.2 Unequal input common-mode signal

Now it is assumed that $V_{GS1} \neq V_{GS2}$ and $v_{gs1} = -v_{gs2} = v_{id}/2$. The ac transconductance and dc power dissipation are found to be

$$g_{ac} = \frac{\partial I_{out}}{\partial v_{id}} = K[(V_{GS1} - V_{th}) + (V_{GS2} - V_{th})] \tag{3.8}$$

and

$$P_{diss} = K[(V_{GS1} - V_{th})^2 + (V_{GS2} - V_{th})^2](V_{dd} - V_{ss}) \tag{3.9}$$

The g_{ac}/P_{diss} is obtained as

$$\frac{g_{ac}}{P_{diss}} = \frac{V_{GS1} + V_{GS2} - 2V_{th}}{[(V_{GS1} - V_{th})^2 + (V_{GS2} - V_{th})^2](V_{dd} - V_{ss})} \tag{3.10}$$

In eqn.(3.10), either V_{GS1} or V_{GS2} can be used as the independent variable for g_{ac}/P_{diss} optimization while the rest of the voltages are assumed to be constants. Comparing eqn.(3.10) with the expression of general Case 2 in section 3.2, the similarity is obvious. Replacing the symbols in the optimization result of general Case 2 by proper voltages of eqn.(3.10) and assuming V_{GS1} and V_{GS2} are independent, the optimal $V_{GS1,2}$ can be determined from eqns.(3.11) and (3.12).

$$V_{GS1|opt} = -(V_{GS2} - 2V_{th}) + \sqrt{2}(V_{GS2} - V_{th}) \tag{3.11}$$

or $$V_{GS2|opt} = -(V_{GS1} - 2V_{th}) + \sqrt{2}(V_{GS1} - V_{th}) \tag{3.12}$$

If V_{GS1} and V_{GS2} are related to another control voltage V_C by $V_{GS1} = \alpha_1 V_C$, $V_{GS2} = \alpha_2 V_C$, eqn.(3.10) can be re-written as

$$\frac{g_{ac}}{P_{diss}} = \frac{(\alpha_1 + \alpha_2)V_c - 2V_{th}}{[(\alpha_1 V_c - V_{th})^2 + (\alpha_2 V_c - V_{th})^2](V_{dd} - V_{ss})} \tag{3.13}$$

Eqn.(3.13) can also be optimized according to general case 2 and the optimal V_C can be expressed by

$$V_{c|opt} = \frac{2V_{th}}{\alpha_1 + \alpha_2} + \sqrt{\left(\frac{2V_{th}}{\alpha_1 + \alpha_2}\right)^2 - \frac{2V_{th}^2}{(\alpha_1^2 + \alpha_2^2)}} \tag{3.14}$$

The above case, i.e., $V_{GS1}/V_{GS2} = \alpha_1/\alpha_2$, arises when V_{GS1} and V_{GS2} are obtained from a potential division network over which the total potential is V_C . Quite often, in a MOS voltage division network, V_C is generated by a bias current I_{bias} in a biasing MOS transistor, that is, $V_C = \sqrt{I_{bias}/K'} + V_{th}$, where K' is the aspect ratio of the pertinent transistor. Under such circumstance, the g_{ac}/P_{diss} optimization can be carried out with respect to $\sqrt{I_{bias}}$. The optimal I_{bias} can be expressed by

$$I_{bias|opt} = K(V_{c|opt} - V_{th})^2 \tag{3.15}$$

where $V_{c|opt}$ is given in eqn.(3.14).

Considering the feasibility of the optimal results, the optimal $V_{GS1,2}$ and V_c obtained from above equations must satisfy the requirement of $V_{GS} > V_{th}$. When the optimization is done with respect to I_{bias}, only positive $I_{bias|opt}$ is acceptable. Transconductors with two-input-MOS transistors and having unequal input common-mode signals have not been studied extensively in the open literature. This is mainly due to the poor linearity characteristic of such kind of structure. This will be discussed in more details in Chapter 5.

3.3.2 Transconductors with Drain/Source-biased input MOS operating in saturation region

The control voltage of a saturated-operating transconductor can also be applied to the drain or source terminal of a MOS transistor. While biased at drain/source terminal, the instantaneous voltages (dc plus ac) on the gate terminals are fixed. The tuning of the transconductor's performances will be achieved by adjusting the drain/source biases. The conceptual diagrams of PMOS and NMOS structures are shown in Fig. 3.2(a) and (b). For PMOS structure, V_{d1} and V_{d2} are the source bias voltages; for NMOS structure, V_{s1} and V_{s2} are the source bias voltages.

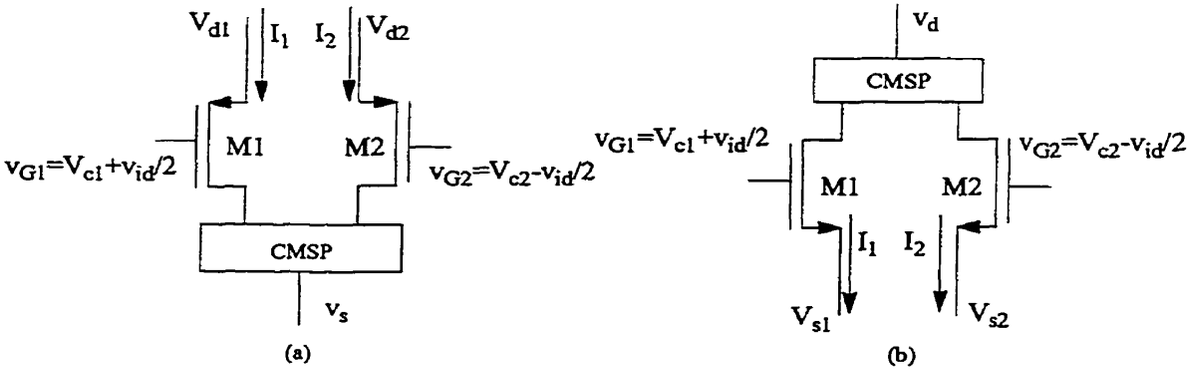


Fig. 3.2 Drain/Source-biased saturated-operating transconductor

Applying the square-law model to M1 and M2 and assuming M1 and M2 are perfectly matched, the g_{ac}/P_{diss} of Fig. 3.2(a) and (b) can be expressed by eqn.(3.16) and (3.17)

respectively.

$$\frac{g_{ac}}{P_{diss}} = \frac{\chi + 2V_{d2} - V_{c1} - V_{c2} - 2V_{th}}{b_0\chi^3 - b_1\chi^2 + b_2\chi + b_3} \tag{3.16}$$

for PMOS structure and

$$\frac{g_{ac}}{P_{diss}} = \frac{-(\chi + 2V_{s2} - V_{c1} - V_{c2}) - 2V_{th}}{b_{n0}\chi^3 + b_{n1}\chi^2 + b_{n2}\chi + b_{n3}} \tag{3.17}$$

for NMOS structure.

In eqn.(3.16),

$$V_{d1} - V_{d2} = \chi \tag{3.18}$$

$$b_0 = 1 \tag{3.19}$$

$$b_1 = 2(V_{d2} - V_{c1} - V_{th}) + (V_{d2} - V_s) \tag{3.20}$$

$$b_2 = (V_{d2} - V_{c1} - V_{th})^2 + 2(V_{d2} - V_{c1} - V_{th})(V_{d2} - V_s) \tag{3.21}$$

$$b_3 = (V_{d2} - V_{c1} - V_{th})^2(V_{d2} - V_s) + (V_{d2} - V_{c2} - V_{th})^2(V_{d2} - V_s) \tag{3.22}$$

The χ of eqn.(3.17) is defined as $V_{s1} - V_{s2}$. The $b_{n0,1,2,3}$ of eqn.(3.17) are similar to eqns.(3.19)-(3.22) with $V_{d2} - V_{c1}$, $V_{d2} - V_{c2}$ and $V_{d2} - V_s$ being replaced by $-(V_{s2} - V_{c1})$, $-(V_{s2} - V_{c2})$ and $V_d - V_{s2}$ respectively. In the following, we will show the optimization procedures for PMOS structure . NMOS structure can be optimized similarly.

The g_{ac}/P_{diss} of PMOS source-biased transconductor (i.e., eqn.(3.16)) has the same form as that of abstract case 3 with $\varepsilon = 0$. Replacing the symbols in eqn.(3.1) by proper voltages in eqn.(3.16), the following equation can be derived.

$$\chi^3 + \frac{(b_1 + 3C)}{2}\chi^2 + b_1 C\chi + \frac{(b_2 C - b_1)}{2} = 0 \tag{3.23}$$

where

$$C = 2V_{d2} - V_{c1} - V_{c2} - 2V_{th} \tag{3.24}$$

For the PMOS source-biased transconductor to operate properly, the inequalities of

$$V_{d1} - V_{c1} - V_{th} > 0 \ , \ V_{d2} - V_{c2} - V_{th} > 0 \tag{3.25}$$

must be satisfied. The solution of eqn.(3.23) which meets the requirement of (3.25) will be the acceptable optimization result.

3.3.3 Mixed saturated-triode-operating input-MOS transconductor

We have explained the operating principle of mixed input-MOS transconductor structure in Chapter 2. Here we will study its g_{ac}/P_{diss} ratio and find out the biasing condition which can lead to highest g_{ac}/P_{diss} ratio. Figure 3.3(a) and (b) are the conceptual structures of mixed input-MOS transconductors. The drain current I_{out} can be mirrored out by employing a current mirror as the active load of the structures.

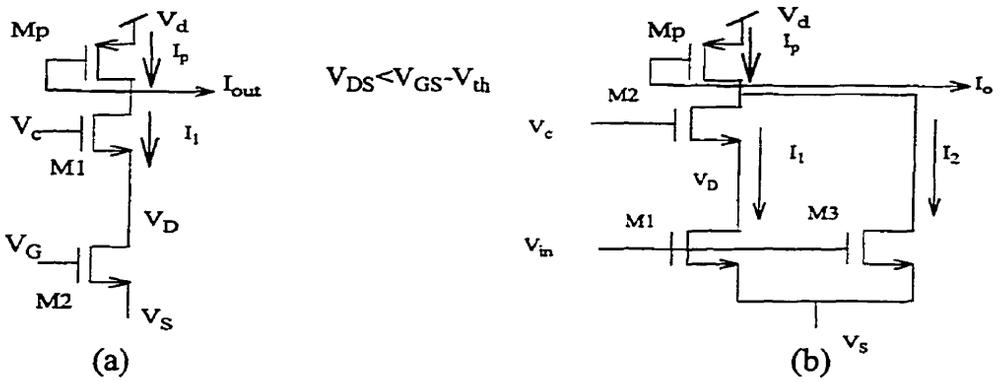


Fig. 3.3 Mixed saturated-triode-operating transconductor

Since the cascoded transistor M1 is mainly used to ensure linear operation of M2, the branch current (i.e., I_{out}) is determined by the voltage-current transfer characteristic of M2. Using the linear operation model for M2, the ac transconductance and dc power dissipation of Fig. 3.3(a) are obtained as

$$g_{ac} = 2KV_{DS} \tag{3.26}$$

$$P_{diss} = 2K\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right](V_{dd} - V_{ss}) \tag{3.27}$$

where V_{GS} and V_{DS} are the gate-source and drain-source voltage of transistor M2 respectively. According to eqns.(3.26) and (3.27), the g_{ac}/P_{diss} ratio is obtained as

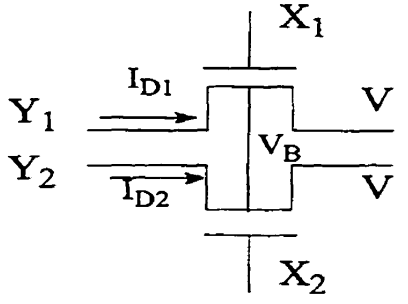
$$\frac{g_{ac}}{P_{diss}} = \frac{1}{[(V_{GS}-V_{th})-V_{DS}/2](V_{dd}-V_{ss})} \tag{3.28}$$

Consider optimizing eqn.(3.28) with respect to V_{DS}. Theoretically, when $V_{DS} = 2(V_{GS}-V_{th})$, g_{ac}/P_{diss} will be infinity. However, for M2 to remain in linear operation, it must have $0 < V_{DS} < V_{GS}-V_{th}$. With this restriction, g_{ac}/P_{diss} becomes a monotonically increasing function of V_{DS}. Moving V_{DS} towards $V_{GS}-V_{th}$ will lead to higher g_{ac}/P_{diss}.

Because Fig.3.3 (b) needs to be paired to implement a linear transconductor, its optimization will be discussed in the four input-MOS section.

3.3.4 Linearly-operating input-MOS transconductors

In section 2.1.2, a linear transconductor structure consisting of two input MOS transistors operating in linear region (Fig. 2.9(b)) were studied. The structure is re-drawn as follows.



The output current of such transconductor was given by eqn.(2.16) and is repeated below.

$$I_{out} = I_{D1} - I_{D2} = (-2)\mu C_{ox}\frac{W}{L}(X_1 - V_{th})Y_1 + 2g_o(Y_1) \tag{3.29}$$

at the condition $Y_1 = -Y_2$ and $X_1 = X_2$.

The dc power dissipation of this transconductor structure is given by

$$P_{diss} = uC_{ox}(W/L)[Y_1^2 - V^2 + 2V(X_1 - V_{th})] \tag{3.30}$$

Because the bias voltage can be input into either gate (X_1) or the drain/source (Y_1) terminal, the g_{ac}/P_{diss} can be optimized with respect to X_1 or Y_1 depending on where the bias voltage is fed.

3.3.4.1 Drain/source-biased

Assume ac input signals are fed into Y terminals of the transconductor, i.e., $Y_1 = V_{dc} + v$ and X_1 is fixed . Neglecting the odd order nonlinear term $g_o(Y_1)$ in eqn.(3.29), we obtained

$$g_{ac} = K(X_1 - V_{tn}) \tag{3.31}$$

The g_{ac}/P_{diss} optimization reveals that when

$$V_{dc} = \sqrt{V^2 - 2V(X_1 - V_{th})} \quad \text{and} \quad V > 2(X_1 - V_{th}) \tag{3.32}$$

g_{ac}/P_{diss} is maximized. However, physical restrictions for the transconductor to operate properly require $V < X_1 - V_{th}$ and $V < V_{dc} < X_1 - V_{th}$. Therefore, the optimization result of eqn.(3.32) is not feasible. Under the circumstance of $V < X_1 - V_{th}$, smaller V_{dc} will lead to higher g_{ac}/P_{diss}.

3.3.4.2 Gate-biased

Assuming the input signals are fed into X_1 terminals, that is, $X_1 = V_{dc} + v$, and neglecting third and higher order nonlinear terms $g_o(Y_1)$ in eqn.(3.29), we get

$$g_{ac} = KY_1 \tag{3.33}$$

The maximal g_{ac}/P_{diss} is found at

$$V_{dc} = \sqrt{2V(X_1 - V_{th})} \tag{3.34}$$

The feasibility of eqn.(3.34) must be examined by the inequalities of (3.35).

$$V_{dc} - V_t > max(Y_1, -Y_1)\ ,\ V < min(Y_1, -Y_1) \tag{3.35}$$

3.3.5 Weakly-inverted input-MOS Transconductor

According to eqn.(2.19), for $|V_{id}| < 3nV_t$, linear transconductance can be achieved by weakly-inverted two-input-MOS transconductor structure. The ac transconductance is expressed by $g_{ac} = I_0/(2nV_t)$. The power dissipation of weakly-inverted two-input-MOS transconductor has the expression of $P_{diss} = I_0(V_{dd} - V_{ss})$. Thus, the g_{ac}/P_{diss} of this transconductor structure is a constant and hence can not be optimized.

3.4 Optimizing g_{ac}/P_{diss} for four input-MOS transconductors

Two-input-MOS transconductors have very simple architectures but usually suffer from very small linear range. Many circuit design techniques which can be used to improve the linearity of the basic two-input-MOS transconductors were discussed in Chapter 2. One of the effective methods for improving linearity is cross-coupled connection of a pair of two-input-MOS transconductors. This technique leads to four-input-MOS transconductors, which can provide better linearity as well as simple circuit architecture. Four-input-MOS transconductors are widely used in literature.

3.4.1 Transconductors with input MOS operating in saturation region

When operating in saturation region, MOS transistors can carry large current (in the range of tens of uA). Many linear transconductor structures are implemented using saturated-operating input-MOS transistors to achieve higher output current. Fig. 3.4 shows the conceptual circuit of a saturated-operating gate-biased four-input-MOS transconductor. The term "gate-biased" refers to that the adjustable bias voltages are fed into the gate terminals of the input transistors.

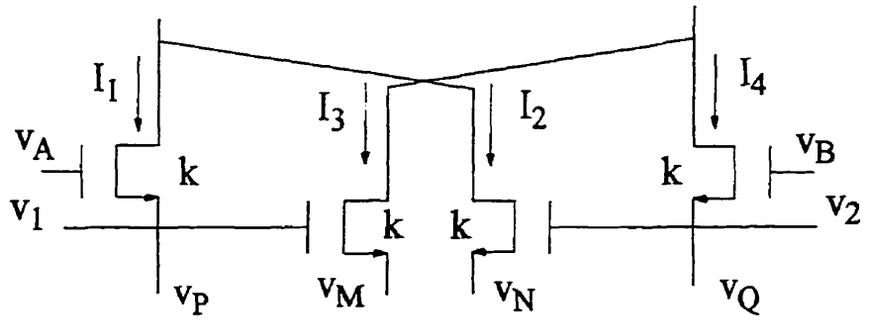


Fig. 3.4 Conceptual diagram of Four-input-MOS transconductor

Ignoring channel length modulation, we can write:

$$I_1 = K(v_A - v_P - V_{th})^2 \ , \ I_2 = K(v_2 - v_N - V_{th})^2 \ , \ I_3 = K(v_1 - v_M - V_{th})^2 \ , \ I_4 = K(v_B - v_Q - V_{th})^2 \quad (3.36)$$

The output differential current I_{out} and the power dissipation P_{diss} are expressed as

$$I_{out} = (I_1 + I_2) - (I_3 + I_4) = (I_1 - I_4) + (I_2 - I_3)$$

$$= K(v_A + v_B - v_P - v_Q - 2V_{th})(v_A - v_B + v_Q - v_P) + K(v_2 + v_1 - v_M - v_N - 2V_{th})(v_2 - v_1 + v_M - v_N) \quad (3.37)$$

$$P_{diss} = (I_1 + I_2 + I_3 + I_4)(V_{dd} - V_{ss}) \quad (3.38)$$

Let $v_{GS1}=v_A-v_P$, $v_{GS2}=v_B-v_Q$, $v_{GS3}=v_1-v_M$, $v_{GS4}=v_2-v_N$, eqn.(3.37) can be re-written as

$$I_{out} = K(v_{GS1} + v_{GS2} - 2V_{th})(v_{GS1} - v_{GS2}) + K(v_{GS3} + v_{GS4} - 2V_{th})(v_{GS4} - v_{GS3}) \quad (3.39)$$

In order for the transconductor to have linear ac transconductance, $v_{GS1} - v_{GS2}$, $v_{GS3} - v_{GS4}$ should be linearly related to the differential ac signal v_{id} . This can be achieved, for example, by setting

$$v_{GS1} = V_{GS1} \pm v_{id}/2 \quad (3.40)$$

$$v_{GS2} = V_{GS2} \mp v_{id}/2 \quad (3.41)$$

$$v_{GS3} = V_{GS3} \pm v_{id}/2 \quad (3.42)$$

$$v_{GS4} = V_{GS4} \mp v_{id}/2 \tag{3.43}$$

In the above, V_{GS1}, V_{GS2}, V_{GS3} and V_{GS4} are adjustable dc bias voltages. By properly choosing the dc bias voltages and the phases of ac signals, transconductors governed by different g_{ac} expressions can be realized. Considering all the possible conditions, there emerges eighteen different ac input phase combinations in total. These eighteen phase combinations can be grouped to nine sets in terms of their similarity of g_{ac}/P_{diss} expressions. Table 3.1 lists the phase sets concerned.

Table 3.1 Polarity of ac component $v_{id}/2$

Phase set	*phasing No.*	v_{gs1}	v_{gs2}	v_{gs3}	v_{gs4}
1	*1 & 2*	+	-	+	-
		-	+	-	+
2	*3 & 4*	+	-	-	+
		-	+	+	-
3	*5 & 6*	+	+	+	-
		-	-	-	+
4	*7 & 8*	+	+	-	+
		-	-	+	-
5	*9 & 10*	+	-	+	+
		-	+	-	-
6	*11 & 12*	+	-	-	-
		-	+	+	+
7	*13 & 14*	+	+	-	-
		-	-	+	+
8	*15 & 16*	+	-	*0*	*0*
		-	+	*0*	*0*
9	*17 & 18*	*0*	*0*	+	-
		0	*0*	-	+

The dc biases within each of the two transistor pairs (M1,M2),(M3,M4) can be balanced or unbalanced. The g_{ac}/P_{diss} expressions and the corresponding optimization results will be different for balance-biased and unbalance-biased cases. Both cases are discussed in the

following sections.

3.4.1.1 By pair balanced input common-mode signal

In this case, we assume $V_{GS1} = V_{GS2} = V_c$, $V_{GS3} = V_{GS4} = V_b$. Four different expressions are possible for I_{out}. They are

$$I_{out} = \pm 2K(V_c - V_b)v_{id} \tag{3.44}$$

$$\text{or} \quad I_{out} = \pm 2K(V_c + V_b - 2V_{th})v_{id} \tag{3.45}$$

$$\text{or} \quad I_{out} = \pm 2K(V_b - V_{th})v_{id} \tag{3.46}$$

$$\text{or} \quad I_{out} = \pm 2K(V_c - V_{th})v_{id} \tag{3.47}$$

Eqn.(3.44) holds for phase set 1 in Table 3.1. Eqn.(3.45) holds for phase set 2, eqn.(3.46) holds for phase sets 3,4 and 9 while eqn.(3.47) holds for phase sets 5,6 and 8. Obviously, phase set 1 is ideal if dependence of I_{out} on V_{th} of the transistors is undesirable.
The dc power dissipation expressions for all cases are the same and is given by

$$P_{diss} = 2K[(V_c - V_{th})^2 + (V_b - V_{th})^2](V_{dd} - V_{ss}) \tag{3.48}$$

where $K = \frac{1}{2}\mu C_{ox}(W/L)$ for the corresponding MOS transistor.
The two voltage variables, V_c and V_b , can be independently controlled or be dependent on each other through another voltage V_r by $V_c = \alpha_1 V_r$, $V_b = \alpha_2 V_r$. The optimization results for independent (V_c, V_b) and dependent (V_c, V_b) cases are provided in Table 3.2 (a). Because a bias voltage can be generated by passing a bias current through a diode-connected MOS transistor, the g_{ac}/P_{diss} of a transconductor can also be optimized with respect to the bias current I_{bias}. The relation between the bias voltage and the bias current is $I_{bias} = K'(V_{bias} - V_{th})^2$, where K' is the aspect ratio of the diode-connected transistor. The optimal bias current of each phase set which will lead to optimal g_{ac}/P_{diss} is also given in Table 3.2. For some transconductor structures [25]-[27], the total current of the circuit

needs to be held as a constant, that is, $\sum I = I_{ss}$. In such case, the P_{diss} can be expressed by $(I_{ss} + nI_b)(V_{dd} - V_{ss})$, where I_b is the bias current which generates the necessary bias voltage and n is a constant representing the number of biasing nodes needed in the transconductor. Taking I_b as the optimizable variable, the optimal I_b is decided by n, I_{ss} and the aspect ratio K of the bias transistor. Table 3.2(b) lists the optimization results of I_b for all the phase sets as well. Since phase set 7 works as a linear transconductor only when input common-mode signals are unbalanced, the analyses conducted and the results obtained in this section are not applicable to it. The optimization on phase set 7 will be discussed in the following section.

Table 3.2 (a) Optimum dc bias voltage expressions for balance-biased four-input-MOS transconductors

Phase set	Optimum control voltage	Optimum control current
1 & 2	Independent Case $V_{c\|opt} = V_b + \sqrt{2}(V_b - V_{th})$ if $V_{c\|opt} < V_{th} + 1$ or $V_{c\|opt} = V_{th}$ if $V_{c\|opt} > V_{th} + 1$ $V_{b\|opt} = V_c + \sqrt{2}(V_c - V_{th})$ if $V_{b\|opt} > V_{th} + 1$ or $V_{c\|opt} = V_{th}$ if $V_{b\|opt} < V_{th} + 1$	Dependent Case $V_{ropt} = \sqrt{\frac{2}{\alpha_1^2 + \alpha_2^2}} V_{th}$
3&4	Independent Case $V_{c\|opt} = -(V_b - 2V_{th}) + \sqrt{2}(V_b - V_{th})$ $V_{b\|opt} = -(V_c - 2V_{th}) + \sqrt{2}(V_c - V_{th})$	Dependent Case $V_{ropt} = \frac{2V_{th}}{\alpha_1 + \alpha_2}\left(1 + \sqrt{1 - \frac{(\alpha_1 + \alpha_2)^2}{2(\alpha_1^2 + \alpha_2^2)}}\right)$
5-8,17,18 & 9-12,15,16	Independent Case (5-8,17,18) $V_{b\|opt} = V_c \quad V_{c\|opt} = V_{th}$ Independent Case (9-12,15,16) $V_{c\|opt} = V_b \quad V_{b\|opt} = V_{th}$	Dependent Case (5-8,17,18) $V_{ropt} = \frac{V_{th}}{\alpha_2}\left(1 + \sqrt{1 - \frac{2\alpha_1\alpha_2}{(\alpha_1^2 + \alpha_2^2)}}\right)$ Dependent Case (9-12,15,16) $V_{ropt} = \frac{V_{th}}{\alpha_1}\left(1 + \sqrt{1 - \frac{2\alpha_1\alpha_2}{(\alpha_1^2 + \alpha_2^2)}}\right)$

Table 3.2 (b) Optimum dc bias current expressions for balance-biased four-input-MOS transconductors

Phase set	Optimum control current	Optimum control current
1 & 2	Independent Case $\sqrt{I_{b\|opt}} = K(V_{c\|opt} - V_{th})$ $\sqrt{I_{b\|opt}} = K(V_{b\|opt} - V_{th})$	Dependent Case $\sqrt{I_{r\|opt}} = K(V_{ropt} - V_{th})$ I_{ss} being constant: $\sqrt{I_{r\|opt}} = \frac{V_{th}}{\sqrt{K}} + \sqrt{\frac{V_{th}^2}{K} + \frac{I_{ss}}{n}}$
3 & 4	Independent Case $\sqrt{I_{b\|opt}} = K(V_{c\|opt} - V_{th})$ $\sqrt{I_{b\|opt}} = K(V_{b\|opt} - V_{th})$	Dependent Case $\sqrt{I_{r\|opt}} = K(V_{ropt} - V_{th})$ I_{ss} being constant: $\sqrt{I_{r\|opt}} = \frac{(\alpha_1 - \alpha_2)V_{th}}{(\alpha_1 + \alpha_2)\sqrt{K}} + \sqrt{\frac{(\alpha_1 - \alpha_2)^2 V_{th}^2}{(\alpha_1 + \alpha_2)^2 K} + \frac{I_{ss}}{n}}$
5-8,17,18 & 9-12,15,16	Dependent Case $\sqrt{I_{b\|opt}} = K(V_{b\|opt} - V_{th})$ $\sqrt{I_{b\|opt}} = K(V_{c\|opt} - V_{th})$	Dependent Case $\sqrt{I_{r\|opt}} = K(V_{ropt} - V_{th})$ I_{ss} being constant: For phases 5-8,17,18 $\sqrt{I_{r\|opt}} = \sqrt{\frac{I_{ss}}{n}}$ For phases 9-12,15,16 $\sqrt{I_{r\|opt}} = \frac{(\alpha_1 - \alpha_2)V_{th}}{(\alpha_1 + \alpha_2)\sqrt{K}} + \sqrt{\frac{(\alpha_1 - \alpha_2)^2 V_{th}^2}{(\alpha_1 + \alpha_2)^2 K} + \frac{I_{ss}}{n}}$

Assuming V_b is a constant, when $V_c = V_{copt}$ the optimal g_{ac}/P_{diss} of the four phase set groups in Table 3.2 are obtained and shown below.

$$\left(\frac{g_{ac}}{P_{diss}}\right)_{1,2} = \frac{\sqrt{2}}{(4+2\sqrt{2})(V_b - V_{th})(V_{dd} - V_{ss})} \tag{3.49}$$

when $V_c > V_b$;

or $$\left(\frac{g_{ac}}{P_{diss}}\right)_{1,2} = \frac{1}{(V_b - V_{th})(V_{dd} - V_{ss})} \tag{3.50}$$

when $V_c<V_b$.

$$\left(\frac{g_{ac}}{P_{diss}}\right)_{3,4} = \frac{\sqrt{2}}{(4-2\sqrt{2})(V_b-V_{th})(V_{dd}-V_{ss})} \tag{3.51}$$

$$\left(\frac{g_{ac}}{P_{diss}}\right)_{5-8,17,18} = \frac{1}{(V_b-V_{th})(V_{dd}-V_{ss})} \tag{3.52}$$

$$\left(\frac{g_{ac}}{P_{diss}}\right)_{9-12,15,16} = \frac{1}{2(V_b-V_{th})(V_{dd}-V_{ss})} \tag{3.53}$$

Comparing eqns.(3.49) to (3.53), we find: *If all phase groups have the same value of* V_b,

$$\max(g_{ac}/P_{diss})_{9\text{-}12,15,16} < \max(\text{abs}\,(g_{ac}/P_{diss}))_{1\&2,5\text{-}8,17,18} < \max(g_{ac}/P_{diss})_{3\&4}$$

when $V_c<V_b$ or

$$\max(g_{ac}/P_{diss})_{1\&2} < \max(g_{ac}/P_{diss})_{9\text{-}12,15,16} < \max(g_{ac}/P_{diss})_{5\text{-}8,17,18} < \max(g_{ac}/P_{diss})_{3\&4}$$

when $V_c>V_b$.

Therefore *the four-input-MOS by-pair balanced common-mode-signal transconductor structure with ac inputs satisfying phase 3 or 4 will give the highest optimal* g_{ac}/P_{diss}.

3.4.1.2 By pair unbalanced input common-mode signal

Assume each transistor pair in Fig. 3.1 is unbalance-biased, that is, $V_{GS1} \neq V_{GS2}$, $V_{GS3} \neq V_{GS4}$. The output current which was defined in eqn.(3.40) needs to be modified for each ac phase set in Table 3.1. To ensure linear ac transconductance, additional conditions of the bias voltages are needed for some phase sets. In general, the output current will consist of a term which is linearly dependent upon the input differential signal plus a term which is not dependent upon the input signal (i.e., dc offset). The g_{ac}/P_{diss} optimization of unbalance-biased four-input-MOS transconductors can be carried out with respect to any one of the four bias voltages V_{GS1}, V_{GS2}, V_{GS3} and V_{GS4}. To obtain a flavor of the scenario, the analysis on phase 1 is given below.

Assume $V_{GS1}-V_{GS2} = V_{GS3}-V_{GS4} = V_{diff}$ for phasing 1. The g_{ac}/P_{diss} has the expression of

$$\frac{g_{ac}}{P_{diss}} = \frac{2V_{GS1}-2V_{GS3}}{[(V_{GS1}-V_{diff}-V_{th})^2+(V_{GS1}-V_{th})^2+(V_{GS3}-V_{diff}-V_{th})^2+(V_{GS3}-V_{th})^2](V_{dd}-V_{ss})} \tag{3.54}$$

V_{GS1}, V_{GS3} are independent

Taking V_{GS1} as the independent variable and other DC voltages as constants, eqn.(3.54) can be optimized with respect to V_{GS1} and the result is

$$V_{GS1|opt} = V_{GS3} + \sqrt{(V_{GS3} - V_{th})^2 + (V_{GS3} - V_{th} - V_{diff})^2} \tag{3.55}$$

If V_{GS3} is chosen as the independent variable for the optimization, the result is

$$V_{GS3|opt} = V_{GS1} + \sqrt{(V_{GS1} - V_{th})^2 + (V_{GS1} - V_{th} - V_{diff})^2} \tag{3.56}$$

Optimization can also be done with respect to $V_{diff} = V_{GS1} - V_{GS2} = V_{GS3} - V_{GS4}$ and the result is

$$V_{diff|opt} = \frac{V_{GS1} + V_{GS3} - 2V_{th}}{2} \tag{3.57}$$

V_{GS1}, V_{GS3} are dependent

Assume V_{GS1} and V_{GS3} are both linearly dependent on another DC voltage V_r . V_{GS1} to V_{GS4} are then expressed as

$$V_{GS1} = \alpha_1 V_r, \quad V_{GS2} = \alpha_1 V_r - V_{diff}, \quad V_{GS3} = \alpha_2 V_r, \quad V_{GS4} = \alpha_2 V_r - V_{diff} \tag{3.58}$$

where $\alpha_1 \neq \alpha_2$. Substituting eqn.(3.58) into eqn.(3.54) , we have got

$$\frac{g_{ac}}{P_{diss}} = \frac{2(\alpha_1 - \alpha_2)V_r}{[(\alpha_1 V_r - V_{diff} - V_{th})^2 + (\alpha_1 V_r - V_{th})^2 + (\alpha_2 V_r - V_{diff} - V_{th})^2 + (\alpha_2 V_r - V_{th})^2](V_{dd} - V_{ss})} \tag{3.59}$$

There are two dc control voltages :V_r and V_{diff} in eqn.(3.59). Their optimal values are given by eqns.(3.60) and (3.61) respectively.

$$V_{r|opt} = \sqrt{\frac{V_{th}^2 + (V_{diff} + V_{th})^2}{\alpha_1^2 + \alpha_2^2}} \tag{3.60}$$

$$V_{diff|opt} = \frac{(\alpha_1 + \alpha_2)V_r}{2} - V_{th} \tag{3.61}$$

Similar analyses can be applied to other phase sets. Taking one of the four bias voltages as the independent variable at a time, the formulas of optimal V_{GS1} to V_{GS4} can be obtained.

Appendix A lists the optimal bias voltage formulas for all phase sets in Table 3.1. Table 3.3 presents the expressions of maximum g_{ac}/P_{diss} with respect to V_{GS1}. Similar results can be obtained for bias voltages $V_{GS2} \sim V_{GS4}$.

Table 3.3 Maximum g_{ac}/P_{diss} expressions for unbalance-biased four-input-MOS transconductors

g_{ac}/P_{diss}	g_{ac}/P_{diss}
$Ph(1,2) = 1/[2\sqrt{T_1} + (c+d)](V_{dd}-V_{ss})$	$Ph(3,4) = 1/[2\sqrt{T_1} - (c+d)](V_{dd}-V_{ss})$
$Ph(5,8) = 1/[2\sqrt{T_2} + 2(b+c+d)](V_{dd}-V_{ss})$	$Ph(6,7) = 1/[2\sqrt{T_3} + 2(b-c-d)](V_{dd}-V_{ss})$
$Ph(9,12) = 1/[2\sqrt{T_4} + 2(c-b-d)](V_{dd}-V_{ss})$	$Ph(10,11) = 1/[2\sqrt{T_5} + 2(d-b-c)](V_{dd}-V_{ss})$
$Ph(13,14) = 1/[2\sqrt{T_6} + 2(b-c+d)](V_{dd}-V_{ss})$	$Ph(15,16) = 1/[2\sqrt{T_7} + 2b](V_{dd}-V_{ss})$
$Ph(17,18) = (c+d)/\left(\left(b^2+c^2\right)+d^2\right)(V_{dd}-V_{ss})$	

In Table 3.3, $b = V_{GS2}-V_{th}$, $c = V_{GS3}-V_{th}$, $d = V_{GS4}-V_{th}$, $T_1 = c^2+d^2$,

$T_2 = b^2+c^2+d^2+(b+c+d)^2$, $T_3 = b^2+c^2+d^2+(b-c-d)^2$, $T_4 = b^2+c^2+d^2+(c-b-d)^2$,

$T_5 = b^2+c^2+d^2+(d-b-c)^2$, $T_6 = b^2+c^2+d^2+(b-c+d)^2$, $T_7 = 2b^2+c^2+d^2$, $T_8 = 2b^2+c^2+d^2$.

Since all the b, c and d have positive values (due to the physical restrictions for MOS transistors to operate properly), assuming $V_{GS2}\sim V_{GS4}$ have the same values for all phase sets, it can be easily found that

$$(g_{ac}/P_{diss})_{1,2} < (g_{ac}/P_{diss})_{3,4}$$

$$(g_{ac}/P_{diss})_{5,8} < (g_{ac}/P_{diss})_{6,9\text{-}14}$$

However, due to the overwhelming 3-D searching space introduced by the changes of b, c and d, it is prohibitive to obtain a simple relation among all the optimal g_{ac}/P_{diss}s in Table 3.3. Hence, numerical-based comparison is necessary and one example will be presented in later Chapters.

Previous analyses have clearly revealed that the optimum g_{ac}/P_{diss} can be different for the same transconductor structure at different phase combinations of the ac input signals. In reality, the net small signal differential output current varies with respect to the relative phase of the input small signal differential voltages. This is illustrated in Fig. 3.5(a)-(c) for phase sets 1, 2 and 3.

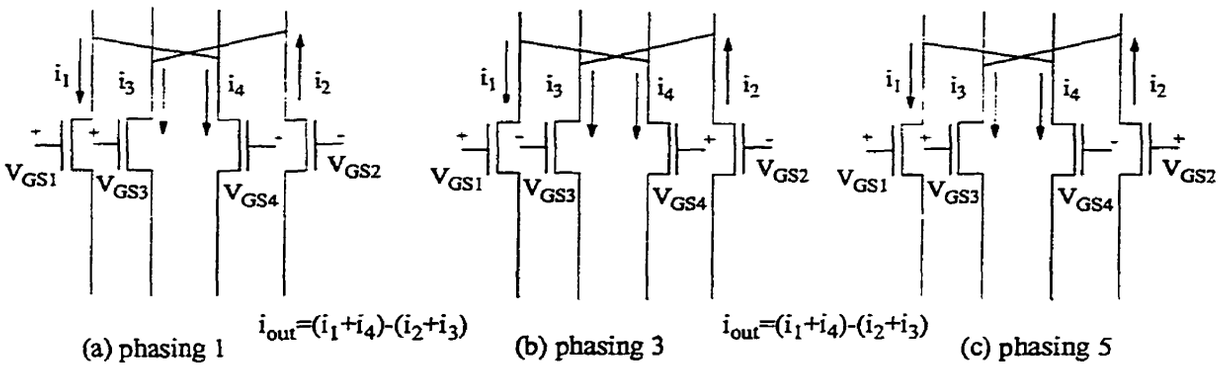


Fig. 3.5 Physical relation between ac phasing and output current

Assuming the absolute values of $i_1, i_2, \ldots i_4$ are the same for Fig. 3.5(a)-(c), different g_{ac} for the three cases can be obtained as a result of different current directions. The different values of g_{ac} gives rise to different g_{ac}/P_{diss}s because the amount of power dissipation of the three cases are the same.

At this point, it may be interesting to elaborate on the concept of dc offset and relative phasings of the input ac signals. Difference in the phasings of the ac signal can be conceived of as a *de facto* offset, but it does not constitute a dc offset. From the above discussions, it becomes clear that a dc offset between the two halves of the transconductor structure (between the transistors in the two-MOS structure and between the pairs of transistors in the four-MOS structure) facilitates maximization of the g_{ac}/P_{diss} ratio. This observation may not be very novel since changed bias conditions are likely to change the dc power dissipations and hence lead to changed values of g_{ac}/P_{diss} . A more novel information is the knowledge that the maximal values of g_{ac}/P_{diss} can be increased by suitable choice of the relative phasing of the input ac signals. This phenomenon can be observed clearly in Chapter 4 when numerical analyses are conducted. This finding and its significance can be expressed as follows: Assuming the dc biases are the same for all phase sets, the corresponding g_{ac}/P_{diss} of each ac phase set is different. So the designer has two degrees of freedom to maximize the g_{ac}/P_{diss} ratio, that is, (i) choose an optimum dc offset value; and/or (ii) choose an optimum ac signal phasing.

3.4.2 Transconductors with drain/source-biased input MOS operating in saturation region

The control voltages of a four-input MOS transistors can also be applied to the drain or source terminals and hence leads to drain/source-biased saturated-operating transconductor structures. Fig. 3.6 depicts the schematic of drain/source-biased transconductor structure with PMOS transistors being the input transistors.

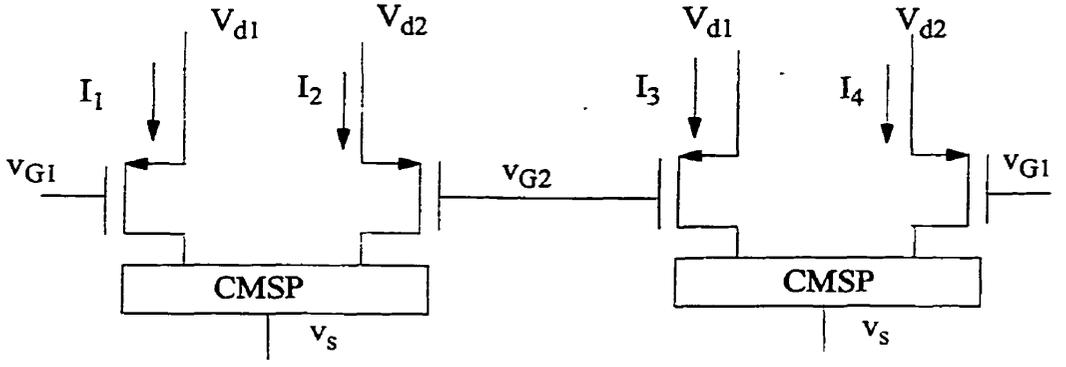


Fig. 3.6 Drain/Source-biased transconductor

By combining the four branch currents of Fig. 3.6 in different ways and deriving the corresponding ac transconductance expressions, three combinations are found to be able to result in linear transconductor implementation. The g_{ac}/P_{diss} expressions and the ac phase arrangements of these three linear transconductors are given in Table 3.4.

Table 3.4 g_{ac}/P_{diss} for drain/source-biased transconductors

Current Combination	g_{ac}/P_{diss}	ac phase assignment
$I_{out} = I_1 + I_2 - I_3 - I_4$	$\frac{2\chi}{b_0\chi^3 + b_1\chi^2 + b_2\chi + b_3}$	$v_{GS1} = V_{c1} + v_{id}/2$ $v_{GS2} = V_{c2} - v_{id}/2$
$I_{out} = I_1 + I_3 - I_2 - I_4$	$\frac{-2\chi}{b_0\chi^3 + b_1\chi^2 + b_2\chi + b_3}$	$v_{G1} = V_{c1} + v_{id}/2$ $v_{G2} = V_{c2} + v_{id}/2$
$I_{out} = I_1 + I_4 - I_2 - I_3$	$\frac{-2[\chi + 2V_{d2} - (V_{c1} + V_{c2}) - 2\lvert V_{tp}\rvert]}{b_0\chi^3 + b_1\chi^2 + b_2\chi + b_3}$	$v_{GS1} = V_{c1} + v_{id}/2$ $v_{GS2} = V_{c2} - v_{id}/2$

The definition of variables χ and the coefficients in the power dissipation expressions of the three

combinations are given below:

$$V_{d1} - V_{d2} = \chi$$

$$b_0 = 2$$

$$b_1 = 2[(2V_{d2} - V_{c1} - V_{c2} - 2V_{th}) + (V_{d2} - V_s)]$$

$$b_2 = (V_{d2} - V_{c1} - V_{th})^2 + (V_{d2} - V_{c2} - V_{th})^2 + 2(2V_{d2} - V_{c1} - V_{c2} - 2V_{th})(V_{d2} - V_s)$$

$$b_3 = 2(V_{d2} - V_{c1} - V_{th})^2(V_{d2} - V_s) + 2(V_{d2} - V_{c2} - V_{th})^2(V_{d2} - V_s)$$

For NMOS based four-input-MOS drain/source-biased transconductors, the g_{ac}/P_{diss} expressions are similar to those of PMOS based structures but with the following modifications: i) χ is now becoming $V_{s1} - V_{s2}$; ii) $V_{d2} - V_{c1}$, $V_{d2} - V_{c2}$ and $V_{d2} - V_s$ are replaced by $-(V_{s2} - V_{c1})$, $-(V_{s2} - V_{c2})$ and $V_d - V_{s2}$ respectively. Due to the similarity between NMOS and PMOS structures, we will only study PMOS structures in the following context. The results obtained for PMOS structures can be modified properly to produce the results of NMOS structures.

Looking at the g_{ac}/P_{diss} expressions in Table 3.4, we see that they all have the similar form as that of the abstract case 3 in section 3.2. The first and second combinations correspond to $\varepsilon = 0$ and $\lambda = 0$ of abstract case 3, while the third combination corresponds to $\varepsilon = 0$ of abstract case 3. Replacing the symbols in eqn.(3.1) by the proper design variables, three fourth-order equations can be obtained for the three output current combinations. The acceptable solution for each of the three equations is the optimal χ of that corresponding g_{ac}/P_{diss} expression.

Because the g_{ac}/P_{diss} optimization concerns only the absolute value of the ratio, the g_{ac}/P_{diss} expressions of the first and second current combinations can be regarded as identical because they are only opposite in sign. Thus the optimization results of these two combinations are the same. For the third current combination, it is easy to prove that $2V_{d2} - (V_{c1} + V_{c2}) - 2|V_{tp}| > 0$. Therefore, *when $\chi > 0$, the third combination will give higher optimal g_{ac}/P_{diss}; when $\chi < 0$, the optimal g_{ac}/P_{diss} of the third combination could be higher or lower than the first and second combinations depending on the values of* $(2V_{d2} - (V_{c1} + V_{c2}) - 2|V_{tp}|)$ *and* χ ..

3.4.3 Transconductors with input MOS operating in mixed region

In section 2.1.3, we have discussed transconductors which are based on MOS transistors operating in saturation and linear regions. In this section and the rest context, we will use "input MOS in mixed region" to represent transconductors in this category. One of the commonly used four-input-MOS transconductors of this kind consists of two blocks of Fig. 3.3(a) and uses differential ac input signals. This is shown in Fig. 3.7.

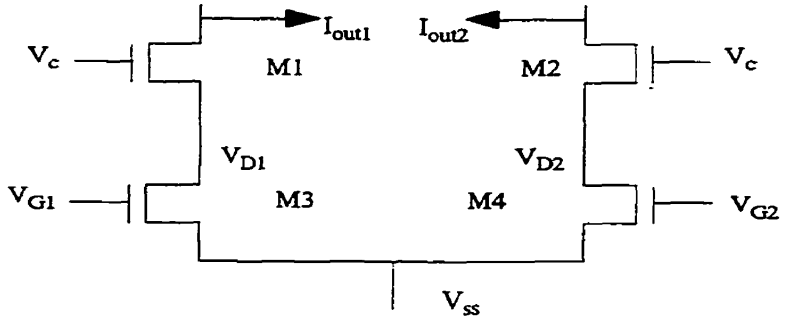


Fig. 3.7 Conceptual diagram of four-input MOS transconductor based on Fig.3.3(a)

Assume $V_{GS1} = V_{GS} + v_{id}/2$, $V_{GS2} = V_{GS} - v_{id}/2$. The output current of Fig. 3.7 is expressed by

$$I_{out} = I_{out1} - I_{out2} = 2\beta V_{DS} v_{id} \tag{3.62}$$

where $\beta = \mu C_{ox}\left(\frac{W}{L}\right)_{M1}$, v_{id} represents the differential ac input signal. Simple derivation shows that if v_{id} is the same as that of the two-MOS structure (i.e., Fig. 3.3(a)), the g_{ac}/P_{diss} expression of Fig. 3.7 will be the same as that of Fig. 3.3(a) . *Therefore the maximum g_{ac}/P_{diss} for both two-MOS and four-MOS mixed saturated-triode-operating transconductor structures are (by substituting V_{ds} by V_{GS}-V_{th})*

$$\left.\frac{g_{ac}}{P_{diss}}\right|_{max} = \frac{2}{(V_{GS} - V_{th})(V_{dd} - V_{ss})} \tag{3.63}$$

Employing two Fig. 3.3(b) (Coban 94) structures and using differential ac input signals, it is possible to implement another transconductor structure which has four-input MOS transistors operating in mixed region. This is shown in Fig. 3.8. Strictly speaking, Fig. 3.8 is

not a four-input-MOS transconductor. But if only the dominant transistor in each branch is considered, it can be looked upon as four-input-MOS structure.

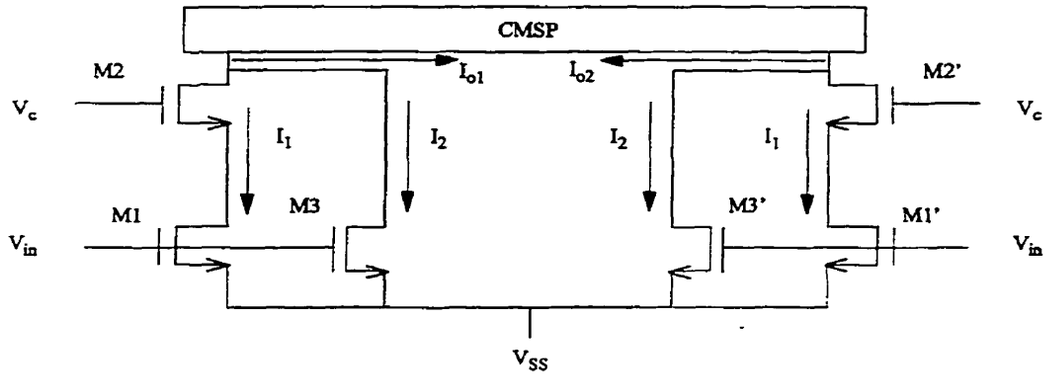


Fig. 3.8 Conceptual diagram of four-input MOS transconductor based on Fig.3.3(b)

Assuming all NMOS transistors are matched and neglecting channel length modulation, the differential output current can be derived as

$$I_{out} = I_{o1} - I_{o2} = K(V_{ds} + V_{GS} - V_{th})v_{id} \tag{3.64}$$

The dc power dissipation is expressed by

$$P_{diss} = K[2(V_{GS} - V_{th})V_{ds} - V_{ds}^2 + (V_{GS} - V_{th})^2](V_{dd} - V_{ss}) \tag{3.65}$$

where $K = \mu C_{ox}\frac{W}{L}$ for eqns.(3.64) and (3.65), V_{GS} is the dc gate-source voltage of transistors M1 and M1', V_{ds} is the drain-source voltage of M1 and M1'. Optimizing g_{ac}/P_{diss} with respect to V_{ds}, we get

$$V_{ds|opt} = (V_{GS} - V_{th}) \text{ or } 0 \tag{3.66}$$

and the corresponding optimal g_{ac}/P_{diss} is

$$\left.\frac{g_{ac}}{P_{diss}}\right|_{max} = \frac{1}{(V_{GS} - V_{th})(V_{dd} - V_{ss})} \tag{3.67}$$

If same V_{GS} is applied to Fig. 3.7 and Fig. 3.8, comparing eqns.(3.63) and (3.67) we see

that Fig. 3.7 gives the higher optimal g_{ac}/P_{diss} .

3.4.4 Transconductors with input MOS operating in linear region

The transconductor structure which consists of four linearly operating input-MOS transistors is shown in Fig. 2.9(c) and re-drawn in Fig. 3.9.

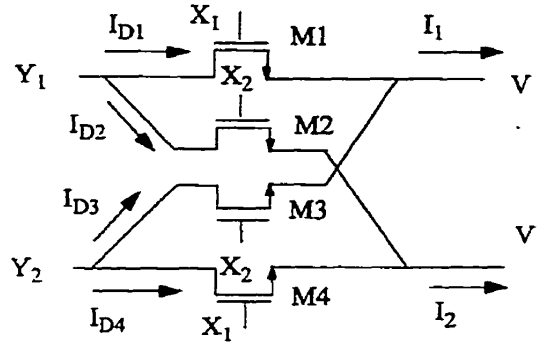


Fig. 3.9 Linearly operating transconductor

Assuming M1 and M2, M3 and M4 are matched, we can obtain from eqn.(2.17) (section 2.1.2)

$$I_{out} = I_1 - I_2 = \mu C_{ox}\frac{W}{L}(X_1 - X_2)(Y_1 - Y_2) \tag{3.68}$$

The power dissipation of Fig. 3.9 can be expressed by

$$P_{diss} = \mu C_{ox}\frac{W}{L}[(X_{1dc} + X_{2dc} - 2V - 2V_{tn})(Y_{1dc} + Y_{2dc} - 2V) - (Y_{1dc} - V)^2 - (Y_{2dc} - V)^2] \tag{3.69}$$

The X_{1dc}, X_{2dc} and Y_{1dc}, Y_{2dc} refer to dc biases on the X and Y terminals. Depending on the terminals to which the ac input signals are fed, we will have

$$X_1 = X_{1dc} + v_{in1} \quad X_2 = X_{dc2} + v_{in2} \text{ or } Y_1 = Y_{1dc} + v_{in1} \quad Y_2 = Y_{dc2} + v_{in2} \tag{3.70}$$

Looking at eqn.(3.68) and (3.69), we see that the X variables of the two equations are in the same order. We can prove that the g_{ac}/P_{diss} can not be optimized with respect to Xs. So

the optimization of the g_{ac}/P_{diss} can only be performed with respect to Ys. The optimal Ys are derived as

$$Y_{1opt} = Y_{2dc} \pm \sqrt{2Y_{2dc}^2 - 4VY_{2dc} - 2(Y_{2dc} - V)(X_{1dc} + X_{2dc} - 2V - 2V_{th})} \tag{3.71}$$

$$Y_{2opt} = Y_{1dc} \pm \sqrt{2Y_{1dc}^2 - 4VY_{1dc} - 2(Y_{1dc} - V)(X_{1dc} + X_{2dc} - 2V - 2V_{th})} \tag{3.72}$$

for X-driving cases and

$$Y_{1opt} = Y_{2opt} = (X_{1dc} + X_{2dc} - 2V_{th})/2 \tag{3.73}$$

for Y-driving cases. The feasibility of above optimization results needs to be examined by physical restrictions of the transistors. For Fig.3.9, the restrictions are

$$Y - V < X - V - V_{th} \quad \text{and} \quad X - V > V_{th} \tag{3.74}$$

where X refers to X_{1dc}, X_{2dc} and Y refers to Y_{1dc}, Y_{2dc}.

3.5 Optimizing g_{ac}/P_{diss} for eight input-MOS transconductors

Transconductors with eight major input MOS transistors have also been proposed and studied in literature. They are mostly gate-biased structures. In this section, we will give a closer look at some important eight input-MOS transconductors and find out their optimal g_{ac}/P_{diss}.

3.5.1 Four-input-MOS based eight-input-MOS transconductors

In section 2.1.1, we mentioned CMOS double pair. By replacing the single MOS transistors in four-input-MOS transconductor structures by CMOS double pairs, eight-input-MOS transconductors can be easily implemented. Fig.3.10 shows the diagram of such kind of the eight-input-MOS transconductor. Defining

$$V_{GS1} = V_1 - V_a - V_{tn} - |V_{tp}| \quad V_{GS2} = V_2 - V_b - V_{tn} - |V_{tp}| \quad V_{GS3} = V_3 - V_c - V_{tn} - |V_{tp}|$$
$$V_{GS4} = V_4 - V_c - V_{tn} - |V_{tp}| \tag{3.75}$$

the output current of Fig.3.10 is obtained as

$$I_{out} = K_{eq}(v_{GS1} + v_{GS2} - 2V_{theq})(v_{GS1} - v_{GS2}) + K_{eq}(v_{GS3} + v_{GS4} - 2V_{theq})(v_{GS3} - v_{GS4}) \tag{3.76}$$

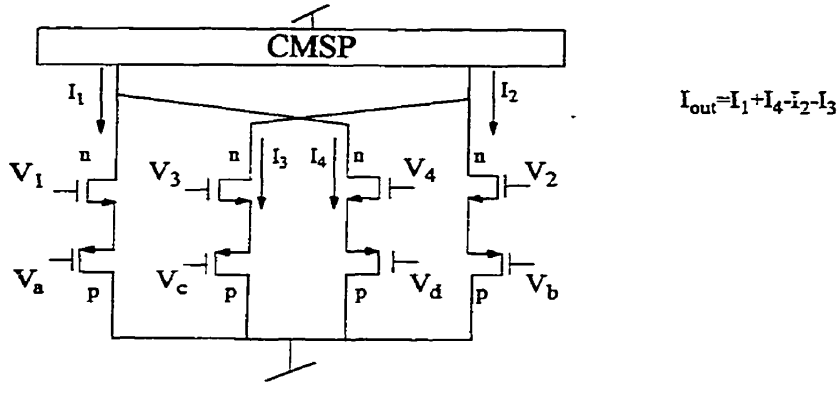


Fig. 3.10 Conceptual diagram of eight input-MOS transconductor

In eqn.(3.76) $K_{eq} = (K_p K_n)/(\sqrt{K_p} + \sqrt{K_n})^2$ and $V_{theq} = V_{tn} + |V_{tp}|$. Comparing eqn.(3.76) with eqn.(3.39), the similarity can be observed. Therefore, the analyses given in section 3.4.1 can be applied to Fig. 3.10 directly with V_{th} being replaced by V_{theq} and K by K_{eq}.

The advantage of using CMOS double pair is that each bias voltage is connected between the two gate terminals of a CMOS double pair. Thus a bias voltage can be adjusted through any of the two gate terminals. In addition, since the bias voltages are isolated from the source terminals of the transistors due to the large gate-source resistance, the potential fluctuations of the source terminals will not affect the operation of the circuit as long as the gate voltages remain unchanged. Thus the PSRR performance of CMOS double pair structure is much better than that of single MOS structures. The disadvantage of using CMOS double pair is that the threshold voltage (i.e., V_{theq}) is bigger than the V_{th} of single MOS structure and hence larger bias voltages and higher supply voltages are needed. These drawbacks prevent the CMOS double pair transconductors from operating at low power

and low voltage environment. So such kind of eight input-MOS transconductors are used in the cases when low voltage and low power operations are not of major concerns.

3.5.2 Other eight-input-MOS transconductors

There also are eight-input-MOS transconductors which do not have corresponding four-input-MOS structure. The transconductances of these eight-input-MOS transconductors need to be derived from the I-V relationship of the structures. Fig. 3.11 shows the basic circuit of the eight-input-MOS structures.

Assume all NMOS transistors are matched and so are all PMOS transistors. Using the square-law model for the transistors and neglecting channel length modulation, we have

$$I_1 = K_{eq}(V_1 - V_a - V_{theq})^2 \quad I_2 = K_{eq}(V_2 - V_b - V_{theq})^2 \quad I_3 = K_{eq}(V_3 - V_c - V_{theq})^2$$
$$I_4 = K_{eq}(V_4 - V_d - V_{theq})^2 \tag{3.77}$$

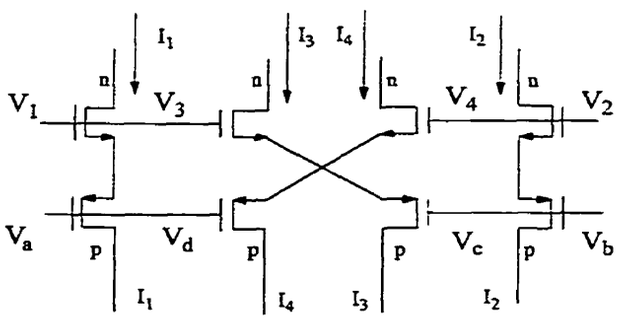


Fig. 3.11 Basic structure of eight input-MOS transconductor

If the output current of Fig. 3.11 is defined by one of the six combinations in Table 3.6, a linear transconductor structure can be achieved.

Table 3.5 Output current expressions of eight input-MOS linear transconductor

$I_{out} = [(I_1 + I_2) - (I_3 + I_4)]$	$I_{out} = -[(I_1 + I_2) - (I_3 + I_4)]$
$I_{out} = [(I_1 + I_3) - (I_2 + I_4)]$	$I_{out} = -[(I_1 + I_3) - (I_2 + I_4)]$
$I_{out} = [(I_1 + I_4) - (I_2 + I_3)]$	$I_{out} = -[(I_1 + I_4) - (I_2 + I_3)]$

Let $$X_1 = V_1 - V_a \quad X_2 = V_2 - V_b \quad Y_1 = V_3 - V_c \quad Y_2 = V_4 - V_d \tag{3.78}$$

Substituting eqn.(3.77) into the output current expressions of Table 3.6 and replacing the voltage variables by *Xs* and *Ys* of eqn.(3.78), we obtained the voltage expressions of Table 3.6.

Table 3.6 Voltage expressions corresponding to Table 3.5

Current Combinations	Corresponding Voltage expressions
$I_1+I_2-(I_3+I_4)=I_1-I_3+I_2-I_4=I_1-I_4+I_2-I_3$	$=K_{eq}[(X_1+Y_1-2V_{theq})(X_1-Y_1)+(X_2+Y_2-2V_{theq})(X_2-Y_2)]$ $=K_{eq}[(X_1+Y_2-2V_{theq})(X_1-Y_2)+(X_2+Y_1-2V_{theq})(X_2-Y_1)]$
$I_1+I_3-(I_2+I_4)=I_1-I_2+I_3-I_4=I_1-I_4+I_3-I_2$	$=K_{eq}[(X_1+X_2-2V_{theq})(X_1-X_2)+(Y_1+Y_2-2V_{theq})(Y_1-Y_2)]$ $=K_{eq}[(X_1+Y_2-2V_{theq})(X_1-Y_2)-(X_2+Y_1-2V_{theq})(X_2-Y_1)]$
$I_1+I_4-(I_2+I_3)=I_1-I_2+I_4-I_3=I_1-I_3+I_4-I_2$	$=K_{eq}[(X_1+X_2-2V_{theq})(X_1-X_2)-(Y_1+Y_2-2V_{theq})(Y_1-Y_2)]$ $=K_{eq}[(X_1+Y_1-2V_{theq})(X_1-Y_1)-(X_2+Y_2-2V_{theq})(X_2-Y_2)]$

From Table 3.6 one can see that by properly arranging the *Xs* and *Ys*, linear transconductors governed by different ac transconductance expressions can be achieved.

Czarnul and Takagi [29] implemented and analyzed five different linear transconductor structures based on a sub-set of Fig. 3.11.This is shown in Fig. 3.12.

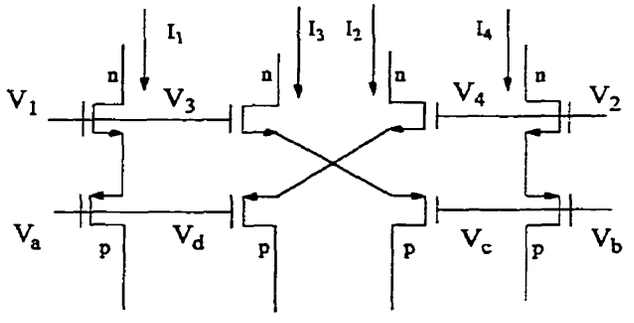


Fig. 3.12 Czarnul and Takagi's CMOS differential transconductor cell

The connection of Fig.3.12 leads to

$$X_1+X_2=Y_1+Y_2 \text{ or } X_1-Y_1=-(X_2-Y_2) \tag{3.79}$$

The five transconductor types are defined as follows.

I. $I_{out} = I_1 - I_4$ with $V_1 - V_b = V_2 - V_a = V_c = const$;

II.a. $I_{out} = I_1 - I_2$ or $I_{out} = I_3 - I_4$ with $I_1 + I_2 - I_3 - I_4 = I_c = const$ and $V_b - V_a = V_c = const$;

II.b. $I_{out} = I_3 - I_1$ or $I_{out} = I_4 - I_2$ with $I_1 + I_3 - I_2 - I_4 = I_c = const$ and $V_1 - V_2 = V_c = const$;

III. $I_{out} = I_1 + I_3 - I_2 - I_4$ or $I_{out} = I_3 + I_4 - I_1 - I_2$ with $(I_1 + I_3 - I_2 - I_4)/(V_1 - V_2) = (I_1 + I_2 - I_3 - I_4)/(V_b - V_a)$;

IV.a. $I_{out} = I_1 + I_4 - I_2 - I_3$ with $I_1 + I_2 - I_3 - I_4 = I_c = const$ and $V_b - V_a = V_c = const$;

IV.b. $I_{out} = I_2 + I_3 - I_1 - I_4$ with $I_1 + I_3 - I_2 - I_4 = I_c = const$ and $V_1 - V_2 = V_c = const$;

According to the definitions of *X*s and *Y*s in eqn.(3.78), we can replace the output current expressions of the above five transconductor types by voltage expressions.

I. $I_{out} = K_{eq}(X_1 - X_2)(X_1 + X_2 - 2V_{theq})$ with $X_1 + X_2 = Y_1 + Y_2 = V_c = const$;

II.a. $I_{out} = K_{eq}(X_1 - Y_2)(X_1 + Y_2 - 2V_{theq})$

with $X_1 - Y_1 = Y_2 - X_2 = V_c = const$ and $X_1 + Y_2 - 2V_{theq} = (I_c/2K_{eq}V_c) + V_c$;

or $I_{out} = K_{eq}(Y_1 - X_2)(Y_1 + X_2 - 2V_{theq})$

with $X_1 - Y_1 = Y_2 - X_2 = V_c = const$ and $Y_1 + X_2 - 2V_{theq} = (I_c/2K_{eq}V_c) - V_c$;

II.b. $I_{out} = K_{eq}(X_1 - Y_1)(X_1 + Y_1 - 2V_{theq})$

with $X_1 - Y_2 = Y_1 - X_2 = V_c = const$ and $X_1 + Y_1 - 2V_{theq} = (I_c/2K_{eq}V_c) + V_c$;

or $I_{out} = K_{eq}(X_2 - Y_2)(X_2 + Y_2 - 2V_{theq})$

with $X_1 - Y_2 = Y_1 - X_2 = V_c = const$ and $X_2 + Y_2 - 2V_{theq} = (I_c/2K_{eq}V_c) + V_c$;

III.a. $I_{out} = K_{eq}(X_1 + Y_1 + X_2 + Y_2 - 4V_{theq})(X_1 - Y_2)$

with $X_1 - Y_1 = Y_2 - X_2 = V_c = const$ and $X_1 + Y_1 + X_2 + Y_2 - 4V_{theq} = I_c/(K_{eq}V_c)$;

III.b. $I_{out} = K_{eq}(X_1 + Y_1 + X_2 + Y_2 - 4V_{theq})(X_1 - Y_1)$

with $X_1 - Y_2 = Y_1 - X_2 = V_c = const$ and $X_1 + Y_1 + X_2 + Y_2 - 4V_{theq} = I_c/(K_{eq}V_c)$;

IV.a. $I_{out} = 2K_{eq}(X_1 - Y_1)(X_1 - Y_2)$ with $X_1 - Y_1 = Y_2 - X_2 = V_c = const$;

IV.b. $I_{out} = 2K_{eq}(Y_1 - X_1)(Y_1 - X_2)$ with $X_1 - Y_2 = Y_1 - X_2 = V_c = const$;

V. Similar to IV.

The total dc power dissipation for each transconductor type can be expressed by

I. $P_{diss} = K_{eq}[(X_{1dc} - V_{theq})^2 + (X_{2dc} - V_{theq})^2 + (Y_{1dc} - V_{theq})^2 + (Y_{2dc} - V_{theq})^2](V_{dd} - V_{ss})$

II.a. $P_{diss} = K_{eq}[2(X_{2dc} - V_{theq})^2 + 2(Y_{1dc} - V_{theq})^2 + I_c](V_{dd} - V_{ss})$

II.b. $P_{diss} = K_{eq}[2(X_{2dc} - V_{theq})^2 + 2(Y_{2dc} - V_{theq})^2 + I_c](V_{dd} - V_{ss})$

III. $P_{diss} = K_{eq}[2(X_{2dc} - V_{theq})^2 + 2(Y_{2dc} - V_{theq})^2 + I_c/V_c](V_{dd} - V_{ss})$

IV. $P_{diss} = K_{eq}[2(X_{2dc} - V_{theq})^2 + 2(Y_{2dc} - V_{theq})^2 + I_c](V_{dd} - V_{ss})$

V. Similar to IV.

Having the expressions of output currents and dc power dissipations, it is possible to study the g_{ac}/P_{diss} of each transconductor type proposed by Czarnul et al.

I. Assume $X_1 - X_2 = nv_{id}$, in which n is a constant, we have

$$\frac{g_{ac}}{P_{diss}} = \frac{n(V_c - 2V_{theq})}{[2X_{1dc}^2 + 2Y_{1dc}^2 - 2(X_{1dc} + Y_{1dc} + 2V_{theq})V_c + 6V_c^2](V_{dd} - V_{ss})} \tag{3.80}$$

Optimizing eqn.(3.80) with respect to V_c we get

$$V_{copt} = 2V_{theq} + 2\sqrt{V_{theq}^2 - \frac{2V_{theq}(X_{1dc} + Y_{1dc} + 2V_{theq}) - X_{1dc}^2 - Y_{1dc}^2}{12}} \tag{3.81}$$

II.a Assume $X_1 - Y_2 = nv_{id}$ or $Y_1 - X_2 = nv_{id}$ we have

$$\frac{g_{ac}}{P_{diss}} = \frac{n(I_c/(2V_c) + K_{eq}V_c)}{K_{eq}[2(X_{2dc} - V_{theq})^2 + 2(Y_{1dc} - V_{theq})^2 + I_c](V_{dd} - V_{ss})} \tag{3.82}$$

and $$V_{copt} = 1 + \sqrt{1 + (nI_c)/(2K_{eq})} \tag{3.83}$$

II.b Assume $X_1 - Y_1 = nv_{id}$ or $X_2 - Y_2 = nv_{id}$ we have

$$\frac{g_{ac}}{P_{diss}} = \frac{n(I_c/(2V_c) + K_{eq}V_c)}{K_{eq}[2(X_{2dc} - V_{theq})^2 + 2(Y_{2dc} - V_{theq})^2 + I_c](V_{dd} - V_{ss})} \tag{3.84}$$

and $$V_{copt} = 1 + \sqrt{1 + (nI_c)/(2K_{eq})} \tag{3.85}$$

III. Assume $X_1 - Y_2 = nv_{id}$ or $X_1 - Y_1 = nv_{id}$, we have

$$\frac{g_{ac}}{P_{diss}} = \frac{n(I_c/V_c)}{K_{eq}[2(X_{2dc}-V_{theq})^2 + 2(Y_{2dc}-V_{theq})^2 + I_c/V_c](V_{dd}-V_{ss})} \tag{3.86}$$

Eqn.(3.86) is monotonically decreasing with V_c and increasing with I_c. Thus the lowest acceptable V_c will correspond to highest g_{ac}/P_{diss} or the highest acceptable I_c will lead to highest g_{ac}/P_{diss}.

IV. Assume $X_1 - Y_2 = nv_{id}$ or $Y_1 - X_2 = nv_{id}$, we have

$$\frac{g_{ac}}{P_{diss}} = \frac{2nV_c}{[2(X_{2dc}-V_{theq})^2 + 2(Y_{2dc}-V_{theq})^2 + I_c](V_{dd}-V_{ss})} \tag{3.87}$$

Eqn.(3.87) is monotonically increasing with V_c and decreasing with I_c. Maximal g_{ac}/P_{diss} will be decided by the highest acceptable V_c or the lowest acceptable I_c.

The above analyses on Czarnul's differential transconductor cells give an example of optimizing g_{ac}/P_{diss} for eight-input-MOS transconductors. Several other eight-input-MOS linear transconductors can be implemented by properly setting Xs and Ys in Table 3.6. Exhaustively exploring all possible eight-input-MOS linear transconductors is possible but is going to be too time and space consuming. Since our concentration is the frequency-power -efficiency optimization methodology and the procedures of the optimization are similar no matter which transconductor structure is studied, so we will restrict our g_{ac}/P_{diss} optimization analyses to the transconductor structures which have already been addressed by other researchers.

Instead of employing bias voltages to adjust g_{ac}/P_{diss}, some transconductors achieve g_{ac}/P_{diss} adjustment by changing bias currents. Seevinck and Wassenaar [17] proposed a transconductor structure as shown in Fig. 3.13.

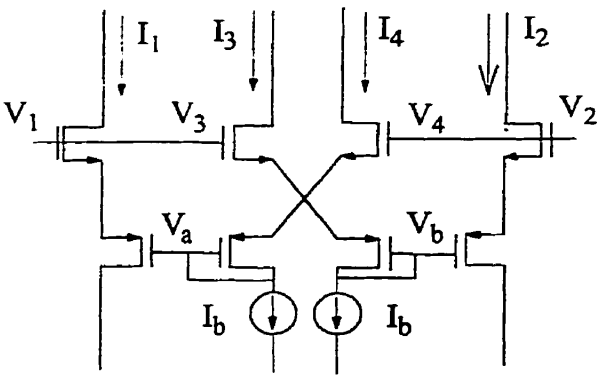


Fig. 3.13 Seevinck and Wassenaar transconductor

It has: $V_1=V_3$ $V_a=V_d$ $V_2=V_4$ $V_b=V_c$ $I_3=I_4=I_b=const$

and the output current is defined by $I_{out} = I_1 - I_2$. Employing bias current as the independent control variable, the g_{ac}/P_{diss} of Fig. 3.13 is obtained as

$$\frac{g_{ac}}{P_{diss}} = \frac{\sqrt{2K_{eq}I_b}}{4I_b(V_{dd}-V_{ss})} \tag{3.88}$$

when ac input signal is defined as $V_1 - V_2 = v_{id}$.

Eqn.(3.88) is a monotonically decreasing function of I_b. So the highest g_{ac}/P_{diss} is corresponding to the lowest acceptable I_b.

A modified structure of Fig. 3.13 was proposed by Walker and Green[27]. The circuit diagram is shown in Fig. 3.14.

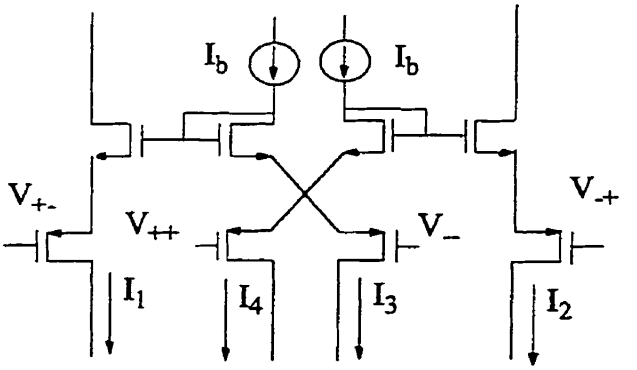


Fig. 3.14 Walker and Green transconductor

Assuming $(V_{+-}+V_{-+})-(V_{++}+V_{--})=0$, the output current of Fig. 3.14 is

$$I_{out} = I_1 - I_2 = \sqrt{2K_{eq}I_b}\ [(V_{++}-V_{-+})-(V_{--}-V_{+-})] \tag{3.89}$$

The g_{ac}/P_{diss} expression as well as the optimization result of Fig. 3.14 are the same as those of Fig. 3.13.

3.6 Summary

In this chapter, the g_{ac}/P_{diss} ratio which reflects the frequency-power-efficiency characteristic of a CMOS linear transconductor structure has been studied very carefully. The general mathematical expressions of the possible g_{ac}/P_{diss} functions and their respective optimization results have been provided first. Transconductor structures consisting of up to eight major input MOS transistors were studied in detail. Their analytical g_{ac}/P_{diss} expressions are obtained and optimized employing the optimization results of general mathematical expressions. All the optimization performed is based on the assumption that the objective function is an single variable function and no constraints are required to be satisfied for the optimization.

However, looking at the analytical g_{ac}/P_{diss} expressions obtained from most of the transconductor structures, precisely, they are multi-variable functions (for example, eqn.(3.10) is a function of V_{GS1} and V_{GS2}). In addition, we have mentioned before that linearity, noise, etc are also very important characteristics of a CMOS transconductor. Therefore a practical frequency-power-efficiency optimization should involve multi-variable search with given constraints. The constraints could reflect the specifications of other characteristics such as linearity and harmonic distortion.

The significance of this chapter lies in the derivation of the analytical expressions for g_{ac}/P_{diss} of various transconductor structures and illustrating the possibility of improving the frequency-power efficiency of a transconductor by selecting dc biases and ac signal phases

properly. The optimization results obtained in this chapter are effective for the situations that only one bias voltage (current) of the transconductor is tuned. Besides, the results of this chapter can also be used as a starting point for the more complicated multi-variable constrained optimization method which will be addressed in Chapter 6.

Chapter 4

Simulations and Experiments for frequency-power Efficiency Optimization I : Unconstrained single variable Optimization

In this chapter, the g_{ac}/P_{diss} characteristic of transconductor structures discussed in previous chapters will be analyzed numerically. Optimal bias voltages are obtained on the basis of unconstrained single variable optimization procedure which has been studied in detail in Chapter 3. To evaluate the effectiveness of the numerical results, HSPICE simulation as well as experiments on a test chip are being conducted. In addition, the linearity characteristics of the transconductors at different biasing conditions are simulated and measured as well.

4.1 Assumptions used

In chapter 3 we have shown that the objective function (g_{ac}/P_{diss}) of a transconductor usually consists of several bias voltages. Assume n bias variables appear in a g_{ac}/P_{diss} function. To ensure that the function is determined by only one of the variables, it is necessary to assign fixed values to the other $n-1$ variables. In order to compare the optimization results among different transconductor structures, the bias conditions used for the transconductors of the same category should be as close as possible. Table 4.1 lists the assumptions made for the simulations and experiments of the g_{ac}/P_{diss} optimizations of the CMOS transconductors. The technology considered is Mitel 1.5μm CMOS technology.

Table 4.1 Biasing conditions for the transconductors

Transconductor	Assumptions (V_{dd}=-V_{ss}=2.5V V_{th}=0.84V if not specified)
Two-MOS balanced	V_{GS}=1.6V
Two-MOS unbalanced	V_{GS1}=1.6V
Four-MOS balanced	For all phases: V_b=1.6V
Four-MOS unbalanced	phase set 1 : V_{GS3}=1.2V V_{diff}=0.32V phase set 2 : V_{GS4}=2.4V V_{diff}=0.4V phase set 3 : V_{GS2}=V_{GS3}=0.96V V_{GS4}=1.2V phase set 4,5: V_{GS2}=V_{GS3}=1.2V V_{GS4}=1.6V phase set 6 : V_{GS2}=1.6V V_{GS3}=V_{GS4}=1.2V phase set 7 : V_{GS2}=V_{GS3}=1.6V V_{GS4}=1.2V phase set 8 : V_{GS2}=V_{GS4}=1.6V V_{GS3}=1.2V phase set 9 : V_{GS2}=1.2V V_{GS3}=V_{GS4}=1.6V
Two-MOS (PMOS) Source-biased	V_{d2}=2.5V V_{c1}=V_{c2}=0.5V V_{ss}=-2.5V V_{thp}=-0.72V
Four-MOS(PMOS) source-biased	V_{d2}=2.5V V_{c1}=V_{c2}=0.5V V_{ss}=-2.5V V_{thp}=-0.72V
Two-MOS mixed operating	V_{GS}=1.6V
Four-MOS mixed operating	V_{GS1}=V_{GS2}=1.6V
Linearly operating *	

1. * Since Fig. 2.9(b) and Fig.3.9 are rarely used on their own as linearly operating transconductors, the biasing conditions and the simulation results will strongly depend on the actual structure (for example, [28]). Therefore, we will not simulate and test structures of Fig.2.9(b) and Fig.3.9. In the case that a linearly operating transconductor structure must be analyzed, similar procedures as those used by other transconductor structures can be followed.

From Table 4.1, one can see that for balanced gate-biased transconductor structures and the mixed-operating input-MOS structures, the fixed bias voltages used are *1.6V*. For unbalanced gate-biased structures, most of the cases use either *1.6V* or *1.2V* as their fixed bias voltages. However, for phase sets 1 and 2, the bias voltages are correlated (see Appendix A) and hence can not be set to arbitrary values; for phase set 3, the variable bias voltage V_{GS1} can not be optimized if the fixed bias voltages used are *1.2V* and *1.6V*. Thus, bias voltages employed for these phase sets are different from *1.6V* and *1.2V*. The bias voltages used for two-MOS and four-MOS source-biased transconductor structures are

identical.

4.2 Numerical Analyses

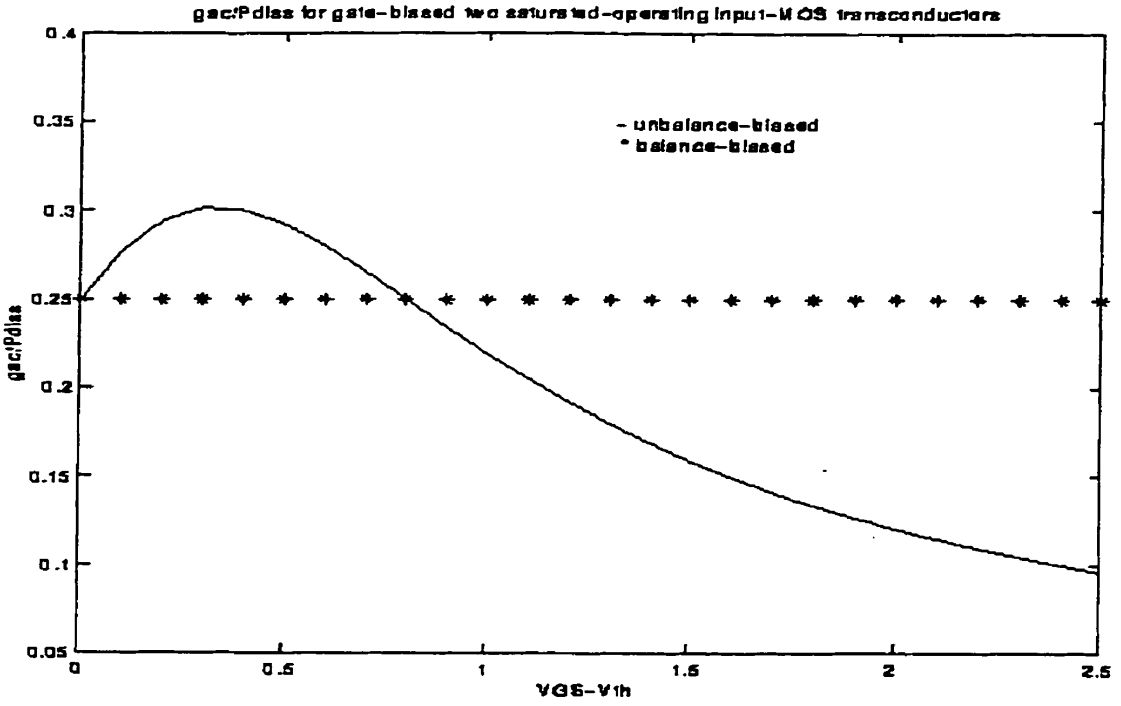
Employing the analytical formulas obtained in Chapter 3 and the values in Table 4.1, the relations between the g_{ac}/P_{diss}s of the CMOS transconductors discussed previously and the corresponding adjustable bias voltages are shown in Figures 4.1(a)-(e).

The y-axes of Fig.4.1(a)-(e) are the absolute g_{ac}/P_{diss} values. The reason of using absolute g_{ac}/P_{diss} is because the amount of transconductance that can be obtained from per unit DC power consumption(i.e., transconductance's power efficiency) are the same for (g_{ac}/P_{diss} is) and ($-g_{ac}/P_{diss}$).

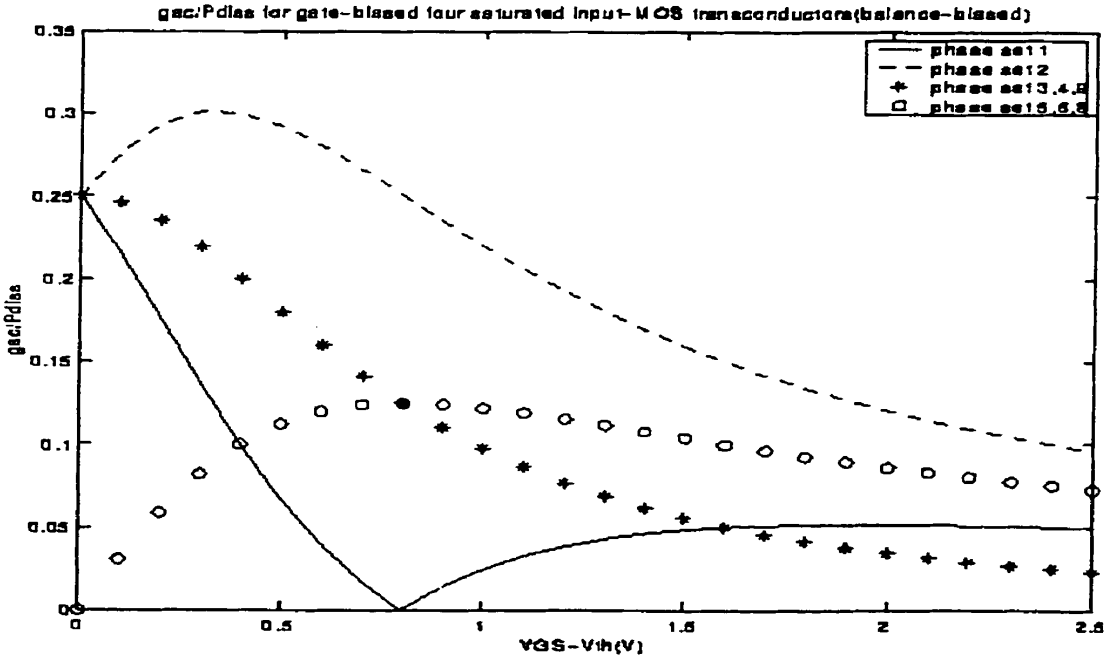
Due to the usage of absolute g_{ac}/P_{diss}, special care should be given while searching for the maximum of the curves. For transconductors where transconductance changes sign, the point that has zero g_{ac}/P_{diss} becomes a discontinuous point. The optimum g_{ac}/P_{diss} of a transconductor should be decided by inspecting the absolute g_{ac}/P_{diss} curve. Taking Fig. 4.1(d) as an example, the g_{ac}/P_{diss} has a maxima at V_{d1}-V_{d2}=*1.0V*. However, when absolute g_{ac}/P_{diss} is considered, the value is monotonically increasing when (V_{d1}-V_{d2}) changing from *-0.5V* to *-1.0V*. And the values are bigger than the maxima of the non-absolute g_{ac}/P_{diss}. Therefore, the bias voltage which corresponds to highest g_{ac}/P_{diss} should be close to *-1.0V*. The optimum g_{ac}/P_{diss} and the respective bias value of other transconductor categories can be obtained similarly.

4.3 HSPICE simulation

In order to verify the accuracy of the results predicted by numerical calculations, circuit simulations using HSPICE have been conducted. The technology used is a 1.5 μm CMOS technology. For each transconductor structure, at least three different bias voltage values are used to show the trend of variation of g_{ac}/P_{diss}, except for two-input-MOS balance-biased structure. The balance-biased two-input-MOS transconductor has only one bias voltage variable, and with the assumption in Table 4.1, the bias voltage is fixed.

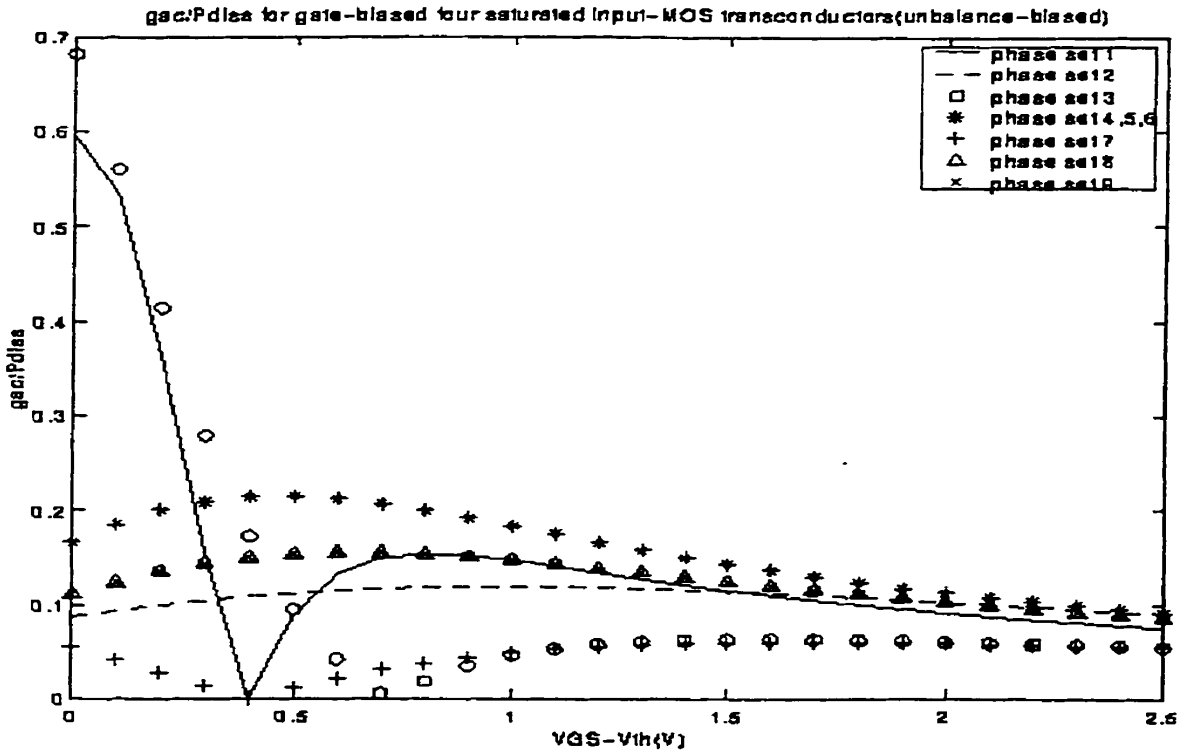


(a) Two-input-MOS

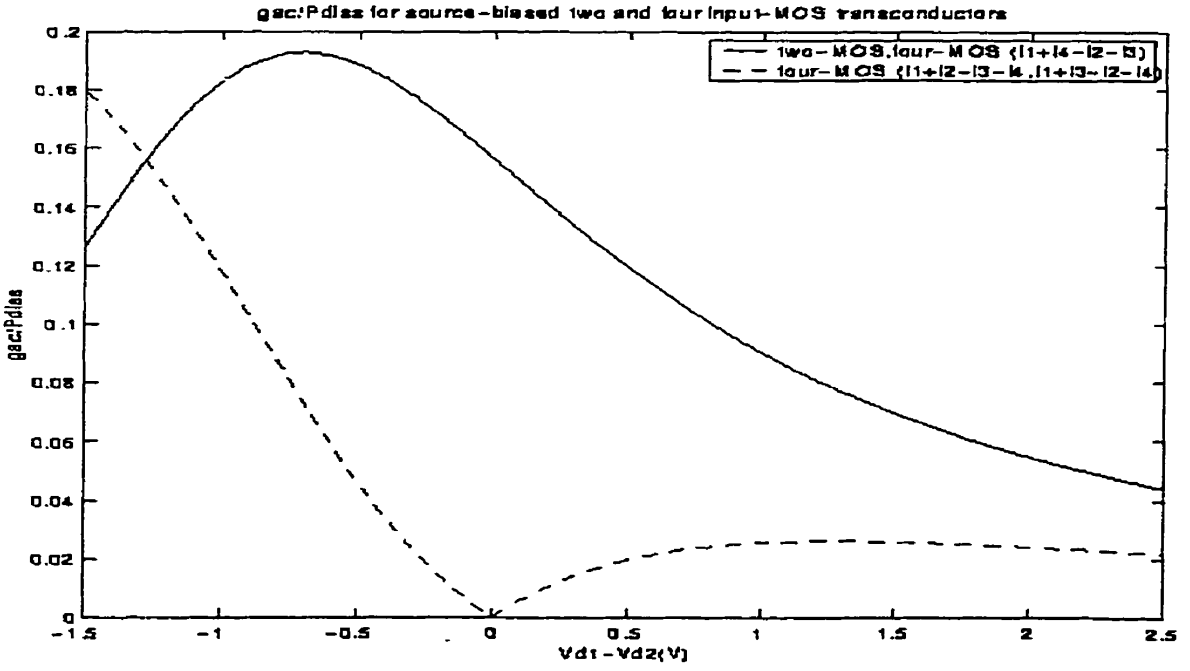


(b) balanced four-input-MOS

Fig. 4.1 g_{ac}/P_{diss} of CMOS transconductors

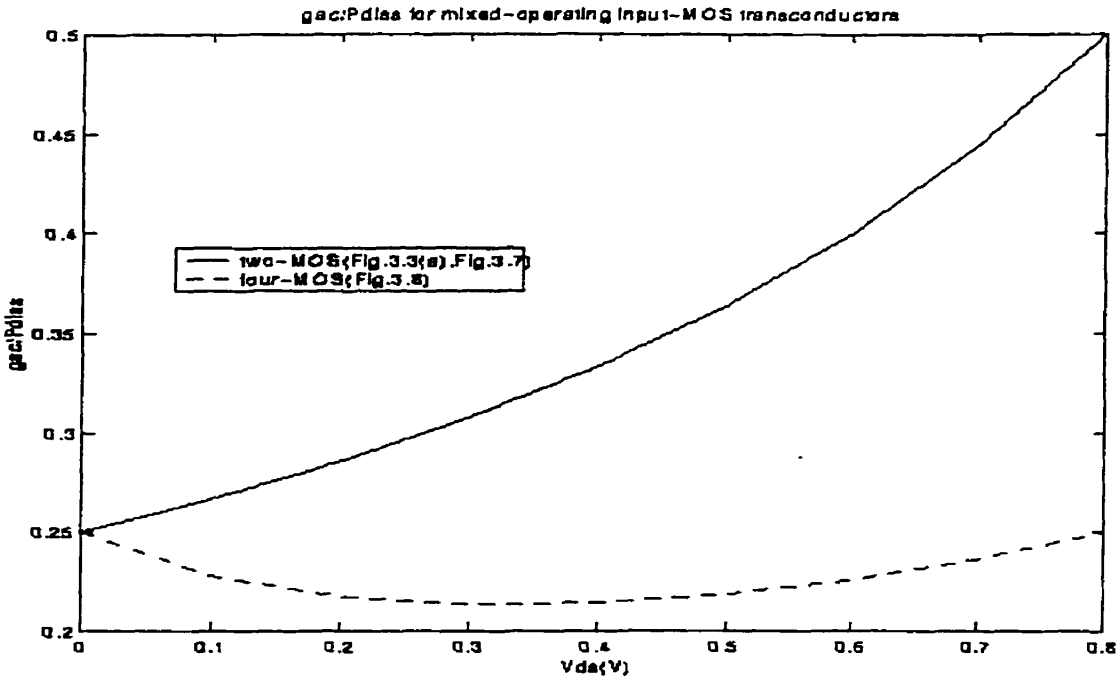


(c) Unbalanced four-input-MOS



(d) Drain/Source-biased structures

Fig.4.1 g_{ac}/P_{diss} of CMOS transconductors(cont'd)



(e) Mixed operating input-MOS structures

Fig.4.1 g_{ac}/P_{diss} of CMOS transconductors(cont'd)

The bias voltages, the calculated g_{ac}/P_{diss}s and the simulated g_{ac}/P_{diss}s corresponded to the given biases are presented in Table 4.2. The optimal bias values and the respective g_{ac}/P_{diss}s are represented by bold numbers. From Table 4.2, one can see that most transconductors present consistent calculation and simulation results. However, larger deviations (i.e., >10%) are observed for four-MOS unbalanced structures with phase sets 1 and 3, four-MOS source-biased structures of combinations 1&2. The reason is that the g_{ac}/P_{diss} expressions of these particular structures are more sensitive to the process parameters, especially the threshold voltages of the input transistors. The calculations are based on the ideal situations, that is, the input transistors are perfectly matching. Thus, the threshold voltage, aspect ratio and other process parameters of each input transistor are having ideal values. However, the transistor models used by the HSPICE (level=3) simulator are much-more complicated. The threshold voltage and other process parameters of the input transis-

tors are non-linearily related with their bias voltages. Therefore, for certain transconductor structure and under certain bias conditions, the discrepancy between the calculated and simulated optimal g_{ac}/P_{diss}s can be more distinguishable. It reveals that for those corner cases, the simplified transistor models are not adequate to describe the performances of those transconductor structures precisely.

Table 4.2 Calculated, Simulated and measured g_{ac}/P_{diss}

Structure	V_{bias}(V)	Calculated g_{ac}/P_{diss}	Simulated g_{ac}/P_{diss}	Experimental g_{ac}/P_{diss}
Two-MOS balanced	**1.6**	**0.25**	**0.2586**	**0.24**
Two-MOS unbalanced	1.0	0.287	0.291	0.282
	1.13	**0.301**	**0.314**	0.288
	1.2	0.292	0.3	**0.295**
	1.5	0.28	0.27	0.285
Four-MOS balanced (phase set 1)	**0.9**	**0.215**	**0.236**	**0.259**
	1.0	0.177	0.19	0.22
	1.2	0.1	0.1	0.141
(phase set 2)	1.0	0.294	0.3	0.282
	1.13	**0.301**	**0.314**	0.288
	1.2	0.3	0.313	**0.295**
	1.5	0.265	0.276	0.285
(phase set 3,4,9)	**0.9**	**0.246**	**0.257**	**0.236**
	1.0	0.235	0.247	0.226
	1.2	0.2	0.21	0.2
(phase set 5,6,8)	1.0	0.0588	0.0542	0.113
	1.6	**0.125**	**0.129**	**0.118**
	2.0	0.115	0.078	0.113

Table 4.2 Calculated, Simulated and measured g_{ac}/P_{diss} (Continued)

Structure	V_{bias}(V)	Calculated g_{ac}/P_{diss}	Simulated g_{ac}/P_{diss}	Experimental g_{ac}/P_{diss}
Four-MOS unbalanced (phase set 1)	1.4	0.132	0.164	0.037
	1.6	**0.154**	**0.177**	**0.144**
	1.8	0.147	0.161	0.143
(phase set 2)	1.5	0.165	0.166	0.198
	1.6	**0.167**	**0.167**	**0.201**
	1.8	0.164	0.164	**0.204**
(phase set 2)	2.0	0.162	0.158	0.202
(phase set 3)	**1.0**	**0.414**	**0.486**	**0.446**
	1.1	0.279	0.303	0.402
	1.2	0.172	0.167	0.352
(phase set 4,5,6)	1.2	0.214	0.228	0.214
	1.3	**0.2148**	**0.2294**	0.217
	1.4	0.212	0.227	**0.221**
	1.5	0.207	0.219	0.220
(phase set 7)	2.0	0.055	0.056	0.079
	2.2	0.058	0.058	**0.0806**
	2.4	**0.06006**	**0.0589**	0.0805
	2.5	0.06004	0.0585	-
(phase set 8,9)	1.2	0.15	0.1568	-
	1.4	**0.1556**	**0.163**	0.17
	1.6	0.1538	0.16	**0.175**
	1.8	0.147	0.152	0.117
Two-MOS source-biased	1.9	0.189	0.184	0.197
	2.0	**0.191**	**0.1855**	**0.2**
	2.1	0.189	0.182	0.196

Table 4.2 Calculated, Simulated and measured g_{ac}/P_{diss} (Continued)

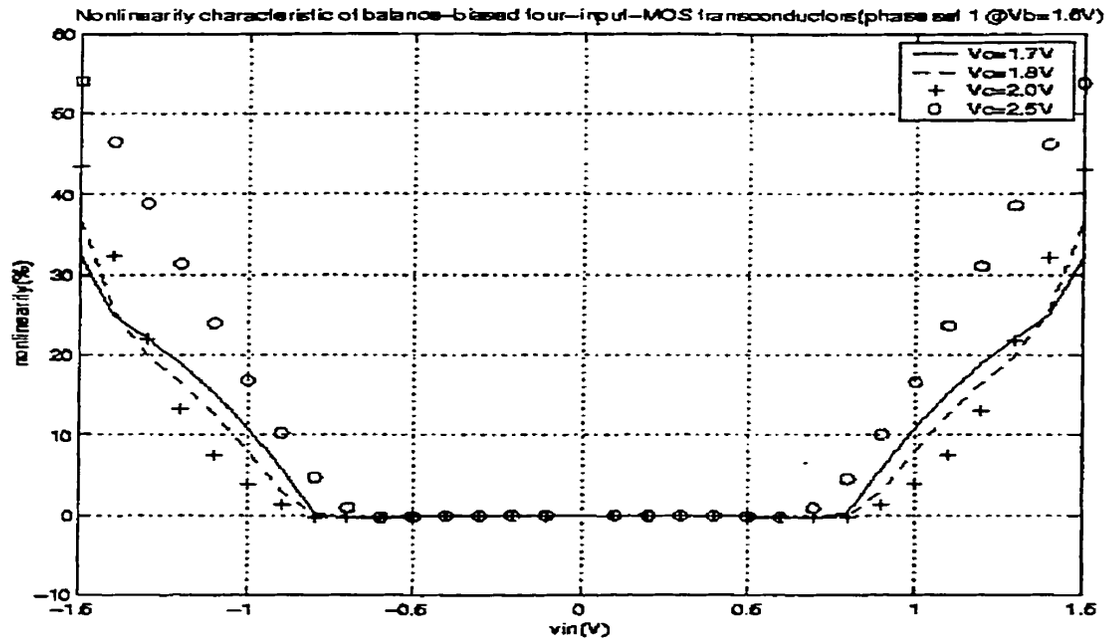
Structure	V_{bias}(V)	Calculated g_{ac}/P_{diss}	Simulated g_{ac}/P_{diss}	Experimental g_{ac}/P_{diss}
Four-MOS source-biased (combination 1,2)	**1.5**	**0.179**	**0.1466**	**0.153**
	1.6	0.162	0.145	0.141
	1.7	0.142	0.123	0.129
Four-MOS source-biased (combination 3)	1.9	0.193	0.184	0.187
	2.0	**0.1944**	**0.1856**	0.1931
	2.1	0.191	0.182	**0.1932**
	2.2	0.185	0.175	0.19
Two-MOS mixed-operating	0.6	0.4	0.45	0.397
	0.7	0.444	0.52	0.412
	0.8	**0.5**	**0.52**	**0.435**
Four-MOS mixed-operating (Fig.3.7)	0.6	0.4	0.34	0.492
	0.7	0.444	0.412	0.5
	0.8	**0.5**	**0.514**	**0.504**
Four-MOS mixed-operating(Fig.3.8)	0.6	0.226	0.244	0.246
	0.7	0.236	0.26	0.248
	0.8	**0.25**	**0.26**	**0.25**

4.4 Linearity characteristics

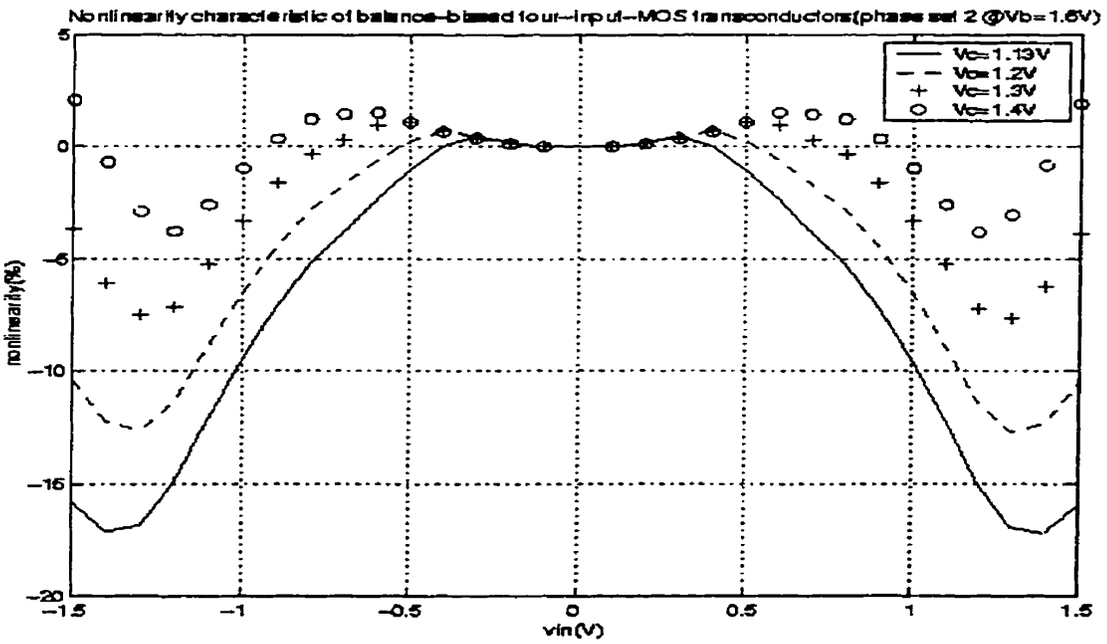
An important characteristic of transconductors is the range of linear operation. The linear range of a transconductor is strongly dependent on the operating point, which is determined by the biasing conditions, of the transconductor. Only when the transconductors are biased properly, they offer linear operation over wider range of the ac input signals. Since the frequency-power-efficiency optimization of a transconductor is achieved by adjusting the bias voltages, the linearity characteristic of the transconductor is unavoidably affected by the adjustment. If the transconductor which is biased optimally in terms of its g_{ac}/P_{diss}

ratio also has acceptable linearity characteristic, one should always try using the optimal biases for the design. However, if the optimal biases could not meet the linearity requirement, one should try using the bias condition which can satisfy the linearity requirement and also provide higher g_{ac}/P_{diss} ratio. Fig. 4.2 illustrates the simulated linearity performance of balance-biased four-input-MOS transconductor structures. The x-axis is the large signal input voltage. The curves with different symbols (solid line, dash line, etc.) correspond to different bias voltage values (given by the legends). The y-axes of Fig. 4.2(a)-(d) depict the percentage nonlinearity. In Fig. 4.1(a), the solid line represents the bias condition at which optimal g_{ac}/P_{diss} can be obtained. One can see that the input range in which the nonlinearity is less than 2% at this bias condition is very small.

Fig. 4.1(a) also reveals that the linearity of the balance-biased four-input-MOS transconductor with phase set 1 is degrading as V_c increases. The best linearity happens at $V_c=2.0V$ (the curve represented by the circles). We have known from previous sections that smaller V_c corresponds to higher g_{ac}/P_{diss}. In order to obtain higher g_{ac}/P_{diss} as well as meet the linearity requirement, one can choose the smallest V_c from the bias voltages which can provide desired linearity for the transconductor . For example, if 1% nonlinearity is acceptable for input signal range of $(-0.8V, 0.8V)$. It can be seen from Fig. 4.2(a) that $V_c=1.8V$ is the lowest bias voltage which meets the requirement. Since for four MOS gate-biased transconductor with ac phase set 1, the g_{ac}/P_{diss} increases as bias voltage decreases. Thus $V_c=1.8V$ is the best bias voltage among the voltages which can provide desired linearity. The solid lines in Fig. 4.2(b),(c) and the thick solid line in Fig. 4.2(d) represent the optimal bias condition of these three phase groups respectively. By inspecting the graphs, the bias voltages which lead to better linearity in figures 4.2(b) to (d) are $1.4V, 0.85V$ and $1.6V$ respectively.



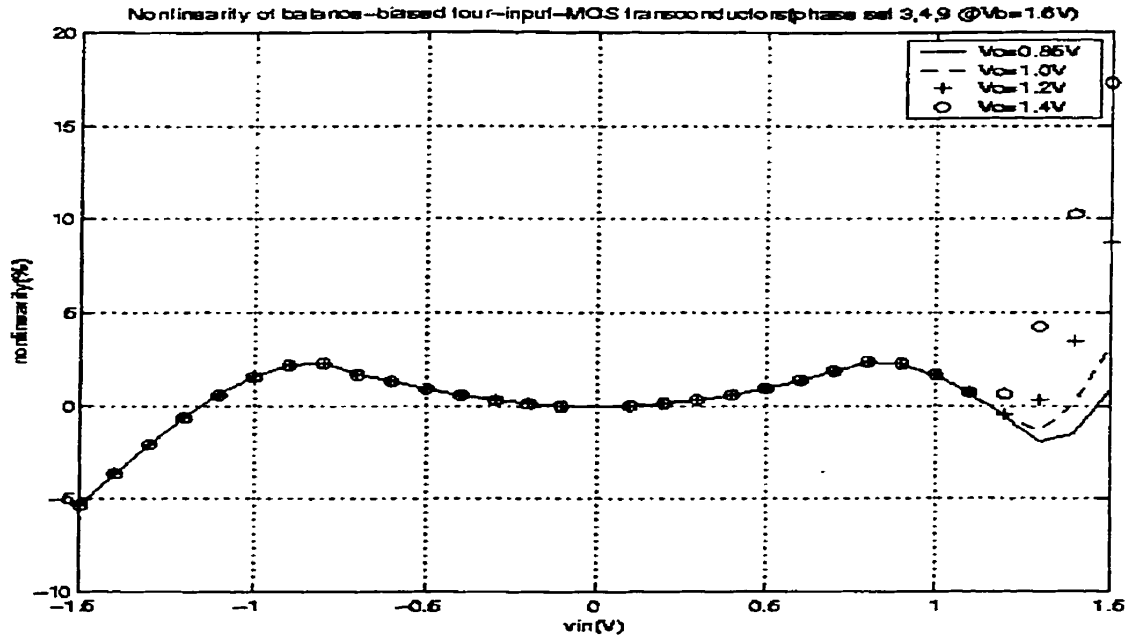
(a) Phase set 1



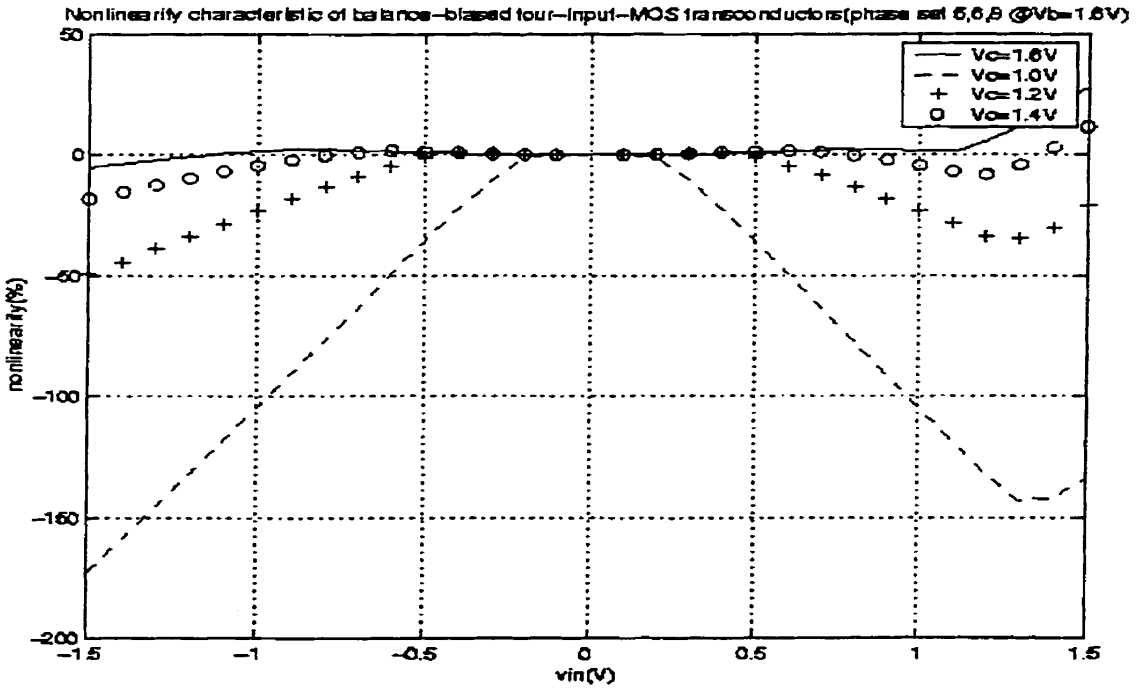
(b) Phase set 2

Fig. 4.2 Linearity characteristic of balance-biased four-input-MOS transconductors

(a) percentage nonlinearity of ac phase set 1 (b) percentage nonlinearity of ac phase set 2
(c) percentage nonlinearity of ac phase sets 3,4 and 9
(d) perentage nonlinearity of ac phase sets 5,6 and 8



(c) Phase set 3, 4 and 9



(d) Phase set 5, 6 and 8

Fig.4.2 Linearity characteristic of balance-biased four-input-MOS transconductors

(a) percentage nonlinearity of ac phase set 1 (b) percentage nonlinearity of ac phase set 2

(c) percentage nonlinearity of ac phase sets 3,4 and 9

(d) perentage nonlinearity of ac phase sets 5,6 and 8 (Cont'd)

If the required linearity is 1% in the input range (-1V,1V), one can see that the balance-biased four-input-MOS transconductor with phase sets 2 to 9 can meet this requirement at their respective optimal bias condition. Thus, by biasing these transconductors at their optimal voltages, the desired linearity performance and the highest g_{ac}/P_{diss} ratio can be achieved at the same time.

Table 4.3 presents the simulated input linear ranges and the total harmonic distortions for all the transconductor structures discussed in Chapter 3. Each transconductor is biased at the optimal condition so that highest g_{ac}/P_{diss} can be obtained. Consistent to what we have observed in Fig. 4.2, the phase sets 2 to 9 of balance-biased four-input-MOS transconductor provide wider linear ranges and less total harmonic distortions, (see Table 4.3). By studying Table 4.3, it is noticed that unbalance-biased structures generally have poorer linearity compared to the balance-biased counterparts. This will be discussed further in Chapter 5.

4.5 Experimental Measurements

4.5.1 The structure of the test Chip

The results given in Table 4.2 showed that the theoretical predictions of the optimal g_{ac}/P_{diss} comply very well with the values obtained from HSPICE simulation. However, although the transistor models and process parameters used in HSPICE (level=3) are based on empirical measurements, they are not exactly the same as those of a physical device. Therefore, the only way to prove that the analyses we have done so far are effective is to physically implement the transconductor structures we have studied in previous sections and measure their g_{ac}/P_{diss} characteristics experimentally to obtain the relation between the bias voltages and the g_{ac}/P_{diss} ratios.

Table 4.3 Linearity characteristic of optimally biased transconductor structures

Transconductor	Linear Range(2% nonlinearity)	Linear Range(5% nonlinearity)
Two-MOS	balanced : -1V ~ 1V unbalanced: -1V ~ 0.3V	balanced : -1.4V ~ 1.4V unbalanced: -1.1V ~ 0.2V
Four-MOS **(B.1- balance** **B.2-unbalance)**	B1 set 1 : -0.16V ~ 0.16V B1 set 2 : -0.6 V ~ 0.6 V B1 set 3,4,9: -1.1 V ~ 1.1 V B1 set 5,6,8 : -1.1 V ~ 1.1 V B2 set 1 : -0.5 V ~ 0.1 V B2 set 2 : -0.7V ~ -0.96V B2 set 3 : -0.4 V ~ 0.4 V B2 set 4: -0.4 V ~ 0.2 V B2 set 5 : -0.2 V ~ 0.1 V B2 set 6 : -0.1 V ~ 0.1 V B2. set 7: -0.2 V ~ 0.2 V B2 set 8 : -0.2 V ~ 0.2 V B2 set 9: -0.5 V ~ 0.2 V	B1 set 1 : -0.3V ~ 0.3V B1 set 2 : -0.8 V ~ 0.7 V B1 set 3,4,9: -1.4 V ~ 1.5 V B1 set 5,6,8 : -1.4 V ~ 1.5 V B2 set 1 : -0.5 V ~ 0.1 V B2 set 2 : -0.7V ~ 0.1V B2 set 3 : -0.2 V ~ 0.4 V B2 set 4: -0.3V ~ 0.1 V B2 set 5 : -0.3 V ~ 0.1 V B2 set 6 : -0.3 V ~ 0.1 V B2. set 7: -0.1 V ~ 0.1 V B2 set 8 : -0.3 V ~ 0.1 V B2 set 9: -0.3 V ~ 0.1 V
Drain/Source-biased **(1,2,3 represents combinations 1,2 and 3)**	two-MOS : -0.3 V ~ 0.7V four-MOS 1, 2 : - 0.6 V ~ 0.6 V four-MOS 3 : -0.3 V ~ 0.3 V	two-MOS : -1.5 V ~ 0.8V four-MOS 1, 2 : - 0.1 V ~ 0.2 V four-MOS 3 : -0.6 V ~ 0.8 V
Mixed-operating	Fig.3.7: -0.1V ~ 0.1V Fig.3.8: -0.2V ~ 0.2V	Fig.3.7: -0.4V ~ 0V Fig.3.8: -0.7V ~ 0.6V

Due to the above reason, a test chip was designed and fabricated using Mitel 1.5 μm CMOS technology. By using the same technology as that of the HSPICE simulation, the test results can be compared with the simulation results directly.

The test chip consists of three current mirrors and six NMOS and PMOS transistors as shown in Fig. 4.3. All the six NMOS transistors and the six PMOS transistors are sized identically.

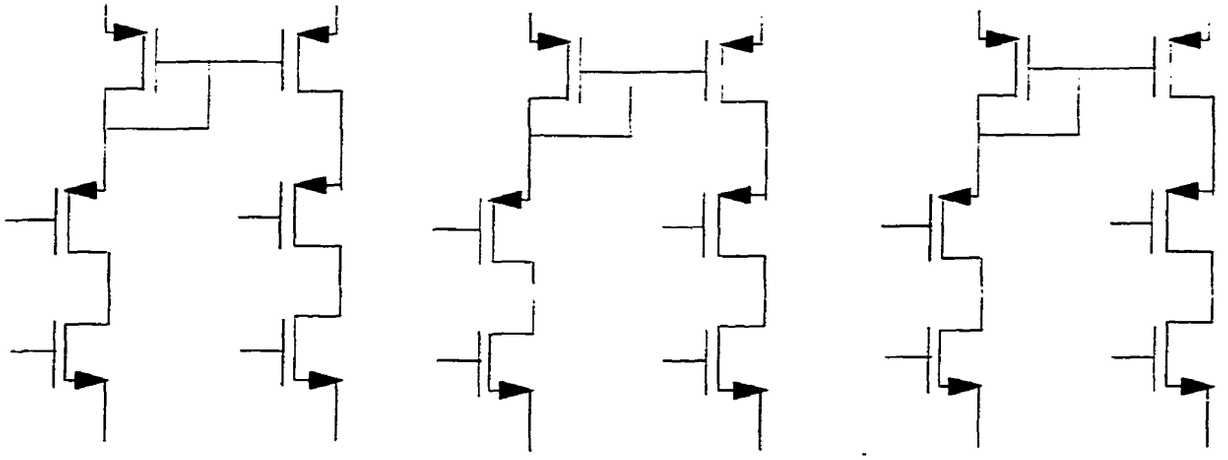


Fig. 4.3 Schematic of the test chip

Employing the structure of Fig. 4.3 makes the design very compact and hence less pins can be used. However, a performance issue comes up with the structure. That is the body effect of the PMOS transistor pairs. Since 1.5 μm Mitel CMOS is P-well technology, all PMOS transistors share the common n-substrate which must be connected to the highest potential of the circuit. For the structure of Fig. 4.3, if both current mirror and the PMOS pair underneath are needed in a transconductor circuit, the body effect of the PMOS pair must be taken into account. We will try to avoid body effect when implementing the transconductors. But if it is unavoidable, we will take that into consideration while comparing with the simulation results.

The structure of Fig. 4.3 has thirty-six terminals in total. Using a forty pin DIP package, each of the thirty-six terminals can be connected to a pin and hence can be externally controlled. Two of the extra four pins are used for positive and negative power supply (i.e., V_{dd} and V_{ss}). The other two pins are floating. The layout of the test chip is shown in Fig. 4.4.

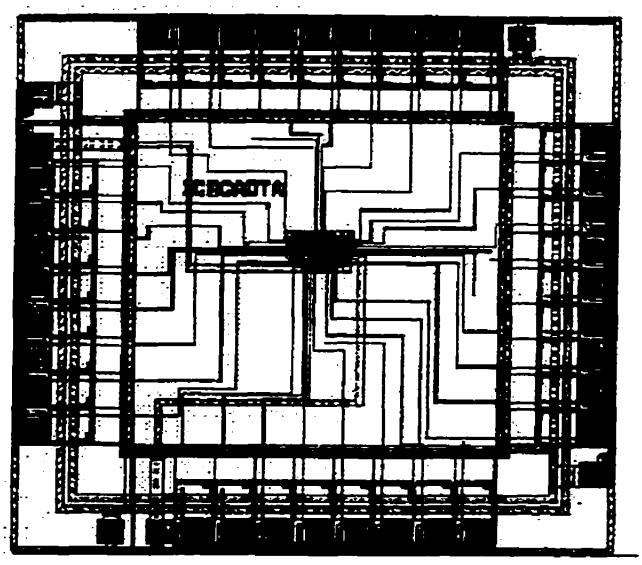


Fig. 4.4 Layout of the test chip (3008x3008micron^2)

4.5.2 Experimental results of g_{ac}/P_{diss} Optimization

Using the structure of Fig. 4.3, different transconductor structures can be implemented by changing the connection among the pins. The bias voltages employed in the experiments and the corresponding g_{ac}/P_{diss} values obtained from the measurements for different transconductors are presented in Table 4.2. The bias voltages are chosen to be close to those used in the calculations and the simulations.

Comparing the experimental results in Table 4.2 with the calculation and simulation results, the experimental optimal bias conditions and g_{ac}/P_{diss}s of most transconductor structures are within ± *10%* range of the values predicted by the calculation and simulation. Larger disparities (>± *10%*) happened for the structures which have near threshold optimal bias voltage and the structures which are highly unbalanced. When being biased at near threshold voltage, the transistor works at the margin of saturation and weakly inversion regions. A small threshold voltage variation will make the transistor move from one operation region to another. Since both calculation and simulation are based on the saturated operating transistor model, if the transistor actually operates in weakly inversion

region, its physical g_{ac}/P_{diss} will be much different from the predicted values. For highly unbalanced structures, more distortion terms will be presented in the g_{ac} and P_{diss} expressions (see Chapter 5). These terms are not included in the .AC analysis of the simulations. But they do appear in the measured results because the measured values are transient values which are obtained by inputing a sinusoid signal to the structures.

4.5.3 Experimental results of the linearity characteristics for optimally biased transconductors

The linearity performance of the transconductor structures of interest have been studied as well. The assumptions given in Table 4.1 are employed while conducting measurements. The linear ranges obtained from the experiments are also given in Table 4.3. Comparing the simulated linearity characteristic and the experimental results, one can see that for input signals in the range of less than 2% simulated nonlinearity, the measured nonlinearity is less than 5%. This degradation of the linearity is because of the process and environment variations, the systematic errors of the equipments and human errors of the measurements.

4.6 Summary

In this chapter, numerical calculations, HSPICE simulations and experimental measurements have been conducted to quantitatively study the g_{ac}/P_{diss} and linearity characteristics of various CMOS transconductor structures. The results obtained in this chapter proved that the frequency-power efficiency optimization methodology for CMOS transconductor structures is effective. However, when considering the feasibility of the analytical optimal results, the linearity performance of a transconductor needs to be taken into account. If linearity performance is used as a constraint for the g_{ac}/P_{diss} optimization, the optimization results, if exist, will automatically satisfy the linearity requirements. The case of constrained optimization will be studied in Chapters 5 and 6.

Chapter 5

Transconductor Frequency-Power Efficiency optimization II: Constrained multivariable Optimization

The objective functions (i.e., g_{ac}/P_{diss}) we have obtained in Chapter 3 are based on the assumptions that the MOS transistors of the same type are perfectly matched and their operations can be effectively described by the first order transistor models. However, in order to describe a transconductor's performance precisely, second order factors such as transistor mismatches, channel length modulation, mobility reduction and body effect should be taken into consideration. The body effect of a transistor is usually because of the potential difference between its source and substrate terminals. Such effect can be avoided by connecting the source and substrate terminals of a transistor to the same potential point. This design technique can easily be achieved using modern semiconductor technology and hence the subsequent discussions will not include body effect. In the following, we are going to review the g_{ac}/P_{diss} functions of CMOS transconductors using more accurate transistor models, which consider important second order effects, and then perform the optimization on the revised g_{ac}/P_{diss} functions.

5.1 Second order factors of MOS transistors

5.1.1 Mobility reduction (μ_{eff})

The mobility of carriers in the channel of a MOS transistor decreases as the carriers' velocity approaches the saturation value limited by scattering. The empirical expression of the effective mobility of a transistor is given by [5]

$$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_{GS} - V_{th})} \tag{5.1}$$

where μ_0 is the low field bulk mobility, θ is mobility degradation factor, V_{GS} is the gate-source voltage of the transistor.

5.1.2 Channel length modulation (λ)

The channel length modulation of a MOS transistor is represented by a parameter λ. If λ is nonzero, the drain current I_D will rely on the drain-source voltage V_{DS} by a factor of $1 + \lambda V_{DS}$. The voltage-to-current transfer characteristics of a saturated MOS transistor can be expressed as

$$I_D = (\mu C_{ox} W/2L)(v_{GS} - V_{th})^2(1 + \lambda V_{DS}) \qquad V_{GS} > V_{th} \text{ and } V_{DS} \geq V_{GS} - V_{th} \tag{5.2}$$

where $v_{GS} = V_{GS} + v_{gs}$, is the instantenous gate-source voltage.

5.1.3 Mismatch (ΔV_{th} and ΔK)

The analyses in Chapter 3 were based on the assumption that transistors of the same type are perfectly matched. In fact, no two transistors can be exactly the same after being physically implemented. The mask layout of transistors can be designed to have the same sizes, but when physical fabrication process is concerned, different location on a wafer and different surroundings of other devices will result in different environment parameters of transistors and further will lead to various mismatches among transistors. Even though particular layout design technique can be employed to make the environment of matched transistors as identical as possible, random process variation can also cause parameter mismatch among transistors. The two important transistor mismatches are threshold voltage mismatch and K mismatch.

Taking the two mismatches into consideration, the current-voltage relation of a MOS transistor in saturation or in linear operating region can be expressed as

$$I_D = (K \pm \Delta K)(v_{GS} - V_{th} \pm \Delta V_{th})^2 \qquad V_{GS} > V_{th} \text{ and } V_{DS} \geq V_{GS} - V_{th} \tag{5.3}$$

$$I_D = (K \pm \Delta K)(V_{GS} - V_{th} \pm \Delta V_{th} - V_{DS}/2)V_{DS} \qquad V_{GS} > V_{th} \text{ and } V_{DS} < V_{GS} - V_{th} \tag{5.4}$$

where $K = \mu C_{ox} W/L$, ΔV_{th} and ΔK represent the threshold mismatch and K mismatch respectively.

Eqns.(5.1)-(5.4) express the three nonideal features of a MOS transistor one at a time. If the three factors are in effect simultaneously, the I-V expression of the transistor can be obtained by combining eqn.(5.1) with (5.3) and (5.2) with (5.4) while replacing μ in the K by μ_{eff} for all equations.

The influence of these nonideal factors on a transconductor structure is the degradation of linear performance. More complicated DC offset and higher order distortions will appear in the expressions of ac transconductances of the transconductors. The following sections will re-analyze transconductor structures discussed in Chapter 3 using the equations (5.1)-(5.4) and derive the analytical formula to describe the linearity of the transconductors. Since each nonideal factor affects the linearity of a transistor independently, the overall distortions in the ac transconductance of a transconductor can be expressed by the root-mean-square of the distortion introduced by each factor. The quantitative linear characteristic can then be used as constraints for g_{ac}/P_{diss} optimization.

5.2 Optimizing g_{ac}/P_{diss} for two-input-MOS transconductors

Let us consider the three nonideal factors one by one and find out their corresponding effects on the I-V equation and the dc power dissipation expression of a transconductor structure.

5.2.1 Gate-biased saturated-operating input-MOS transconductors

Consider Fig. 3.1. The I_{out}-V_{in} equations with each nonideal factor being considered are

given below.

When mobility reduction is in effect,

$$I_{out} = I_1 - I_2 = K\left[\frac{(v_{GS1} - V_{th})^2}{1+\theta(v_{GS1} - V_{th})} - \frac{(v_{GS2} - V_{th})^2}{1-\theta(v_{GS2} - V_{th})}\right] \tag{5.5}$$

$$P_{diss} = K\left[\frac{(V_{GS1} - V_{th})^2}{1+\theta(V_{GS1} - V_{th})} + \frac{(V_{GS2} - V_{th})^2}{1+\theta(V_{GS2} - V_{th})}\right](V_{dd} - V_{ss}) \tag{5.6}$$

where $K = \mu_0 C_{ox}(W/L)$. When $\theta(v_{GS} - V_{th}) < 1$, Taylor series expansion around $\theta(v_{GS1} - V_{th})$ and $\theta(V_{GS2} - V_{th})$ can be used to replace the two terms in the brackets of eqns.(5.5)-(5.6)

$$I_{out} = K[(v_{GS1} - V_{th})^2 - (v_{GS2} - V_{th})^2 - \theta(v_{GS1} - V_{th})^3 + \theta(v_{GS2} - V_{th})^3 \cdot$$

$$+ \theta^2(v_{GS1} - V_{th})^4 - \theta^2(v_{GS2} - V_{th})^4 - \theta^3(v_{GS1} - V_{th})^5 + \theta^3(v_{GS2} - V_{th})^5] \tag{5.7}$$

$$P_{diss} = K[(V_{GS1} - V_{th})^2 + (V_{GS2} - V_{th})^2 - \theta(V_{GS1} - V_{th})^3 - \theta(V_{GS2} - V_{th})^3$$

$$+ \theta^2(V_{GS1} - V_{th})^4 + \theta^2(V_{GS2} - V_{th})^4 - \theta^3(V_{GS1} - V_{th})^5 - \theta^3(V_{GS2} - V_{th})^5](V_{dd} - V_{ss}) \tag{5.8}$$

Where terms up to third order in θ have been retained.

When channel length modulation is considered,

$$I_{out} = K[(v_{GS1} - V_{th})^2 - (v_{GS2} - V_{th})^2] + \lambda K V_{DS1}(v_{GS1} - V_{th})^2\left[1 - \frac{(v_{GS2} - V_{th})^2 V_{DS2}}{(v_{GS1} - V_{th})^2 V_{DS1}}\right] \tag{5.9}$$

$$P_{diss} = K[(V_{GS1} - V_{th})^2 + (V_{GS2} - V_{th})^2] + \lambda K V_{DS1}(V_{GS1} - V_{th})^2\left[1 + \frac{(V_{GS2} - V_{th})^2 V_{DS2}}{(V_{GS1} - V_{th})^2 V_{DS1}}\right](V_{dd} - V_{ss}) \tag{5.10}$$

When mismatches are considered, assuming $V_{th1} = V_{th} + \Delta V$, $V_{th2} = V_{th} - \Delta V$ and $K_1 = K + \Delta K$, $K_2 = K - \Delta K$

$$I_{out} = K[(v_{GS1} - V_{th} - \Delta V)^2 - (v_{GS2} - V_{th} + \Delta V)^2] + (\Delta K)[(v_{GS1} - V_{th} - \Delta V)^2 + (v_{GS2} - V_{th} - \Delta V)^2] \tag{5.11}$$

$$P_{diss} = [(K + \Delta K)(v_{GS1} - V_{th} - \Delta V)^2 + (K - \Delta K)(v_{GS2} - V_{th} - \Delta V)^2](V_{dd} - V_{ss}) \tag{5.12}$$

In order to quantitatively describe how the linearity is degraded because of the nonideal factors, we need to find out the dc offset, coefficient of the linear term and coefficients of

the second and third order distortion terms for each I_{out} given above. Let $v_{GS1} = V_{GS1} + v_{id}/2$, $v_{GS2} = V_{GS2} - (v_{id}/2)$. The dc offsets and the coefficients are listed in Table 5.1. For balance-biased case, $X_1 = X_2$. All terms of the form $X_1^n - X_2^n$ can be eliminated.

Table 5.1 DC offsets and 1st, 2nd, 3rd order Coefficients of the input signals (Gate-biased Saturated operating structures; $X_1 = V_{GS1} - V_{th}$ $X_2 = V_{GS2} - V_{th}$)

Nonideality	dc offset	1st order	2nd order	3rd order
Mobility reduction	$K_0(X_1^2 - X_2^2)$ $-\theta K_0(X_1^3 - X_2^3)$	$K_0(X_1 + X_2)$ $-K_0\frac{3\theta}{2}(X_1^2 + X_2^2)$	$\frac{-3\theta K_0}{4}(X_1 - X_2)$	$\frac{K_0\theta}{4}$
Channel length modulation	$K(X_1 + X_2)(X_1 - X_2)$ $+\lambda K(V_{DS1}X_1^2 - V_{DS2}X_2^2)$	$K(X_1 + X_2)$ $+\lambda K(X_1 V_{DS1} - X_2 V_{DS2})$	$\frac{\lambda K(V_{DS1} + V_{DS2})}{4}$	0
mismatch	$K(X_1 + X_2)(X_1 - X_2 - 2\Delta V)$ $+\Delta K[(X_1 - \Delta V)^2 + (X_2 - \Delta V)^2]$	$(K + \Delta K)(X_1 + X_2)$	$\frac{\Delta K}{2}$	0

Using long-channel transistors and properly laying out the matched transistors, the nonlinearity of a transconductor will mainly come from mobility reduction. If short-channel transistors are employed, all three nonideal factors become significant. Analysis have shown [5] that the square-law and linear models which were developed from long-channel transistors are inaccurate for short-channel transistors. However, as long as analytical models of transistors are existent, the idea and methodology of optimizing frequency-power ratio of CMOS transconductors will still be valid. Certainly, the optimal values obtained will vary for different transistor models.

Since our primary concern is the effectiveness of the frequency-power ratio optimization methodology, it is reasonable to use the well-understood long-channel transistor models initially and then extend the analysis toward complicated short-channel transistor cases. Short-channel effects will be briefly discussed in Chapter 8.

From Table 5.1, one can see that the dc offset and second order distortion of balance-biased structure are much smaller than unbalance-biased structure. This phenomenon has also been clearly shown in the simulation results in Chapter 4. To reduce (or eliminate) the dc offset of the unbalance-biased structure, usually, an identical unbalance-biased structure is used. The ac input phases of the second structure are opposite to those of the original structure. This modification results in the phase set 2 of four-input-MOS gate-biased transconductor structure and will be discussed later. Two-input-MOS unbalance-biased transconductor is rarely used because of its poor linearity. We only use it as a sample for the multivariable constrained optimization.

Generally, for two-input-MOS transconductors, the frequency-power efficiency optimization problem can be modeled as follows:

$$max \quad f(X_1, X_2)$$

subject to: $VUB > X_1, X_2 > VLB$

$$max(Coef(2nd)v/Coef(1st), Coef(3rd)v^2/Coef(1st)) < n\% \qquad (5.13)$$

where $f(X_1, X_2) = Coef(1st)/P_{diss}$, $Coef(1st)$, $Coef(2nd)$ and $Coef(3rd)$ are the coefficients of linear term, second and third order distortions respectively, VLB and VUB are the lower and upper bound respectively, $n\%$ is desired percentage nonlinearity. Setting the upper and lower bounds are necessary because the transconductor will not function properly when the input biases are out of these bounds .

Assuming the channels of the transistors are long enough (six times minimum feature size) and mismatches among same type transistors are tolerable, the nonlinear terms introduced by channel length modulation and transistor mismatches can be neglected. Since θ is usually very small (i.e., <0.1) , we can further ignore second and higher order θ terms in eqn.(5.8). Substituting the expressions into (5.13), we obtained

$$max \quad \frac{X_1 + X_2 - ((3\theta)/2)(X_1^2 + X_2^2)}{[X_1^2 + X_2^2 - \theta(X_1^3 + X_2^3)](V_{dd} - V_{ss})}$$

subject to

$$max\left(abs\left(\frac{3\theta(X_1 - X_2)}{4(X_1 + X_2) - 6\theta(X_1^2 + X_2^2)}\right),\ abs\left(\frac{\theta}{4(X_1 + X_2) - 6\theta(X_1^2 + X_2^2)}\right)\right) < n\%$$

$$VUB > X_1, X_2 > VLB$$

It is a complicated nonlinear optimization problem and a Matlab® function has been used to solve the problem.

5.2.2 Drain/Source-biased saturated-operating input-MOS transconductors

This kind of transconductor structures have adjustable source-biased input transistors. If the bulk terminals of the input transistors can not be connected to their corresponding source terminals, the transconductor's linearity will be greatly deteriorated by the body effect of the input transistors. In order to suppress body effect, we should choose proper type of input transistors according to the technology available. Suppose n-well technology is used, the input transistors then should be PMOS. The reason is that the bulk voltage of a PMOS transistor, which is the potential of the corresponding n-well, is controllable and can be set to the same potential as that of the source terminal of the PMOS transistor. Similarly, if p-well technology is used, NMOS input transistors will be preferred. But if a NMOS (PMOS) structure must be used with n-well (p-well) technology, nonlinearity caused by the body effect of each input transistor must be studied carefully. Table 5.2 shows the four nonideal factors and their influence on the output current of the drain/source-biased transconductor structure with p-type input MOS transistors.

Using long channel transistors and employing special layout technique to eliminate body effect as well as restrict the mismatch and channel length modulation to a tolerable range, the transconductor's linearity distortion will be mainly resulted from mobility reduction.

Table 5.2 DC offsets and 1st, 2nd, 3rd order Coefficients of the input signals (Source-biased saturated operating structure; $Y_1 = V_{d1} - V_{c1} - |V_{tp}|$ $Y_2 = V_{d2} - V_{c2} - |V_{tp}|$)

Nonideal factor	DC offset	1st Coeff.	2nd Coeff.	3rd Coeff.
mobility reduction	$K_0(Y_1^2 - Y_2^2)$ $-\theta K_0(Y_1^3 - Y_2^3)$	$-2K_0(Y_1 + Y_2)$ $+3\theta(Y_1^2 + Y_2^2)$	$-3K_0\theta(Y_1 - Y_2)$	$2K_0\theta$
channel length modulation	$K(Y_1 + Y_2)(Y_1 - Y_2)$ $+\lambda K\left(V_{DS1}Y_1^2 - V_{DS2}Y_2^2\right)$	$-K(Y_1 + Y_2)$ $-\lambda K(V_{DS1}Y_1 + V_{DS2}Y_2)$	$\frac{\lambda K}{4}(V_{DS1} - V_{DS2})$	0
mismatch	$K(Y_1 + Y_2)(Y_1 - Y_2 - 2\Delta V)$ $+\Delta K\left[(Y_1 - \Delta V)^2 + (Y_2 - \Delta V)^2\right]$	$-K(Y_1 + Y_2)$ $-\Delta K(Y_2 - Y_1 + 2\Delta V)$	$\frac{\Delta K}{2}$	0
body effect	$K(Y_1' + Y_2')(Y_1' - Y_2')$ where $Y_1' = V_{d1} - V_{c1} - \lvert V_{tp1}\rvert$ $Y_2' = V_{d2} - V_{c2} - \lvert V_{tp2}\rvert$	$-K(Y_1' + Y_2')$	0	0

The objective function and constraints are given as

$$max \quad \frac{-2(Y_1 + Y_2) + 3\theta(Y_1^2 + Y_2^2)}{((Y_1^2 - \theta Y_1^3)(V_{d1} - V_{ss}) + (Y_2^2 - \theta Y_2^3))(V_{d2} - V_{ss})}$$

subject to

$$max\left(\; abs\left(\frac{3\theta(Y_1 - Y_2)}{2(Y_1 + Y_2) - 3\theta(Y_1^2 + Y_2^2)}\right), \; abs\left(\frac{2\theta}{2(Y_1 + Y_2) - 3\theta(Y_1^2 + Y_2^2)}\right)\right) < n\%$$

$$VUB > Y_1, Y_2 > VLB$$

Using sequential quadratic programming to solve the above optimization problem, optimal biasing set (Y_1, Y_2) can be obtained.

5.2.3 Other two-input-MOS transconductor structures

In sections 3.3.3 and 3.3.4 we have discussed another two types of two-input-MOS transconductors. The mixed saturated-triode structure has one input transistor operating in saturation region and another one in linear region. The linearly operating structure has both input transistors work in the linear region. For linearly operating transconductor, even

without considering second order effects, the odd order nonlinear terms exist. These odd order nonlinear terms can be cancelled out by properly connecting two such structures to arrive at the four input-MOS structure. Because of the poor linearity, transconductor with input transistors operating in linear region are rarely used on its own unless nonlinearity is not a serious concern or extra circuits are employed to compensate the nonlinearity. In this section, we will only study the second order effects of mixed saturated-triode transconductor structure and defer the analysis of linearly operating transconductor to the four-input-MOS structure section.

Table 5.3 lists the nonideal factors and their effects on the mixed saturated-triode transconductor. Using p-well CMOS technology, the body effect of a NMOS transistor can be eliminated by connecting the source terminal of the transistor to its bulk terminal.

Table 5.3 DC offsets and 1st, 2nd, 3rd order Coefficients of the input signals ($X = V_{GS} - V_{th}$)

Nonideal	DC offset	1st Coeff.	2nd Coeff.	3rd Coeff.
mobility reduction	$2K_0\left(XV_{ds} - V_{ds}^2/2\right) + K_0\theta V_{ds}^2 X - 2K_0\theta V_{ds} X^2$	$2K_0 V_{ds} + K_0\theta V_{ds}^2 - 4K_0\theta V_{ds} X$	$-2K_0\theta V_{ds}$	0
channel length modulation	$2K\left(XV_{ds} - V_{ds}^2/2\right)(1+\lambda)V_{ds}$	$2KV_{ds}(1+\lambda V_{ds})$	0	0
mismatch	$2(K+\Delta K)\left[(X-\Delta V_{th})V_{ds} - V_{ds}^2/2\right]$	$2(K+\Delta K)V_{ds}$	0	0

The optimization to this transconductor structure can be conducted following similar procedures as we have described in previous sections.

5.3 Optimizing g_{ac}/P_{diss} for four-input-MOS transconductors

Considering second order factors for the input transistors, the output currents and dc power dissipations of four-input-MOS transconductor structures need to be revised. Taking each nonideal factor into account, eqns.(5.1) to (5.4) should be used to replace expressions of I_1

to I_4.

5.3.1 Gate-biased saturated-operating input-MOS transconductors

The diagram of gate-biased saturated-operating transconductor is re-drawn as follows.

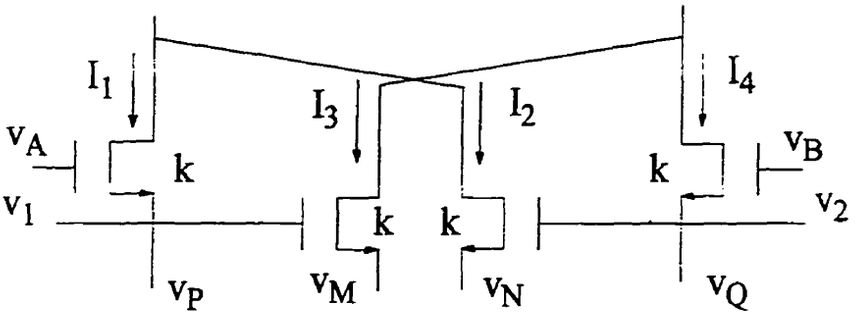


Fig. 5.1 Gate-biased saturated-operating transconductor

When mobility reduction is in effect, we have

$$I_{out} = K_0\left[\frac{(V_{GS1}-V_{th}\pm v_i/2)^2}{1+\theta(V_{GS1}-V_{th}\pm v_i/2)}-\frac{(V_{GS2}-V_{th}\mp v_i/2)^2}{1+\theta(V_{GS2}-V_{th}\mp v_i/2)}+\frac{(V_{GS4}-V_{th}\mp v_i/2)^2}{1+\theta(V_{GS4}-V_{th}\mp v_i/2)}-\frac{(V_{GS3}-V_{th}\pm v_i/2)^2}{1+\theta(V_{GS3}-V_{th}\pm v_i/2)}\right] \quad (5.14)$$

where $K_0 = \mu_0 C_{ox} W/(2L)$.

Using Taylor series to expand eqn.(5.14) around $1+\theta(\ )$ and re-arranging the right side of the equation in the increasing order of ac input signal v_i, the following approximation is obtained

$$I_{out} \cong a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + \ldots \quad (5.15)$$

In eqn.(5.15), $a_0 \ldots a_3$ represent DC offset, coefficients of linear term, 2nd order and 3rd order distortion respectively.

When channel length modulation is considered, the output current can be written as

$$I_{out} = I_{(ideal)} + \lambda K\left[V_{ds1}(V_{GS1}-V_{th}\pm v_i/2)^2 - V_{ds2}(V_{GS2}-V_{th}\mp v_i/2)^2 + V_{ds4}(V_{GS4}-V_{th}\mp v_i/2)^2 - V_{ds3}(V_{GS3}-V_{th}\pm v_i/2)^2\right] \quad (5.16)$$

The mismatch of four-input-MOS structure is complicated compared to two-input-MOS

structure. Consider the two paired transistors (M1,M2) and (M3,M4). Assume the threshold voltages of the two pairs are $V_{th} \pm \Delta V_1$ and $V_{th} \pm \Delta V_2$, the aspect ratios are $K \pm \Delta K_1$ and $K \pm \Delta K_2$, the output current has the expression of

$$\begin{aligned} I_{out} = I_{ideal} &+ 2K[\Delta V_1(V_{GS1} - V_{GS2} \pm v_i) + \Delta V_2(V_{GS4} - V_{GS3} \mp v_i)] \\ &+ \Delta K_1\left[(V_{GS1} - V_{th} - \Delta V_1 \pm v_i/2)^2 + (V_{GS2} - V_{th} + \Delta V_1 \mp v_i/2)^2\right] \\ &- \Delta K_2\left[(V_{GS3} - V_{th} - \Delta V_1 \pm v_i/2)^2 + (V_{GS4} - V_{th} + \Delta V_1 \mp v_i/2)^2\right] \end{aligned} \quad (5.17)$$

Equations (5.16) and (5.17) can also be modified to the form of eqn.(5.15) with different expressions of $a_0 \ldots a_3$.

We have discussed in section 3.4.1 that there are overall 18 ac input phase combinations. Different combination will lead to different $a_0 \ldots a_3$. It is also well-known that unbalance-biased structures will present worse linearity compared to their balance-biased counterparts. This has been clearly shown by the nonlinearity simulation results in Chapter 4. Therefore we will focus on the analysis of balance-biased structures and find out the $a_0 \ldots a_3$ associated with each of the three nonideal factors and tabulate them in Table 5.4. The $a_0 \ldots a_3$ for unbalance-biased structures are given in Appendix B. The V_{DS}s for paired transistors are assumed to be equal in Table 5.4. If they are not equal, the results of channel length modulation need to be revised. As we have mentioned before, through careful layout design, the nonlinearity of a transconductor will mainly result from mobility reduction. Therefore, the assumption we have made will not affect our further analysis on the nonlinear characteristic of transconductors.

The power dissipations for above four phase sets are the same and can be revised from eqn.(3.48) using eqns.(5.1) to (5.4) depending on which non-ideal factor is in effect. Since the dc power dissipation only involves dc variables, its modification is simpler compared to the modifications on the output current expressions of the transconductors. The modified dc power dissipation expressions will be presented in Chapter 6 when numerical simulations are conducted.

Table 5.4 DC offsets and 1st, 2nd, 3rd order Coefficients of the input signals

$(X_1 = V_{GS1} - V_{th},\ X_2 = V_{GS2} - V_{th})$

Phase set	Nonideality	dc offset	1st order	2nd order	3rd order
1	Mobility reduction	0	$2K_0(X_1 - X_2)$ $-3K_0\theta\left(X_1^2 - X_2^2\right)$	0	0
	Channel length modulation	0	$2K(X_1 - X_2)$ $+2\lambda K(X_1 V_{DS1} - X_2 V_{DS2})$	0	0
	mismatch	$-4K(X_1\Delta V_1 - X_2\Delta V_2)$ $+2\Delta K_1\left(X_1^2 + \Delta V_1^2\right) + 2\Delta K_2\left(X_2^2 + \Delta V_2^2\right)$	$2K(X_1 - X_2)$ $-2\Delta K_1\Delta V_1 - 2\Delta K_2\Delta V_2$	$\frac{\Delta K_1 + \Delta K_2}{2}$	0
2	Mobility reduction	0	$2K_0(X_1 + X_2)$ $-3K_0\theta\left(X_1^2 + X_2^2\right)$	0	$\frac{K_0\theta}{2}$
	Channel length modulation	0	$2K(X_1 + X_2)$ $+2\lambda K(X_1 V_{DS1} + X_2 V_{DS2})$	0	0
	mismatch	$-4K(X_1\Delta(V_1 + X_2\Delta V_2)$ $+2\Delta K_1\left(X_1^2 + \Delta V_1^2\right) + 2\Delta K_2\left(X_2^2 - \Delta V_2^2\right)$	$2K(X_1 + X_2)$ $-2\Delta K_1\Delta V_1 - 2\Delta K_2\Delta V_2$	$\frac{\Delta K_1 + \Delta K_2}{2}$	0
3,4,9	Mobility reduction	0	$-2K_0X_2 + 3K_0\theta X_2^2$	0	$\frac{K_0\theta}{4}$
	Channel length modulation	0	$-2K(1 + \lambda V_{DS2})X_2$	0	0
	mismatch	$-4K(X_1\Delta V_1 - X_2\Delta V_2)$ $+2\Delta K_1\left(X_1^2 + \Delta V_1^2\right) + 2\Delta K_2\left(X_2^2 + \Delta V_2^2\right)$	$-2K(X_2 + \Delta V_1)$ $+2\Delta K_1\Delta V_1 - 2\Delta K_2\Delta V_2$	$\frac{\Delta K_1 + \Delta K_2}{2}$	0
5,6,8	Mobility reduction	0	$2K_0X_1 - 3K_0\theta X_1^2$	0	$\frac{K_0\theta}{4}$
	Channel length modulation	0	$2K(1 + \lambda V_{DS2})X_1$	0	0
	mismatch	$-4K(X_1\Delta V_1 - X_2\Delta V_2)$ $+2\Delta K_1\left(X_1^2 + \Delta V_1^2\right) + 2\Delta K_2\left(X_2^2 + \Delta V_2^2\right)$	$2K(X_1 + \Delta V_2)$ $-2\Delta K_1\Delta V_1 + 2\Delta K_2\Delta V_2$	$\frac{\Delta K_1 + \Delta K_2}{2}$	0

Having obtained the analytical formulas to describe the nonlinearity performance, we can derive the objective function and constraints for each phase set and then solve them using

computer programs.

5.3.2 Drain/Source-biased saturated-operating input-MOS transconductors

Table 5.5 lists the dc offsets and coefficients of 1st to 3rd order ac input signal for the three output current expressions in Table 3.4.

Table 5.5 DC offsets and Coefficients of 1st, 2nd, 3rd order input signals for I_{out} of drain/source-biased transconductor ($Y_{11} = V_{d1} - V_{c1} - |V_{tp}|$ $Y_{12} = V_{d1} - V_{c2} - |V_{tp}|$ $Y_{21} = V_{d2} - V_{c1} - |V_{tp}|$ $Y_{22} = V_{d2} - V_{c2} - |V_{tp}|$)

I_{out}	nonideal factor	DC offset	1st Coeff.	2nd Coeff.	3rd Coeff
I_1+I_2 $-I_3-I_4$	mobility reduction	$2K_0(V_{c1}-V_{c2})(V_{d2}-V_{d1})$	$K_0(V_{d1}-V_{d2})(2-3\theta\sum Y)$ $\sum Y = Y_{11}+Y_{12}+Y_{21}+Y_{22}$	0	0
	channel length modulation	$K\left(Y_{11}^2-Y_{12}^2+Y_{22}^3-Y_{21}^3\right)$ $+\lambda KV_{ds1}\left(Y_{11}^2-Y_{21}^2\right)$ $+\lambda KV_{ds2}\left(Y_{22}^2-Y_{12}^2\right)$	$2K(V_{d1}-V_{d2})$ $-\lambda KV_{ds1}(Y_{11}-Y_{21})$ $-\lambda KV_{ds2}(Y_{22}-Y_{12})$	0	0
	mismatch	$2K(V_{d1}-V_{d2}-\Delta V_1-\Delta V_2)$ $\times(Y_{11}-Y_{21}-\Delta V_1+\Delta V_2)$ $+\Delta K_1(Y_{11}+Y_{22})(Y_{11}-Y_{22}-2\Delta V_1)$ $-\Delta K_2(Y_{11}+Y_{22})(Y_{11}-Y_{22}-2\Delta V_1)$	$2K(V_{d1}-V_{d2}-\Delta V_1-\Delta V_2)$ $+\Delta K_1(Y_{11}+Y_{22})$ $-\Delta K_2(Y_{12}+Y_{21})$	0	0
I_1+I_3 $-I_2-I_4$	mobility reduction	$2K_0(Y_{11}+Y_{22})(V_{d1}-V_{d2})$ $-\theta K_0\left(Y_{11}^3-Y_{22}^3+Y_{12}^3-Y_{21}^3\right)$	$2K_0(V_{d1}-V_{d2})$ $-(\frac{3\theta}{2})K_0\left(Y_{11}^2-Y_{22}^2+Y_{12}^2-Y_{21}^2\right)$	$\frac{3\theta}{2}K_0(V_{d1}-V_{d2})$	0
	channel length modulation	$2K(Y_{11}+Y_{22})(V_{d1}-V_{d2})$ $+\lambda KV_{ds1}\left(Y_{11}^2-Y_{21}^2\right)$ $+\lambda KV_{ds2}\left(Y_{12}^2-Y_{22}^2\right)$	$2K(V_{d1}-V_{d2})$ $+\lambda KV_{ds1}(Y_{11}-Y_{21})$ $+\lambda KV_{ds2}(Y_{12}-Y_{22})$	0	0
	mismatch	$2K(V_{d1}-V_{d2}-\Delta V_1-\Delta V_2)(Y_{11}+Y_{22})$ $+\Delta K_1\left[(Y_{11}-\Delta V_1)^2+(Y_{22}-\Delta V_1)^2\right]$ $+\Delta K_2\left[(Y_{12}-\Delta V_2)^2+(Y_{21}-\Delta V_2)^2\right]$	$2K(V_{d1}-V_{d2}-\Delta V_1-\Delta V_2)$ $+\Delta K_1(Y_{11}+Y_{22})$ $-\Delta K_2(Y_{12}+Y_{21})$	$\frac{\Delta K_1-\Delta K_2}{2}$	0

Table 5.5 DC offsets and Coefficients of 1st, 2nd, 3rd order input signals for I_{out} of drain/source-biased transconductor ($Y_{11} = V_{d1} - V_{c1} - |V_{tp}|$ $Y_{12} = V_{d1} - V_{c2} - |V_{tp}|$ $Y_{21} = V_{d2} - V_{c1} - |V_{tp}|$ $Y_{22} = V_{d2} - V_{c2} - |V_{tp}|$)

I_{out}	nonideal factor	DC offset	1st Coeff.	2nd Coeff.	3rd Coeff.
I_1+I_4 $-I_2-I_3$	mobility reduction	$2K_0(Y_{11}+Y_{22})(V_{c2}-V_{c1})$ $-\theta K_0\left(Y_{11}^3 - Y_{22}^3 + Y_{21}^3 - Y_{12}^3\right)$	$2K_0\left[(Y_{11}+Y_{22}) - \frac{3\theta}{2}(Y_{11}Y_{22}+Y_{21}Y_{12})\right]$ $-\left(\frac{3\theta}{2}\right)K_0\left[(Y_{11}-Y_{22})^2+(Y_{21}-Y_{12})^2\right]$	$-\frac{3\theta}{2}K_0(V_{c1}-V_{c2})$	$\frac{K_0\theta}{2}$
	channel length modulation	$2K(Y_{11}+Y_{22})(V_{c2}-V_{c1})$ $+\lambda K V_{ds1}\left(Y_{11}^2+Y_{21}^2\right)$ $-\lambda K V_{ds2}\left(Y_{22}^2+Y_{12}^2\right)$	$2K(Y_{11}+Y_{22})$ $+\lambda K V_{ds1}(Y_{11}+Y_{21})$ $-\lambda K V_{ds2}(Y_{22}-Y_{12})$	$\frac{\lambda K(V_{ds1}-V_{ds2})}{2}$	0
I_1+I_4 $-I_2-I_3$	mismatch	$2K(V_{d1}-V_{d2}-\Delta V_1+\Delta V_2)(Y_{11}+Y_{22})$ $+\Delta K_1\left[(Y_{11}-\Delta V_1)^2+(Y_{22}+\Delta V_1)^2\right]$ $+\Delta K_2\left[(Y_{12}-\Delta V_2)^2+(Y_{21}+\Delta V_2)^2\right]$	$2K(Y_{11}+Y_{22})$ $+\Delta K_1(Y_{11}+Y_{22})$ $-\Delta K_2(Y_{12}+Y_{21})$	$\frac{\Delta K_1-\Delta K_2}{2}$	0

5.3.3 Other four-input-MOS transconductors

Now we consider transconductors with input transistors operating in non-saturation region and both saturation and non-saturation regions. Employing the basic equations of (5.1) to (5.4), the DC offset and coefficients of the output current for mixed saturated-triode input-MOS (Fig. 3.8) transconductor and linearly operating transconductor (Fig. 3.9) are given in Table 5.6. Since Fig. 3.8 and Fig. 3.9 do not have third order distortion term, Table 5.6 only shows the coefficients of second order distortion terms.

Table 5.6 DC offsets and Coefficients of 1st, 2nd, 3rd order input signals for I_{out} of drain/source-biased transconductor($X = V_{GS} - V_{th}$ $X_{1t} = X_1 - V_{th}$ $X_{2t} = X_2 - V_{th}$)

structure	nonideal factor	DC offset	1st coeff.	2nd coeff.
Fig.3.8	mobility reduction	0	$KV_{ds}(2X - 2\theta X + \theta V_{ds}/2)$	0
	channel length modulation	0	$KV_{ds}(1+\lambda V_{ds})$	0
	mismatch	$\Delta K\left(2V_{ds}X - V_{ds}^2\right) - 2KV_{ds}\Delta V$	KV_{ds}	0

Table 5.6 DC offsets and Coefficients of 1st, 2nd, 3rd order input signals for I_{out} of drain/source-biased transconductor($X = V_{GS} - V_{th}$ $X_{1t} = X_1 - V_{th}$ $X_{2t} = X_2 - V_{th}$)

structure	nonideal factor	DC offset	1st coeff.	2nd coeff.
Fig.3.9	mobility reduction	$K_0(Y_1 - Y_2)(X_{m1} - X_{m2})$ $\frac{(Y_1 + Y_2 - 2V)(Y_1 - Y_2)}{2}$ $\times\left(\frac{1}{1+\theta(X_{1t}-V)} - \frac{1}{1+\theta(X_{2t}-V)}\right)$ $X_{m1} = \frac{X_{1t}-V}{1+\theta(X_{1t}-V)}$ $X_{m2} = \frac{X_{2t}-V}{1+\theta(X_{2t}-V)}$	$K_0(X_{m1} - X_{m2})$ $-\left(\frac{1}{1+\theta(X_{1t}-V)} - \frac{1}{1+\theta(X_{2t}-V)}\right)(Y_1 + Y_2 - 2V)$ $X_{m1} = \frac{X_{1t}-V}{1+\theta(X_{1t}-V)}$ $X_{m2} = \frac{X_{2t}-V}{1+\theta(X_{2t}-V)}$	0
Fig.3.9	channel length modulation	$K(X_1 - X_2)(Y_1 - Y_2)$ $\times(1 + \lambda(Y_1 + Y_2 - 2V))$	$K(X_1 - X_2)(1 + \lambda(Y_1 + Y_2 - 2V))$	0
	mismatch	$K(X_1 - X_2 - \Delta V_1 - \Delta V_2)(Y_1 - Y_2)$ $+\Delta K_1(X_{1t} - V)(Y_1 + Y_2 - 2V)$ $+\Delta K_2(X_{2t} - V)(Y_1 + Y_2 - 2V)$ $-(\Delta V_1 \Delta K_1 - \Delta V_2 \Delta K_2)(Y_1 - Y_2)$ $-\frac{1}{2}(\Delta K_1 + \Delta K_2)\left[(Y_1 - V)^2 + (Y_2 - V)^2\right]$	$K(X_1 - X_2) + \Delta K_1(X_{1t} - V) + \Delta K_2(X_{2t} - V)$ $-(\Delta V_1 \Delta K_1 - \Delta V_2 \Delta K_2)$ $-\frac{1}{2}(\Delta K_1 + \Delta K_2)(Y_1 - Y_2)$	$-\frac{1}{4}(\Delta K_1 + \Delta K_2)$

In Chapter 3, we also discussed transconductor structures with eight input transistors. Because of the similarity between four and eight input-MOS transconductors, analytical expressions of DC offsets, linear terms, 2nd and 3rd order distortions for eight input-MOS transconductors can be obtained easily. It will be tedious if we studied all possible eight input-MOS transconductors. So we will omit the detailed analyses on eight-input-MOS transconductors in this thesis. When the analytical details of eight-input-MOS transconductors are needed, they can be obtained following the same procedures as we have been presented for two- and four-input-MOS structures.

5.3.4 Optimization Using MATLAB

Due to the complicity of the multivariable constrained optimization problem, MATLAB programs are created to solve the problems. MATLAB has an Optimization Toolbox which provides tools for both general and large-scale optimization of nonlinear functions. The

Optimization Toolbox contains routines that implement the most widely used methods for performing minimization or maximization. It includes several nonlinear optimization functions. The function that we used is *fmincon*. *fmincon* has two algorithm options for nonlinear constrained optimization problem [34]. One is called large-scale optimization, the other is medium-scale optimization. Large-scale optimization algorithm is applied when the gradient of the objective function is supplied by the user and if only upper and lower bounds exists or only linear constraints exist. Medium-scale algorithm uses Sequential Quadratic Programming (SQP) method. It represents state-of-the-art nonlinear programming method. In SQP method, a Quadratic Programming (QP) subproblem is solved at each iteration. An estimation of the Hessian of the Lagrangian is updated at each iteration using the BFGS formula. SQP has good efficiency, accuracy and higher percentage of successful solutions.

Since the MATLAB® function *fmincon* intends to minimize the objective function whereas our objective function needs to be maximized, we first must modify the objective function to a minimization problem. By simply inverting $\frac{g_{ac}}{P_{diss}}$, the original maximization problem is changed to a minimization problem. It has been known that the ac transconductance of a transconductor (g_{ac}) can be positive or negative and our goal is to maximize the absolute value of $\frac{g_{ac}}{P_{diss}}$. Therefore, $\left(\frac{P_{diss}}{g_{ac}}\right)^2$ is used as the final target objective function for the optimization. The optimization procedures are:

1. Initialize θ, V_{dd}, V_{ss} and n;
2. Define the objective function, constraints;
3. Set upper and lower bounds for the searching space;
4. Set starting point *x(0)* for the search;
5. Call *fmincon* ;
6. If no feasible solution exists for current constraints, increase the acceptable nonlinearity range and repeat 5.
7. If no feasible solution can be obtained even for the maximum acceptable nonlinearity,

the structure is not optimizable when both g_{ac}/P_{diss} and linearity requirements are concerned.

5.4 Summary

Since linearity is a very important design specification of a CMOS transconductor, we can not optimize frequency-power efficiency without considering its influence on the linearity. In order to obtain both good linearity and high frequency-power efficiency, the unconstrained single variable optimization method in the previous Chapters has been modified to a multivariable constrained optimization algorithm in this chapter. The objective function is still g_{ac}/P_{diss}. The constraints are on the second and third order distortions of the transconductor's output current. The result of such kind of optimization, if exists, will be the bias voltages that can provide highest g_{ac}/P_{diss} among all other bias voltages which meet the linearity specification. To formulate the objective function and the constraints, second order effects of two and four input-MOS transconductor structures have been studied in detail and the analytical expressions related to each non-ideal factor have been derived. The optimization problem can be solved employing MATLAB optimization function.

Chapter 6

Simulations and Experiments for frequency-power efficiency optimization II: Constrained Multivariable Optimization

Having studied the non-linear factors of various transconductor categories, we will modify the power efficiency optimization which we have discussed in the previous chapters so that the linearity characteristics can also be included in the optimization methodology. By doing so, the optimal operating condition obtained through the optimization can not only provide higher frequency-power efficiency but also achieve the desired linearity characteristic.

The expressions of the objective function and the constraints of the constrained multivariable optimization scheme have been defined in chapter 5. We have also mentioned that MATLAB programs need to be employed to perform the optimization. In this chapter, we will present the optimization results obtained from executing MATLAB programs.

In addition, experiments are performed to measure transconductors' g_{ac}/P_{diss} s and the linearities. The set up of the experiments and the results obtained will be presented as well.

6.1 MATLAB Optimization Programs

Unlike the single variable optimization of chapter 3, it is not necessary to make assumptions for the bias voltages of a transconductor structure while performing multivariable optimization. All the bias voltages are variables and the searching space of the optimization is *n*-dimension, where *n* is the number of biases of a transconductor structure.

In chapter 5, we have mentioned that the objective function and the constraints of the multivariable optimization problem are pretty complicated. Thus, mathematical tool-MAT-

LAB has to be employed to solve the problem. Using MATLAB optimization function, the program of gate-biased two-input MOS transconductor optimization (mos2_ub.m) is presented as an example in Appendix C.

In mos2_ub.m, the mobility reduction factor is assumed to be $\theta = 0.041$. It is a process dependent parameter, the smaller the minimum feature size of a technology, the higher θ will be. For example, $\theta_n = 0.041$, $\theta_p = 0.1$ for a $1.5\mu m$ CMOS technology; $\theta_n = 0.26$, $\theta_p = 0.18$ for a 0.5 μm CMOS technology. Since we have used a 1.5 μm CMOS technology for the simulations and experiments in Chapter 4, we are going to stay with the same technology for the simulations and experiments in this chapter so that the results obtained in these two chapters are comparable.

The objective function in mos2_ub.m is $(P_{diss}/g_{ac})^2$. This is because that the optimization provided by MATLAB is to minimize an objective function. Maximizing g_{ac}/P_{diss}, which is the goal of our optimization, can be implemented by minimizing its inverse function (i.e., P_{diss}/g_{ac}). However, g_{ac}/P_{diss} can be positive or negative and our concern is its absolute value, so we took $(P_{diss}/g_{ac})^2$ as our objective function. There are two nonlinear constraints are used for the optimization. One of them is the coefficient of the second-order nonlinear term over the coefficient of linear term ratio, named DIS2. The other one is the coefficient of the third-order nonlinear term over the coefficient of linear term ratio, named DIS3. Since both ac transconductance and DC power dissipation can not be zero, the optimization program also performs feasibility check once a solution is reached. If the solution obtained is acceptable, it will be printed out. Otherwise, the information of why the result is infeasible will be explained briefly.

The program also includes a part to modify the constraints to some extent. The initial constraints for both distortions are 1%. If no optimal result comes out, the constraints will be adjusted to 2% and the optimization will be repeated. If no feasible optimal result can be achieved even when the percentage nonlinearity is set to its highest acceptable value, the transconductor will be regarded as non-optimizable when both distortion and g_{ac}/P_{diss} are

considered together. Similar programs can be written for other transconductor structures.

6.2 g_{ac}/P_{diss} results obtained from analytical calculations, HSPICE simulations and experimental measurements

Analytical results can be obtained through running MATLAB optimization programs. Take two-MOS gate-biased transconductor as an example. After executing the program in section 6.1, the analytical results are presented and explained as follows.

Result of PART ONE : Theoretical graph of the objective function. (not including the constraints).

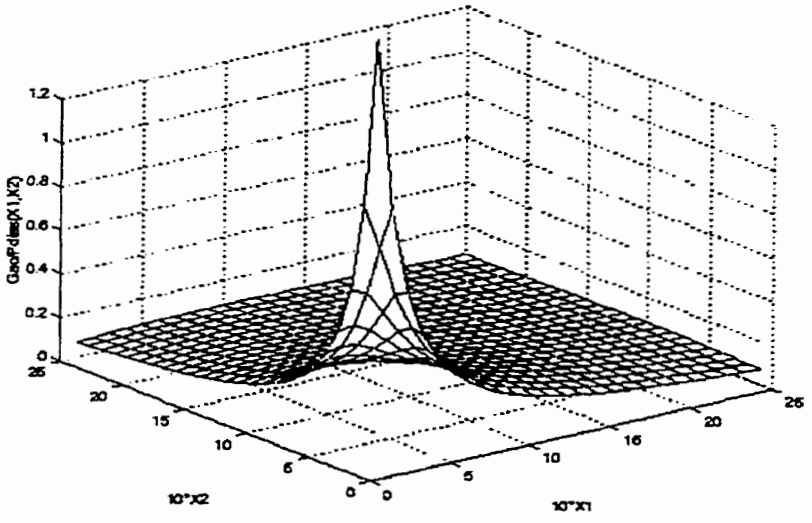


Fig. 6.1 Theoretical g_{ac}/P_{diss} graph of Two-input-MOS transconductor

From Fig.6.1, one can see that it is a 2-D function. $X_1 = V_{GS1} - V_{th}$, $X_2 = V_{GS2} - V_{th}$. Both X_1 and X_2 are in the range of [0 2.5]. Without constraints, the g_{ac}/P_{diss} of two-MOS gate-biased transconductor is monotonically decreasing when X_1 and X_2 are increasing.

Results obtained from PART TWO and PART THREE : Optimization process and results.

terminate successfully

x =

0.7686 0.4352

```
fout =
   0.3044
iter_num =
   50
cu =
  1.0e-07 *
   0.4716   0.0000
cueq =
   []
n =
   0.0100
```

The above results show that the optimal biases are V_{GS1}-V_{th}=*0.7686V*, V_{GS2}-V_{th}=*0.4352V*. The optimal g_{ac}/P_{diss} equals to 0.3044. The second order distortion (DIS2)=*0.4716e-07*, the third order distortion (DIS3)=*0*.

Following similar procedures, the analytical optimization results for other transconductor structures are obtained and listed in the third column of Table 6.1.

Using the analytical optimal bias voltages obtained from MATLAB programs, HSPICE netlists are created for each transconductor structure. The simulated g_{ac}/P_{diss}s are presented in the fourth column of Table 6.1.

To physically evaluate the optimization scheme, the test chip which was described in chapter 4 (see layout of Fig. 4.4) is measured. The g_{ac}/P_{diss} of the transconductors biased by the optimal voltages obtained through the optimization programs are obtained and given in the last column of Table 6.1. The set up of the testing circuits are shown in Appendix C.

In Table 6.1, for each transconductor structure, the upper rows in columns 2 and 3 are the optimal bias condition and the g_{ac}/P_{diss} ratios obtained from single variable unconstrained optimization(chapter 4), while the lower rows present the same quantities obtained from multivariable constrained optimization. It can be seen from Table 6.1 that the three optimal g_{ac}/P_{diss} ratios, that is, analytical, simulated and measured g_{ac}/P_{diss} ratios, are consistent to each other for most structures except for the structures which have near threshold opti-

mal bias voltages and the structures which are highly unbalanced. The reason of high disparity between simulated and experimental results for these two cases have been addressed in section 4.

Table 6.1 Calculated and Simulated (g_{ac}/P_{diss})s at Single variable optimums and Multivariable Optimums

Structure	V_{bias}s(V)	Calculated g_{ac}/P_{diss}	Simulated g_{ac}/P_{diss}	Measured g_{ac}/P_{diss}
Four-MOS balanced (phase set 1)	V_{GS1}=0.85 V_{GS2}=1.6	0.25	0.257	0.259
	V_{GS1}=0.9 V_{GS2}=0.85	3.406	3.029	3.25
(phase set 2)	V_{GS1}=1.13 V_{GS2}=1.6	0.301	0.314	0.295
	V_{GS1}=1.376 V_{GS2}=1.376	0.3733	0.3719	0.3642
(phase set 3,4,9)	V_{GS1}=0.9 V_{GS2}=1.6	0.246	0.257	0.236
	V_{GS1}=0.85 V_{GS2}=1.37	0.3732	0.374	0.35
(phase set 5,6,8)	V_{GS1}=1.6 V_{GS2}=1.6	0.125	0.129	0.118
	V_{GS1}=1.37 V_{GS2}=0.85	0.3732	0.374	0.35
Four-MOS unbalanced (phase set 1)	V_{GS1}=1.6 V_{GS2}=1.28 V_{GS3}=1.2 V_{GS4}=0.88	0.154	0.177	0.144
	V_{GS1}=0.856 V_{GS2}=0.856 V_{GS3}=1.013 V_{GS4}=0.8676	1.1767	1.003	0.8545
(phase set 2)	V_{GS1}=1.6 V_{GS2}=1.2 V_{GS3}=2.0 V_{GS4}=2.4	0.167	0.167	0.204
	V_{GS1}=1.376 V_{GS2}=1.376 V_{GS3}=1.376 V_{GS4}=1.376	0.3733	0.3719	0.3642
(phase set 3)	V_{GS1}=1.0 V_{GS2}=0.96 V_{GS3}=0.96 V_{GS4}=1.2	0.414	0.486	0.446
	V_{GS1}=0.856 V_{GS2}=1.2 V_{GS3}=1.2 V_{GS4}=1.2	0.5573	0.5533	0.5412

Table 6.1 Calculated and Simulated (g_{ac}/P_{diss})s at Single variable optimums and Multivariable Optimums

Structure	V_{bias}s(V)	Calculated g_{ac}/P_{diss}	Simulated g_{ac}/P_{diss}	Measured g_{ac}/P_{diss}
(phase set 4,5,6)	V_{GS1}=1.26 V_{GS2}=1.2 V_{GS3}=1.2 V_{GS4}=1.6	0.215	0.2297	0.221
	(set 4) V_{GS1}=1.07 V_{GS2}=0.856 V_{GS3}=1.20 V_{GS4}=1.07 (set 5) V_{GS1}=1.07 V_{GS2}=1.2 V_{GS3}=0.856 V_{GS4}=1.07 (set 6) V_{GS1}=1.07 V_{GS2}=1.07 V_{GS3}=1.2 V_{GS4}=0.856	0.739	0.694	0.7046
(phase set 7)	V_{GS1}=2.4 V_{GS2}=1.6 V_{GS3}=1.6 V_{GS4}=1.2	0.06	0.0589	0.0806
	V_{GS1}=2.8 V_{GS2}=0.856 V_{GS3}=2.8 V_{GS4}=0.856 *	0.095	0.095	0.0723
(phase set 8,9)	(set 8) V_{GS1}=1.4 V_{GS2}=1.6 V_{GS3}=1.2 V_{GS4}=1.6 (set 9) V_{GS1}=1.4 V_{GS2}=1.2 V_{GS3}=1.6 V_{GS4}=1.6	0.1556	0.163	0.175
	(set 8) V_{GS1}=2.5 V_{GS2}=2.5 V_{GS3}=0.856 V_{GS4}=0.856 (set 9) V_{GS1}=0.856 V_{GS2}=0.856 V_{GS3}=2.5 V_{GS4}=2.5	0.1165	0.1151	0.0938
Two-MOS source-biased	V_{d1}=2.0 V_{d2}=2.5 V_{c1}=V_{c2}=0.5 V_{ss}=-2.5	0.1916	0.1855	0.2
	NA			
Four-MOS source-biased (combination 1,2)	V_{d1}=1.5 V_{d2}=2.5 V_{c1}=V_{c2}=0.5 V_{ss}=-2.5	0.179	0.1466	0.153
	NA			

Table 6.1 Calculated and Simulated (g_{ac}/P_{diss})s at Single variable optimums and Multivariable Optimums (Cont'd)

Structure	V_{bias}s(V)	Calculated g_{ac}/P_{diss}	Simulated g_{ac}/P_{diss}	Measured g_{ac}/P_{diss}
Four-MOS source-biased (combination 3)	V_{d1}=2.0 V_{d2}=2.5 V_{c1}=V_{c2}=0.5 V_{ss}=-2.5	0.1944	0.1856	0.1933
	V_{d1}=2.5 V_{d2}=2.5 V_{c1}=V_{c2}=1.2 V_{ss}=-2.5	0.3859	0.3375	0.35
Two-MOS mixed-operating	V_{ds}=0.8 V_{GS}=1.6	0.5	0.52	0.435
	NA			
Four-MOS mixed-operating (FIg.3.7)	V_{ds}=0.8 V_{GS1}=V_{GS2}=1.6	0.5	0.514	0.5
	NA			
Four-MOS mixed-operating(Fig.3.8)	V_{ds}=0.8 V_{GS1}=V_{GS2}=1.6	0.25	0.26	0.25
	V_{ds}=1.47 V_{GS}=2.316	0.2682	0.26	0.226

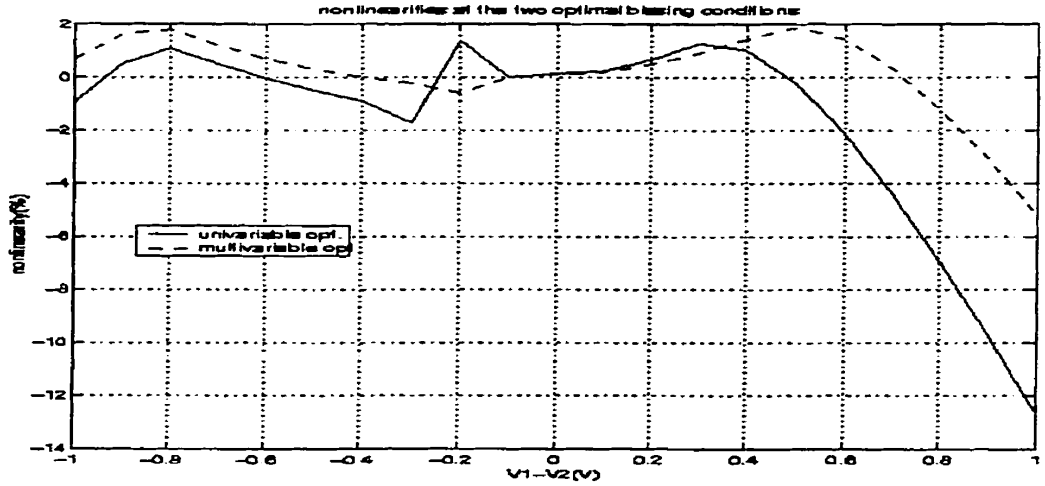
1. NA means that no practical optimal values can be obtained by the optimization procedures.

Since the expressions of the distortion constraints are obtained specifically for the input range of (-1V, +1V), for the structures which have small linear ranges, it is possible that the linearity is poorer than the highest acceptable constraints at the input range of (-1V, +1V). This is the reason that no practical optimal values are obtained for certain transconductor structures (see the note of Table 6.1). In order to overcome the input range limitation, the expressions of the constraints need to be made more general. Since the optimization methodology and the procedures are the same for all the transconductor structures, we will focus on the structures which can be optimized using current optimization programs. The modification of the optimization program can be addressed as a future improvement.

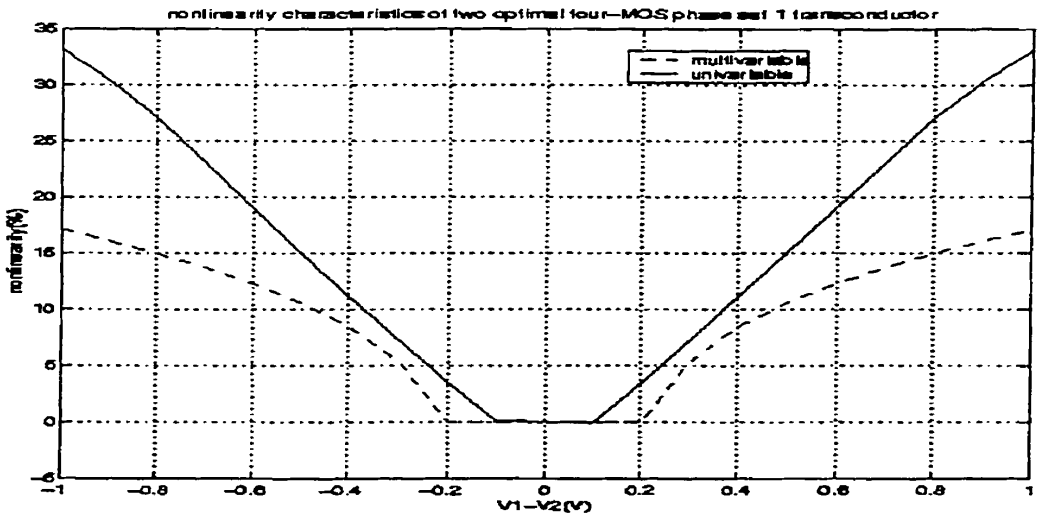
6.3 Linearity characteristic

6.3.1 Linearity Comparison between single variable and multivariable optimization results

To compare the nonlinearity characteristic of the transconductors which are biased according to single variable optimization results or multivariable optimization results, HSPICE netlists for nonlinearity simulation were created and executed. Fig.6.2. presents the simulated nonlinearity characteristics of two and four input-MOS gate-biased transconductors. For each graph, the x-axis represents the difference of the two input voltages. .

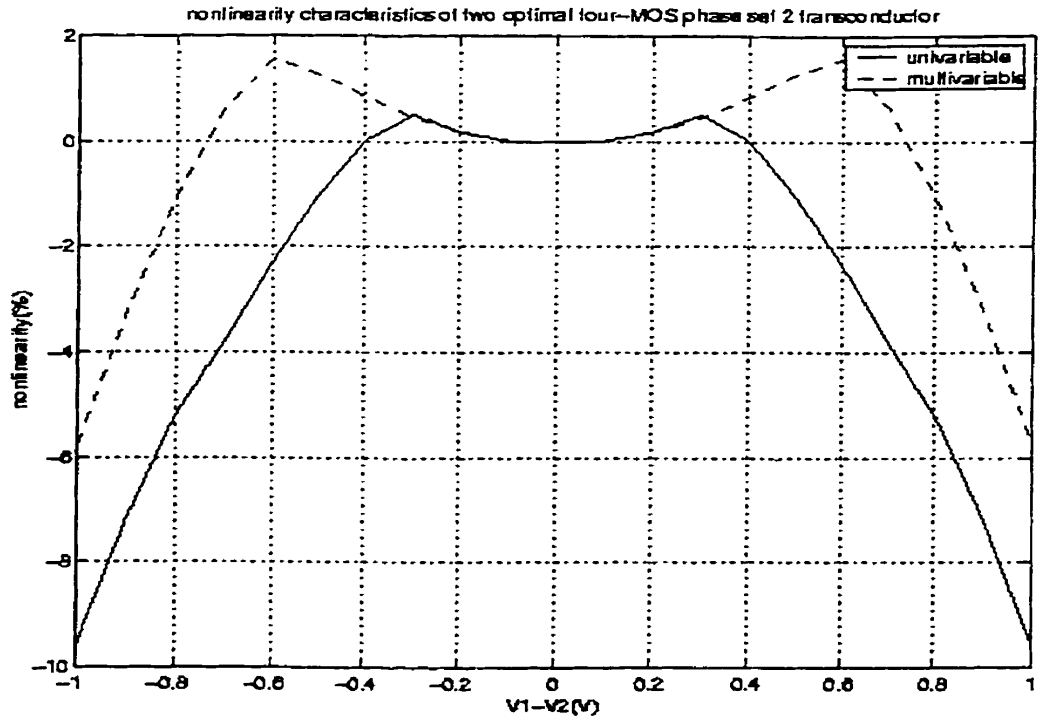


(a) two input-MOS structure

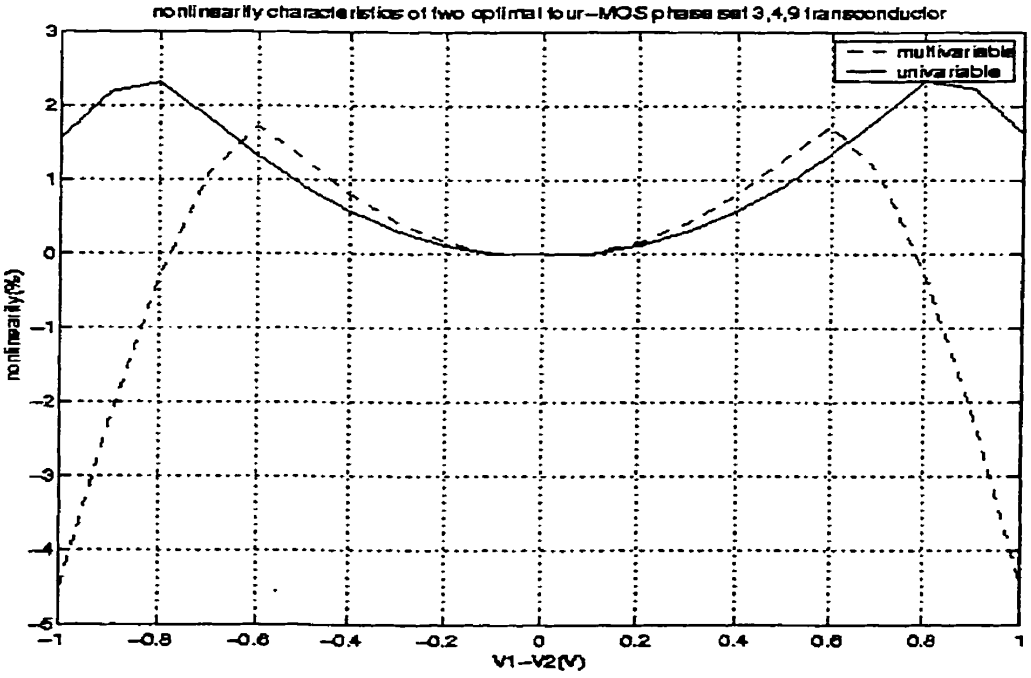


(b) four input-MOS: phase set 1

Fig. 6.2 Linearity characteristics of gate-biased four input-MOS transconductor (balance-biased)

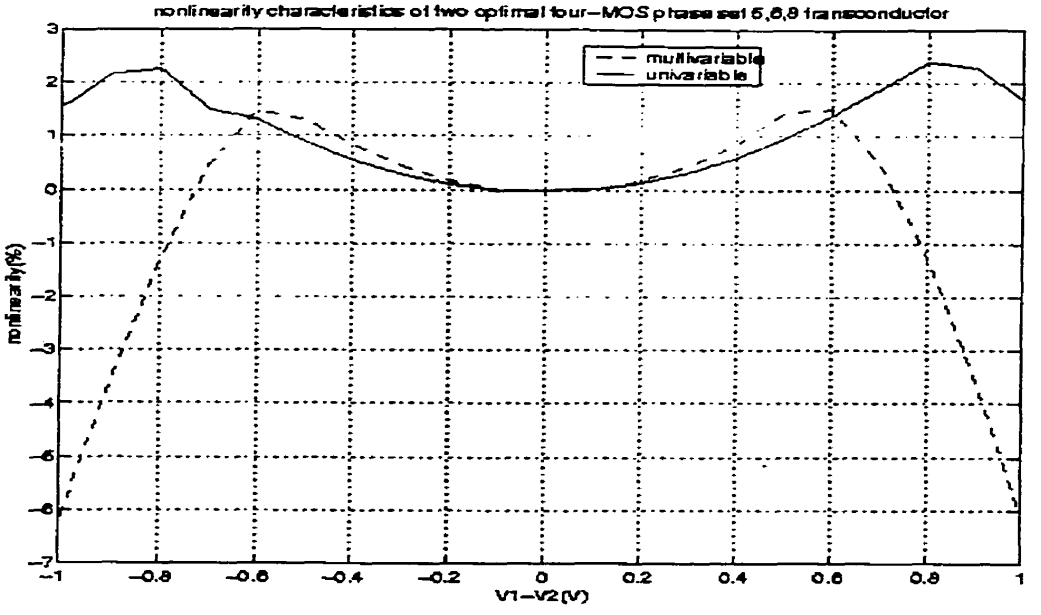


(c) four input-MOS: phase set 2



(d) four input-MOS: phase set 3,4,9

Fig. 6.2 Linearity characteristics of gate-biased four-input-MOS transconductor (balance-biased) (Cont'd)



(e) four input-MOS: phase set 5,6,8

Fig. 6.2 Linearity characteristics of gate-biased four input-MOS transconductor (balance-biased)

The y-axis shows the percentage nonlinearity of the transconductance. In chapter 4 we have discussed the linearity characteristic of the transconductor structures. In chapter 5, we also analytically proved that balance-biased structures have less nonlinear terms than their unbalance-biased counterparts. Since the even order nonlinear terms are proportional to the difference of the input biases, they will cancel out when the biases are equal. Therefore, from a designer's point of view, balance-biased structures are preferred.

Since the multivariable optimization uses linearity characteristics as constraints for the optimization, the feasible results obtained from the optimization should satisfy the requirement of the linearity. Compared to the unconstrained single variable optimized transconductor, the linearity performance of the transconductor which is biased at the results of multivariable constrained optimization should be more predictable.

The constraints employed for the optimization of section 6.1 are :

second order nonlinear term (DIS2) < 1%

third order nonlinear term (DIS3) <1%

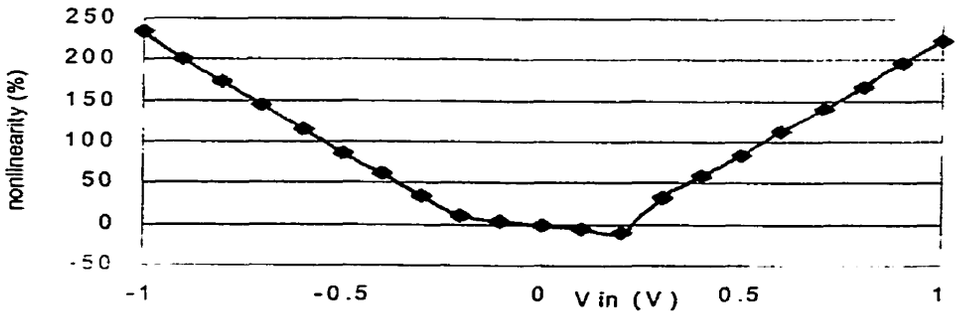
If no feasible optimal results can meet these constraints, the constraints can be increased up to 10%. The V_{bias}s listed in Table 6.1 conceptually satisfy these linearity requirements. But because of the simplification of the formulas in chapter 5, the simulated percentage nonlinearity of the transconductors can be higher than the expected 1%, as shown in Fig. 6.2. The formula employed to obtain the nonlinearity from the simulation is given below[13].

$$\varepsilon = (I_{out} - I_{out}(0) - g_m(0)V_d)/(g_m(0)V_d) \times 100$$

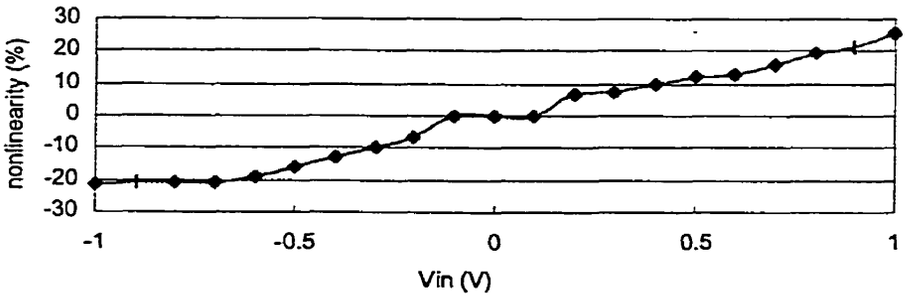
It can be seen from Fig.6.2(b)-(e) that the percentage nonlinearities at multivariable constrained optimal biases are better for the first two phase sets but worse for the later two phase sets. Excepting phase set 1, the nonlinearity of each phase set is less than 6% if the transconductors are biased at the optimal voltages obtained from multivariable constrained optimization. Phase set 1 shows high nonlinearity due to the following reasons: (i) The ideal optimal biases equal to the transistors' threshold voltage, which are not reachable. (ii) The ideal optimal biases result in zero transconductance and zero power dissipation which is not practical. Therefore, the actual biases used for the simulation can only be approximately "optimal" and hence lead to higher nonlinearity. Comparing with the nonlinearities of multivariable optimal cases, transconductors biased at the single variable optimal conditions have unpredictable nonlinearity. For example, the nonlinearities of phase sets 1 and 2 present to be much worse whereas the nonlinearity is much better for phase sets 3 to 9.

6.3.2 Experimental Linearity Characteristic

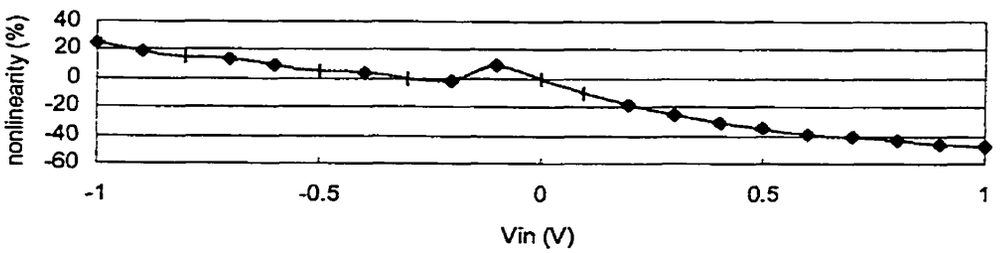
To experimentally measure the linearity characteristics of the transconductor structures, the transconductors are biased at their corresponding optimal bias conditions. The set up of the linearity measurement circuit is also shown in Appendix C. The experimentally obtained linear characteristics of the transconductors which are biased at the multivariable constrained optimal voltages are presented in Fig. 6.3



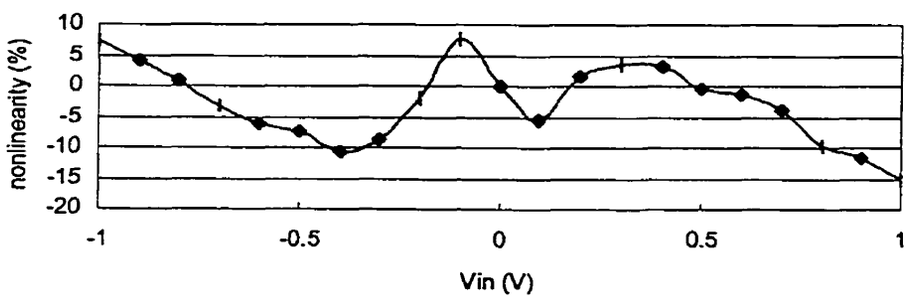
(a) Gate-biased four input MOS transconductor with phase set 1



(b) Gate-biased fourinput MOS transconductor with phase set 2

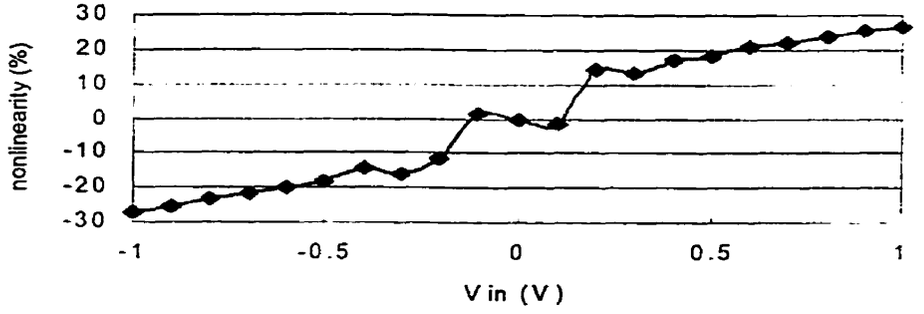


(c) Gate-biased four input MOS transconductor with phase set 3

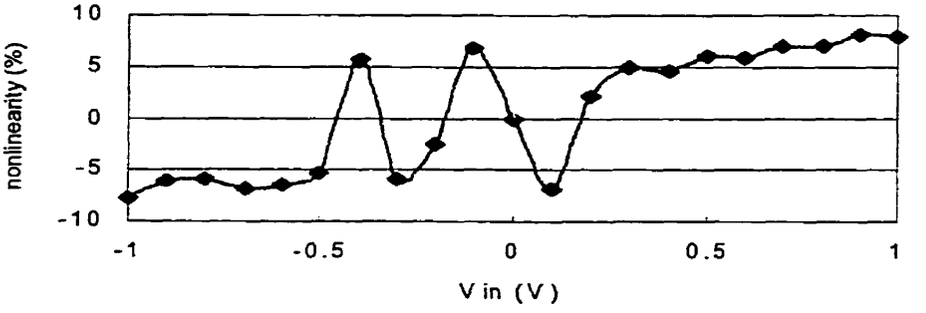


(d) Gate-biased four input MOS transconductor with phase set 4,5,6

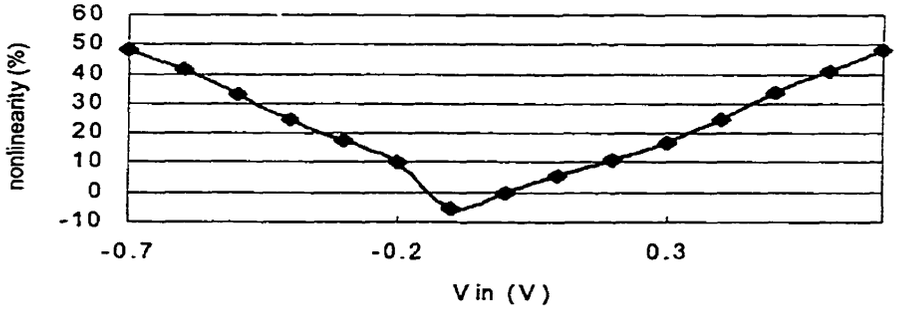
Fig. 6.3 Experimental results of the transconductors' linearity characteristics



(e) Gate-biased four input MOS transconductor with phase set 7

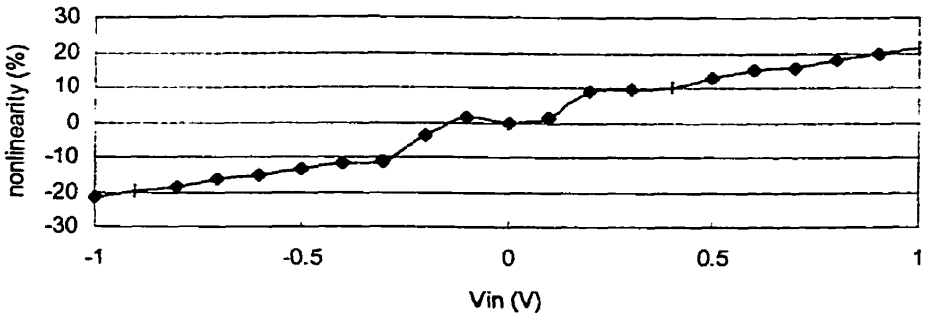


(f) Gate-biased four input MOS transconductor with phase set 8,9



(g) Drain/Source-biased four input MOS transconductor (case 3)

Fig.6.3 Experimental results of the transconductors' linearity characteristics (cont'd)



(h) Mixed operating four input MOS transconductor of the structure Fig.3.8

Fig.6.3 Experimental results of the transconductors' linearity characteristics (Cont'd)

Except for Fig. 6.3(a) and (g), the nonlinearities of the studied transconductor structures are varying from *-20%* to *+20%* for the input DC voltage range of *-1V* to *+1V*. The reason that the gate-biased four input MOS transconductor with phase set 1 has very poor linearity (Fig. 6.3(a)) is as follows. The optimal bias voltages of this structure are all close to the threshold voltage of the input MOS transistor. Since differential input signals are employed for the structure, a small negative DC voltage will cause the input MOS transistor fall into weak inversion operating region. We have mentioned before that in weak inversion operating region, the drain/source current of a MOS transistor is exponentially related to its gate voltage and hence has very poor linearity.

For drain/source-biased four input MOS transconductor (case 3), the optimal gate voltage of the input PMOS transconductors are equal to *1.2V*. In order to ensure that the input PMOS transistors are operating in the saturation region, the differential DC input voltage should be lower than *0.6V*. In addition, since the optimal V_{dI} is different from V_{dd} which is the substrate potential of the transconductor, the threshold voltage of the two PMOS input transistors which have source voltage of V_{dI} are higher due to the body effect (negative V_{SB} for PMOS transistor). Thus the input range in which the input MOS transistors can

operate properly is further reduced.

6.4 Summary

This chapter presents the numerical and HSPICE simulation results of the multivariable constrained frequency-power-efficiency optimization of the transconductor structures. The linearity characteristics of the optimally biased transconductors are studied as well. Experimental measurements are also conducted using the fabricated transistor array. It is revealed that the experimented optimal g_{ac}/P_{diss} ratios are within $\pm$ *10%* range of the simulated values. However, the measured linearities of the transconductors are much worse than the predictions. This is because the transistor models and the formulas employed by the optimization programs are simplified. The accuracy of the prediction could be improved if more precise formulas are used in the optimization program. Since our goal at the current stage is to prove the existence of the optimal bias conditions and propose a systematic methodology for the optimization, developing a more rigorous optimization algorithm could be an undertaking of the future.

Chapter 7

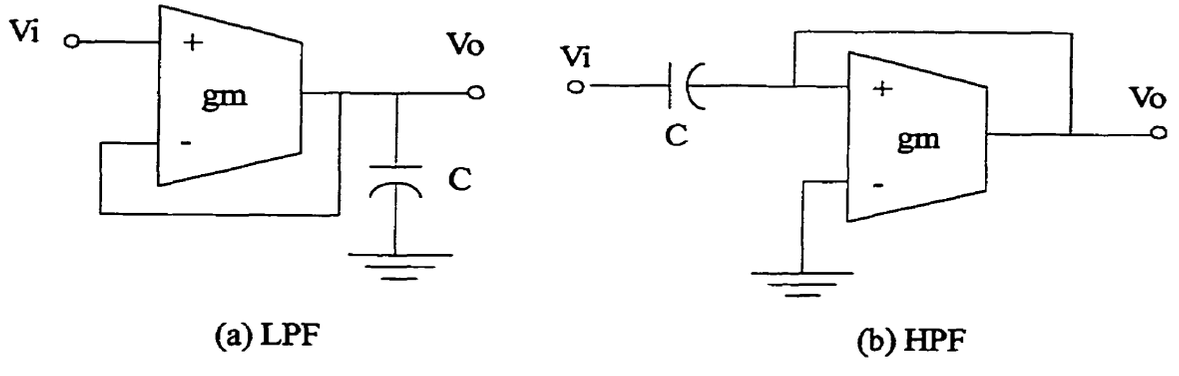
Applications of Transconductor Frequency-Power-efficiency Optimization

On the basis of transconductors (also named the operational transconductance amplifier: OTA), many important signal processing systems can be implemented [35]. Among them, the transconductor-C (or OTA-C) filters attracted a lot of attentions and have found applications in telecommunication, multimedia, consumer electronics, etc. In this chapter we shall investigate how the frequency-power efficiency optimization of CMOS transconductors will affect the performance of transconductor-C filters which are built with the transconductors of interest.

7.1 Frequency-Power-efficiency optimization on Transconductor-C filters

7.1.1 Transconductor-C filter Implementation

Since higher order filters can be achieved by cascading first- and second-order filters, we will focus on the analysis of first- and second- order transconductor-C filters. Figure 7.1 shows the diagram of first-order transconductor-C filters.



(a) LPF (b) HPF

Fig. 7.1 First order transconductor-C filter block

The voltage transfer functions of Fig.7.1 are

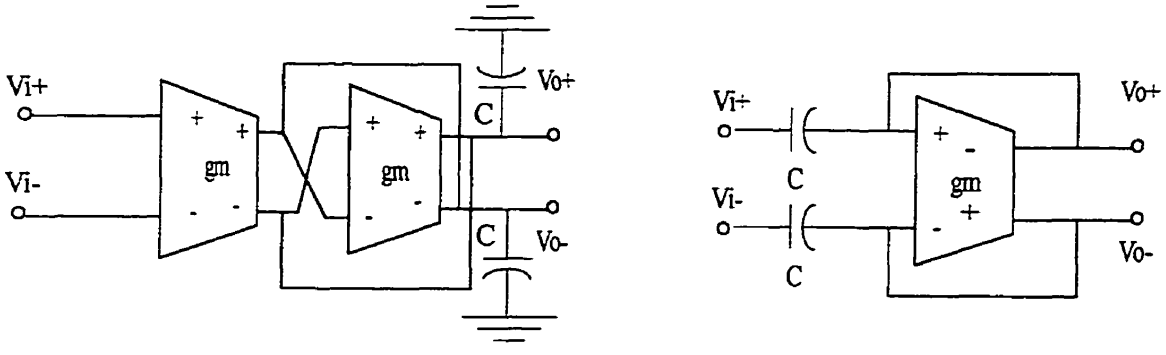
$$\frac{V_o}{V_i} = \frac{g_m}{sC + g_m} \tag{7.1}$$

for Fig. 7.1(a) and

$$\frac{V_o}{V_i} = \frac{sC}{sC + g_m} \tag{7.2}$$

for Fig. 7.1(b).

The transconductor used in Fig. 7.1 is single-input and single-output structure. However, most of the transconductor structures we have discussed in the previous chapters use differential ac input signals and their output signals are also taken differentially. Thus, the structures in Fig. 7.1 need to be modified as shown in Fig. 7.2(a) and (b).



(a) LPF (b) HPF

Fig. 7.2 Fully-balanced first order transconductor-C filters

The transfer functions of the fully-balanced first-order transconductor-C filters are the same as those of eqns.(7.1) and (7.2).

There are different structures of second-order transconductor-C filters [34]. The diagram of the second-order transconductor-C filter that we are going to discuss is given in Fig. 7.3. Other kinds of structures can be analyzed similarly. Fig. 7.3 achieves bandpass frequency characteristic at the output port of the last stage. If the output signal is taken at the output

port of the third stage, a lowpass frequency characteristic will be observed. The transfer functions of the lowpass and bandpass filters are given below.

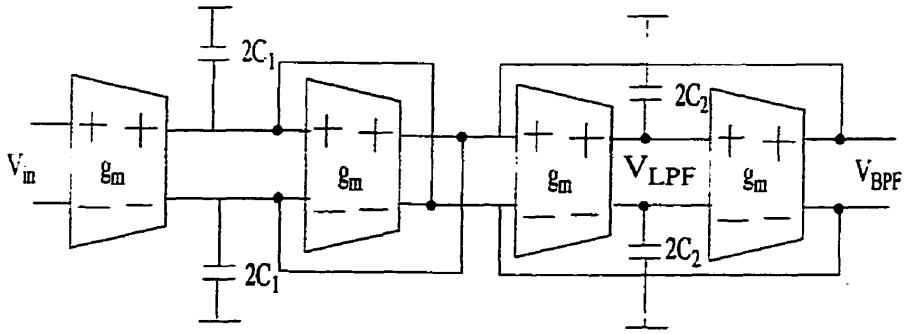


Fig. 7.3 Second-order transconductor-C filter

$$H_{LPS}(s) = \frac{g_m^2}{C_1 C_2 s^2 + sC_2 g_m + g_m^2} \tag{7.3}$$

and

$$H_{BPS}(s) = \frac{sC_2 g_m}{C_1 C_2 s^2 + sC_2 g_m + g_m^2} \tag{7.4}$$

When considering cascade of fully-balanced transconductors, an important issue arises, that is, output DC offset elimination for each transconductor block. One advantage of adopting differential-output structure is to reduce the DC offset of the output signal. Ideally, the DC offset at each of the two output terminals should be equal and hence will cancel out while their difference is taken. However, when loaded by another differential-input transconductor structure, the output offset at each terminal will act as extra input bias to the load transconductor. Therefore the bias condition of the load transconductor will be changed from its original setup. This phenomenon becomes more severe when more stages are being cascaded and in the end, it will either lead to a malfunctional circuit or a circuit that does not function at all. To overcome the DC offset problem, common-mode feedback technique is developed. The principle of common-mode feedback is introducing a negative feedback which is controlled by the common-mode signal of the output stage(i.e., the DC

offset at each terminal of the differential-out structure). Figure 7.4 illustrates the concept of common-mode feedback.

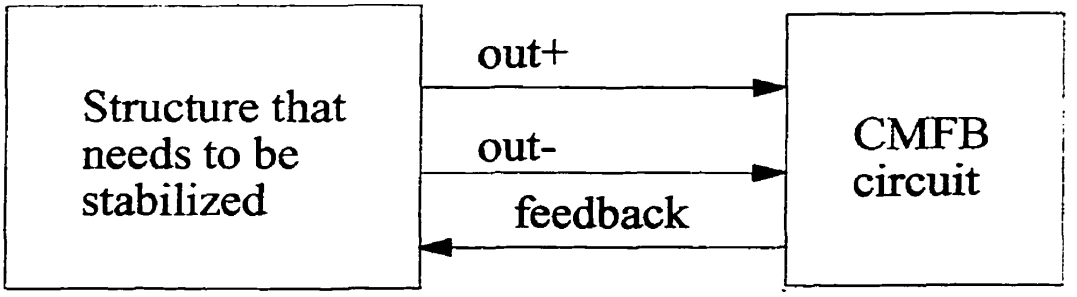


Fig. 7.4 Concept of common-mode feedback

Many different common-mode feedback circuits have been proposed. The one which is most suitable for reducing the DC offset of CMOS transconductors is shown in Fig. 7.5 [36] and it will be adopted in our transconductor-C filter structures.

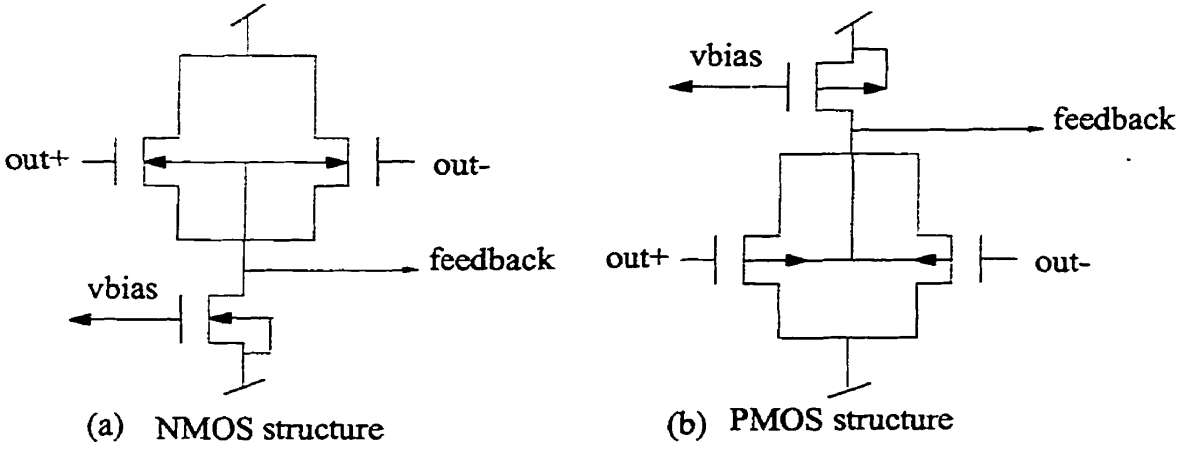


Fig. 7.5 Common-mode feedback circuit used by fully-balanced transconductors

Another extra circuit that must be included in transconductor blocks when implementing transconductor-C filters is the input-bias circuit. The main reasons of using input-bias circuit are : i) simultaneously adjusting biases of multi-transconductors; ii) preventing ac input signal from being affected by DC adjustment; iii) combining the ac input with the

desired DC biases and applying them into the transconductor. The input-bias circuit is used to add a dc level shift to the ac signal much like the dc level shift circuit in an operational amplifier system. Therefore, for two-input-MOS transconductors, two input-bias circuits are used, for four-input-MOS transconductors, four input-bias circuits are needed for each transconductor block. Figure 7.6 presents the schematic diagram of the input-bias circuit.

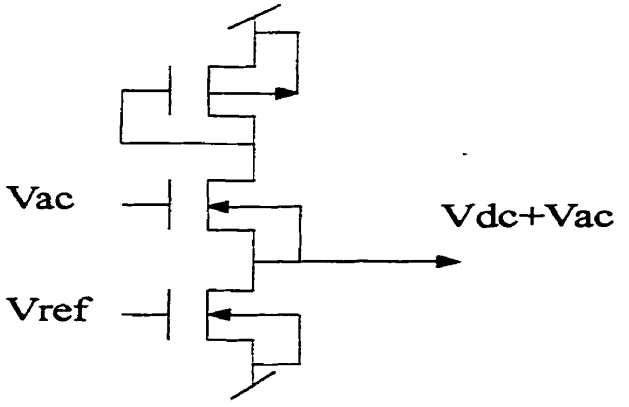
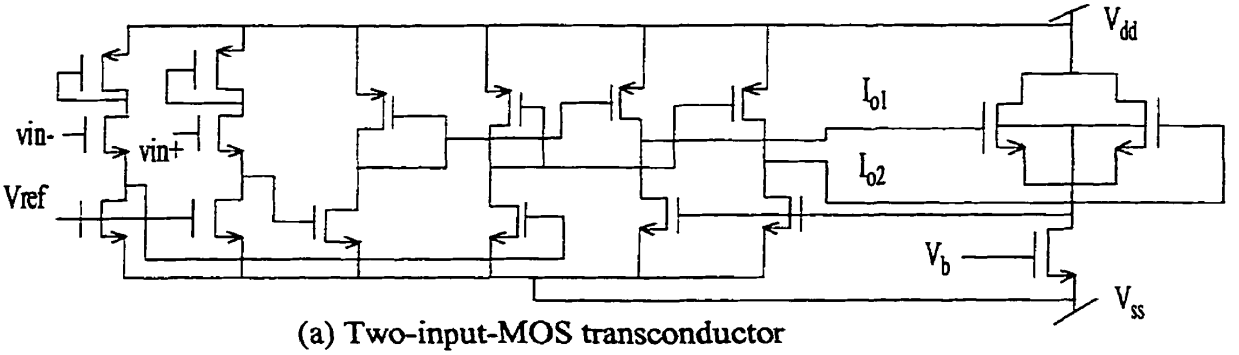


Fig. 7.6 Input-bias circuit

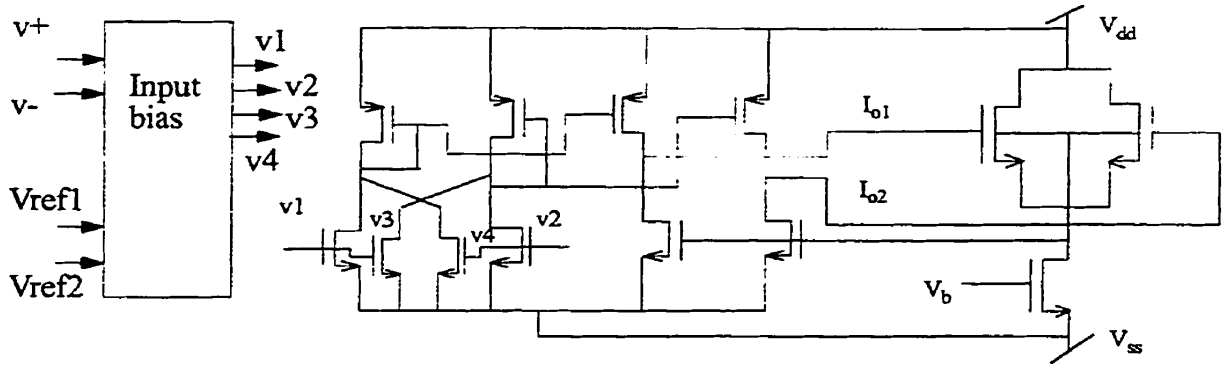
The input of the middle transistor (i.e., V_{ac}) is pure ac signal for the first transconductor block. For the rest transconductor blocks, V_{ac} is the output of the preceding adjacent block. The DC voltage at the gate of the lowest transistor can be externally adjusted so that the DC biases of the transconductor(i.e., V_{dc}) can be tuned to an expected value.

Taking common-mode feedback and input-bias into account, the fully-balanced transconductor blocks of gate-biased, drain/source-biased structures are shown in Fig. 7.7(a)-(c).

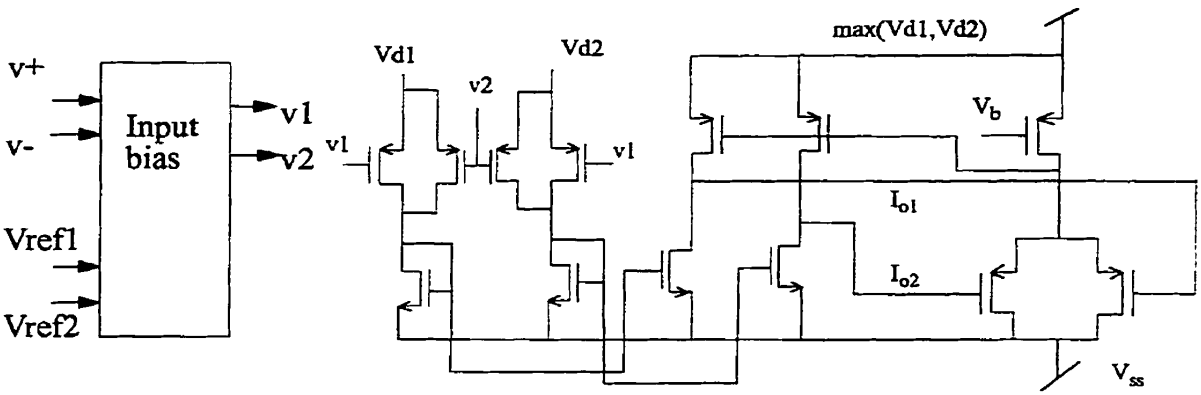


(a) Two-input-MOS transconductor

Fig.7.7 Fully-balanced transconductor block of transconductor-C filters (con't)



(b) Four-input-MOS balance-biased transconductor



(c) Four-input-MOS drain/source-biased transconductor

Fig. 7.7 Fully-balanced transconductor block of transconductor-C filters

The input-bias box of Fig. 7.7(b) consists of four input-bias circuits of Fig. 7.6. The V_{ref} of two input-biases are connected to Vref1, the other two are connected to Vref2. The ac input to each input-bias circuit is set to $v+$ or $v-$ depending on the desired input phase arrangement of the transconductor. The input-bias box of Fig. 7.7(c) consists of two input-bias circuits with V_{ref} and ac input being Vref1, $v+$ and Vref2, $v-$ respectively. Although Fig. 7.7 only presents three kinds of transconductor blocks, other kinds of fully-balanced transconductor blocks can be easily obtained in the similar manner.

In the following sections, we will study the frequency-power performance of the transconductor-C filters on the basis of the transconductor blocks given in Fig. 7.7. Similar analysis

can also be done with respect to other transconductor-based filters but they will not be addressed here.

7.1.2 Frequency-power-efficiency characteristic of transconductor-C filters

In order to study the frequency-power efficiency of a CMOS transconductor-C filter, the analytical formulas of -3dB bandwidth (for lowpass/highpass filters) or f_0 (for bandpass filters) and the DC power dissipation must be derived first. For Fig. 7.2, the expressions are

$$f_{-3dB} = \frac{g_m}{2\pi C} \tag{7.5}$$

$$P_{diss|LPF} = 4P_{diss|transconductor} + 2P_{bias} + 2P_{CMFB} \quad \text{and}$$

$$P_{diss|HPF} = 2P_{diss|transconductor} + P_{bias} + P_{CMFB} \tag{7.6}$$

For Fig. 7.3, the expressions are

$$f_{-3dB} = f_0 = \frac{g_m}{2\pi\sqrt{C_1 C_2}} \tag{7.7}$$

$$P_{diss|LBF} = P_{diss|BPF} = 8P_{diss|transconductor} + 4P_{bias} + 4P_{CMFB} \tag{7.8}$$

In eqns.(7.5) and (7.7), the frequency performance is considered to be external-capacitor-dependent function. Practically, the CMFB circuits will introduce parasitic capacitors to the corresponding transconductors. Using Fig. 7.5 CMFB structure, the gate-to-source and gate-to-drain capacitors will be in parallel with external capacitors. Thus the entire load capacitance of the transconductors will be bigger and hence the bandwidth or center frequency of the filters will be lower than those predicted by eqns.(7.5) and (7.7). When smaller transistors are used for the CMFB circuits, the effect of parasitic capacitances will be smaller and the overall frequency characteristic of the filters should be closer to the pre-

dictions of eqns.(7.5) and (7.7).

Consider the ratio of equations (7.5) to (7.6) and (7.7) to (7.8). They represent the frequency-power efficiency of first- and second-order transconductor-C filters and are expressed by

$$\left(\frac{f}{P_{diss}}\right)_{filter} = \frac{g_m}{2\pi C'(nP_{diss|transconductor} + mP_{bias} + mP_{CMFB})} \tag{7.9}$$

where $C' = C$ for first-order filters and $C' = \sqrt{C_1 C_2}$ for second-order filters; $n = 2, 4, 8$ and $m = 1, 2, 4$ for highpass first-order, lowpass first-order and second-order respectively. If $C_1 = C_2 = C$ for second-order filters, the expressions of the frequency characteristic of the first- and second-order filters become identical. In this case, the frequency-power-efficiency of the first- and second-order transconductor-C filters will only be different by a constant factor (i.e., 0.5 or 0.25).

7.1.3 Numerical and HSPICE simulations

In section 7.1.2 we have found that the frequency-power efficiency of a transconductor-C filter is proportional to the frequency-power efficiency of the transconductor on which the filter is built. This observation implicates that if the frequency-power efficiency of a transconductor can be improved, the frequency-power efficiency of the filter can also be improved. In the previous chapters, we have developed a systematic methodology to optimize frequency-power efficiency characteristic of several kinds of CMOS transconductors. By employing optimized transconductor structures in the filters, the filters should also present optimal frequency-power efficiency characteristic.

To verify the above prediction, three types of CMOS transconductor structures are taken to build first- and second-order transconductor-C filters. They are: gate-biased two-input-MOS transconductor, gate-biased four-input-MOS transconductor and drain/source-biased four-input-MOS transconductor. For the first two types of transconductors, balanced DC

biases are used. Both single variable unconstrained and multivariable constrained optimization results are employed for the transonductors used to implement the filters. To illustrate the existence of optimal frequency-power efficiency of a transconductor-C filter, the frequency-power efficiency of the filters at non-optimal adjacent biases are also exaimined.

During the course of investigating transconductor-C filters, the 1.5 μm CMOS technology became unavailable for fabrication. In order to verify our optimization methodology physically, we made a test chip using a 0.35 μm CMOS technology. The following calculations and simulations are obtained on the basis of a 0.35 μm CMOS technology parameters. The procedures followed to derive the optimal biases of the transconductors are the same as those described in Chapter 6.

Table 7.1 Frequency/P_{diss} of optimally biased transconductor-C filters[1] (single variable optimization)

Transconductor	Filter	biases(V)	Numerical freq./P(Hz/W)	Simulated freq./P
Gate-biased Two-MOS (balanced)	1st-order LPF	1.6	5.278e9 (5.3e9)	0.839e9 (0.84e9)
	1st-order HPF		10.556e9 (10.6e9)	9.235e9 (9.27e9)
	2nd-order LPF		2.638e9 (2.65e9)	0.654e9 (0.65e9)
	2nd-order BPF		2.638e9 (2.65e9)	0.839e9 (0.84e9)
Four-MOS (phase set 1)	1st-order LPF	V_c=0.6 V_b=1.6	2.8e9 (4.70e9)	1.266e9 (2.12e9)
	1st-order HPF		5.6e9 (9.41e9)	5.3e9 (8.8e9)
	2nd-order LPF		1.4e9 (2.35e9)	0.393e9 (0.65e9)
	2nd-order BPF		1.4e9 (2.35e9)	1.173e9 (2.03e9)

Table 7.1 Frequency/P_{diss} of optimally biased transconductor-C filters[1] (single variable optimization)

Transconductor	Filter	biases(V)	Numerical freq./P(Hz/W)	Simulated freq./P
Four-MOS (phase set 2)	1st-order LPF	V_c=1.2 V_b=1.6	5.6e9 (6.07e9)	5.50e9 (6.01e9)
	1st-order HPF		11.2e9 (12.14e9)	10.88e9 (11.86e9)
	2nd-order LPF		2.8e9 (3.03e9)	1.30e9 (1.43e9)
	2nd-order BPF		2.8e9 (3.03e9)	1.92e9 (2.11e9)
Four-MOS (phase set 3)	1st-order LPF	V_c=1.0 V_b=1.6	3.34e9 (4.10e9)	3.12e9 (3.84e9)
	1st-order HPF		6.68e9 (8.21e9)	6.21e9 (7.65e9)
	2nd-order LPF		1.67e9 (2.05e9)	0.82e9 (1.01e9)
	2nd-order BPF		1.67e9 (2.05e9)	1.03e9 (1.27e9)
Four-MOS (phase set 4)	1st-order LPF	V_c=1.4 V_b=1.6	2.58e9 (2.64e9)	2.3e9 (2.56e9)
	1st-order HPF		5.17e9 (5.28e9)	5.02e9 (5.14e9)
	2nd-order LPF		1.29e9 (1.32e9)	0.64e9 (0.66e9)
	2nd-order BPF		1.29e9 (1.32e9)	1.25e9 (1.27e9)
Drain/Source-biased (set 1)	1st-order LPF	V_{d1}=1.2 V_c=0.5	4.63e9 (4.76e9)	1.13e9 (1.16e9)
	1st-order HPF		9.27e9 (9.52e9)	2.52e9 (2.59e9)
	2nd-order LPF		2.31e9 (2.38e9)	0.29e9 (0.30e9)
	2nd-order BPF		2.31e9 (2.38e9)	0.59e9 (0.60e9)

Table 7.1 Frequency/P_{diss} of optimally biased transconductor-C filters[1] (single variable optimization) (Cont'd)

Transconductor	Filter	biases(V)	Numerical freq./P(Hz/W)	Simulated freq./P
Drain/Source-biased(case 3)	1st-order LPF	V_{d1}=1.8 V_c=0.5	6.41e9 (6.46e9)	1.40e9 (1.42e9)
	1st-order HPF		12.82e9 (12.93e9)	3.18e9 (3.21e9)
	2nd-order LPF		3.20e9 (3.25e9)	0.32e9 (0.32e9)
	2nd-order BPF		3.20e9 (3.23e9)	0.93e9 (0.94e9)

1. The values inside the brackets are obtained by dividing the frequency by the power which is consumed by the transconductor-C parts of each filter circuit.

Table 7.2 Frequency/P_{diss} of optimally biased transconductor-C filters[1,2] (multivariable optimization)

Transconductor	Filter	biases (V)	Numerical freq./P	Simulated freq./P
Four-MOS (phase set 1)	1st-order LPF	V_c=0.6 V_b=0.8	0.98e9 (11.93e9)	0.68e9 (7.69e9)
	1st-order HPF		1.96e9 (23.86e9)	1.95e9 (23.72e9)
	2nd-order LPF		0.49e9 (5.965e9)	0.18e9 (1.84e9)
	2nd-order BPF		0.49e9 (5.965e9)	0.33e9 (5.4e9)
Four-MOS (phase set 2)	1st-order LPF	V_c=0.6 V_b=0.6	0.51e9 (25.43e9)	0.42e9 (26.9e9)
	1st-order HPF		1.035e9 (50.86e9)	0.68e9 (73.72e9)
	2nd-order LPF		0.25e9 (12.71e9)	0.12e9 (6.21e9)
	2nd-order BPF		0.25e9 (12.71e9)	0.24e9 (12.39e9)

Four-MOS (phase set 3-18)	1st-order LPF	V_c=0.6 V_b=0.6	0.25e9 (12.7e9)	0.18e9 (11.54e9)
	1st-order HPF		0.51e9 (25.4e9)	0.27e9 (29.8e9)
	2nd-order LPF		0.12e9 (6.35e9)	0.06e9 (3.01e9)
	2nd-order BPF		0.12e9 (6.35e9)	0.12e9 (6.28e9)
Drain/Source-biased (case 1,2)	1st-order LPF	V_{d1}=2.35 V_c=1.85	0.21855e9 (9.27e9)	0.15e9 (8.13e9)
	1st-order HPF		0.437e9 (18.54e9)	0.05e9 (24.13e9)
	2nd-order LPF		0.109e9 (4.63e9)	0.04e9 (1.89e9)
	2nd-order BPF		0.109e9 (4.63e9)	0.097e9 (4.04e9)

1. The values inside the brackets are obtained by dividing the frequency by the power which is consumed by the transconductor-C parts of each filter circuit.
2. There are no practical optimal biases can be obtained for the drain/source biased case 3 structure.

The simulated frequency-power ratio of the filters are obtained from post-layout simulation. A lot of parasitic capacitances and resistances are extracted while generating the HSPICE netlists of the filters. These parasitic components result in the deviation of the filters' critical frequencies and the DC power consumptions. In addition, the periphary circuits also increase the parasitic capacitances and consume DC power, and hence make the frequency-power efficiency of the filters even smaller. Comparing the optimal frequency/power ratio for single variable optimized structure and multivariable optimzed structure, it is found that excluding the impacts of periphary circuits, multivariable optimized structures present better frequency-power efficiency. However, since the bias conditions obtained from multivariable optimization result in higher DC power consumption for the input-biasing circuits and the CMFB circuits (i.e., the two peripheral circuits), the overall frequency-power ratios turns out to be worse.

The results presented in this section reveal that by optimizing the g_{ac}/P_{diss} of transconductor structures, the frequency-power efficiency of the transconductor-C filters which are based on that transconductor can be improved as well. But due to the existence of the periphery circuits employed in the filter circuits, the optimal biases obtained from multi-variable optimization on the transconductors do not necessarily lead to better frequency-power efficiency of the filters implemented with these transconductors.

7.1.4 Experimental measurement

In order to study the impact of the transconductor optimization on the frequency-power ratio of the transconductor-C filters, a test chip which consists of four transconductor-C filter structures is fabricated using TSMC 0.35 μm CMOS technology. The four filters are based on gate-biased two input-MOS transconductor, four input-MOS transconductor with ac phase being (+ - - +), four input-MOS drain/source biased transconductor and mixed-operating four input-MOS transconductor respectively. All the four filters are second-order BPF fitlers.. The layout of the chip is shown in Fig.7.8.

7.1.5 Test settings and experimental results

Since the expected center frequency of the filters are tens of mega hertz, a printed circuit board is used for testing the filter chip. A 40-pin socket is soldered on the board and large capacitors are used to decouple the ac interferences on the DC supplies and biases. In order to obtain differential ac input, a general purpose transistor array chip MC3346 is used to implement single input to differential output transformation.

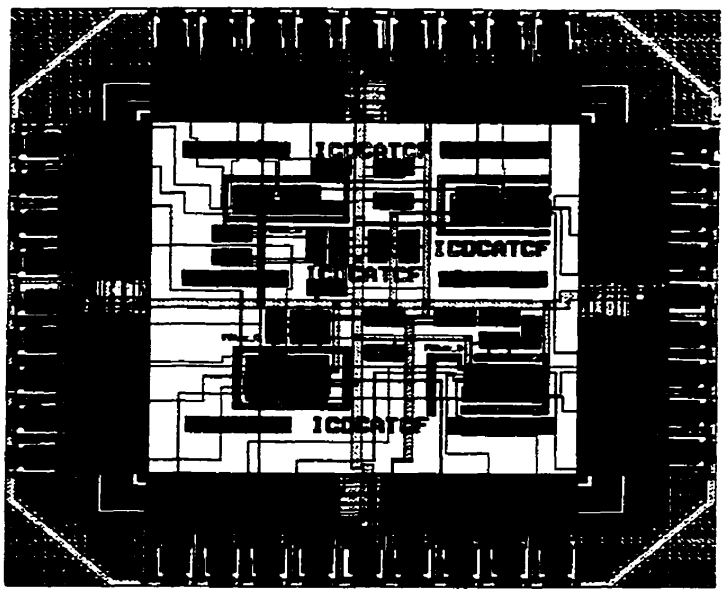


Fig. 7.8 Layout of the fabricated filter chip (3008x3008micron^2)

The MC3346 is inserted in a 14-DIP socket which is also soldered on the board. The input ac signal is generated by a Rhode & Shwartz RF signal generator. The frequency range of the input signal is 100KHz to 3GHz. The filter which is based on the gate-biased four input-MOS transconductor with phase set 2 is tested. The results obtained are given in Table 7.3.

Table 7.3 Measured frequency-power efficiency of transconductor-C filter (ref1=-1.97V Vdd=-Vss=2.5V)

Ref2(V)	Bias(V)	f_0(MHz)	P_{diss}(mW)	f_0/P_{diss}
-1.0	-1.61	38.3	320.95	0.119e9
-1.25	-1.65	46.1	320.55	0.1438e9
-1.5	**-1.76**	**60.9**	**319.85**	**0.1904e9**
-1.6	-1.82	42.9	319	0.1344e9
-1.85	-1.91	41	318	0.1289e9

Ref1 = -1.97V corresponds to 1.6V gate-source voltage of input transistor, Ref2 = -1.5V corresponds to 1.2V gate-source voltage of input transistor. Comparing with the values

given in Table 7.1, we can see that the experimental optimal bias voltage is consistent with the simulated result. However, the measured power dissipation is much more than the simulated values. This could because that the measured power dissipations include the power consumed by the pads. And since four filters are integrated on the chip, there may have some parasitic paths which also result in extra power consumption. The center frequency obtained by the measurements are much higher than the simulated values. This may because what we observed is 2nd harmonic of the actual center frequency. It is also noticed that the transient response of the filter's output showed some distinguishable distortaions at some frequencies. Since the design is not self-testable, it is difficult to figure out the exact reason of the distortions. Either more diagnostic measurements need to be conducted or a new filter chip which includes self-testing mechanism needs to be fabricated.

7.2 Applying frequency-power efficiency optimization to a transconductor-based system: Case study

It is known that the goal of a circuit design is to achieve certain specifications. Thus a design process usually start from a set of specifications. For a transconductor design, the important specifications include the range of transconductance, power dissipation limit, area limit, linearity, noise figure, etc. In addition, tunability is also a desired feature. In this section, we will use a particular transconductor structure [27] to show step by step how the proposed frequency-power efficiency optimization technique can be fit into a design flow and its influence on the design specifications of the system built with the transconductor.

7.2.1 The transconductor structure

Figure 7.9 is the transconductor structure that is going to be used in the case study. From Fig. 7.9 one can see that it consists of two series CMOS-pairs. Assume transistors of the same type (NMOS or PMOS) are sized identically, the output current and power dissipa-

tion expressions of Fig. 7.9 can be derived as eqns.(7.10) and (7.11).

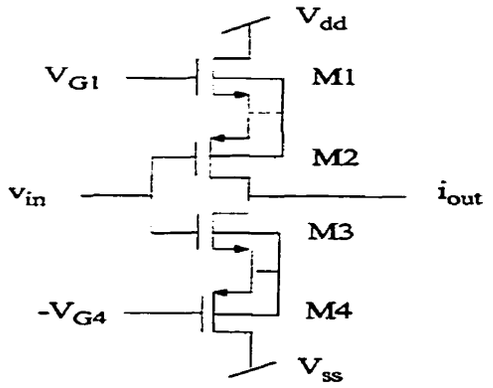


Fig. 7.9 Transconductor structure for the case study

$$I_{out} = 2K_{eff}(V_{G1} + |V_{G4}| - \Sigma V_t)v_{in} \tag{7.10}$$

$$P_{diss} = K_{eff}[(V_{G1} - V_{tn1} - |V_{tp2}|)^2](V_{dd} - V_{ss}) \tag{7.11}$$

where $K_{eff} = \frac{K_n K_p}{(\sqrt{K_n} + \sqrt{K_p})^2}$, $\Sigma V_t = V_{tn1} + |V_{tp2}| + V_{tn3} + |V_{tp4}|$. The transconductance of this linear transconductor is

$$g_{ac} = K_{eff}(V_{G1} + |V_{G4}| - \Sigma V_t) \tag{7.12}$$

The structure shown in Fig. 7.9 does not have body effect because the source-bulk voltage of each transistor is zero. In order to obtain zero offset for zero input signal, the following condition must be satisfied,

$$V_{G1} + V_{G4} = V_{tn1} + |V_{tp2}| - V_{tn3} - |V_{tp4}| \tag{7.13}$$

Without body effect, all NMOS transistors have the same threshold voltage and so do the PMOS transistors. Thus eqn.(7.13) becomes zero, which means that $V_{G1} = -V_{G4}$. Let $V_{G1} = -V_{G4} = V_G$ The g_{ac}/P_{diss} of transconductor Fig. 7.9 has the expression of

$$\frac{g_{ac}}{P_{diss}} = \frac{8}{(V_{dd} - V_{ss})(2V_G - \Sigma V_t)} \tag{7.14}$$

Obviously, eqn.(7.14) is a monotonically decreasing function with respect to V_G and the lowest applicable value of V_G is $\Sigma V_i/2$.

7.2.2 The design flow

Take the filter design given in [37] as an example. The goal is to design a bandpass filter with center-frequency of 4MHz and bandwidth of 800KHz. The passband ripple is 0.5 dB. Analyses showed that the nominal operation of this filter can be achieved by an eighth-order Chebyshev bandpass filter. The circuit can be built by cascading four second-order transconductor-C bandpass sections. The nominal pole frequencies and Q factors (f_{pi}/*MHz*, Q_i, $i=1, ...,4$) of the four second-order bandpass sections are 3.5807/23.9, 3.8090/9.83, 4.1586/9.83, and 4.4237/23.9, respectively. Employing the same filter architecture as given in [38] (re-drawn in Fig. 7.10), the transfer function of each constituent second order bandpass filter is given in eqn.(7.15).

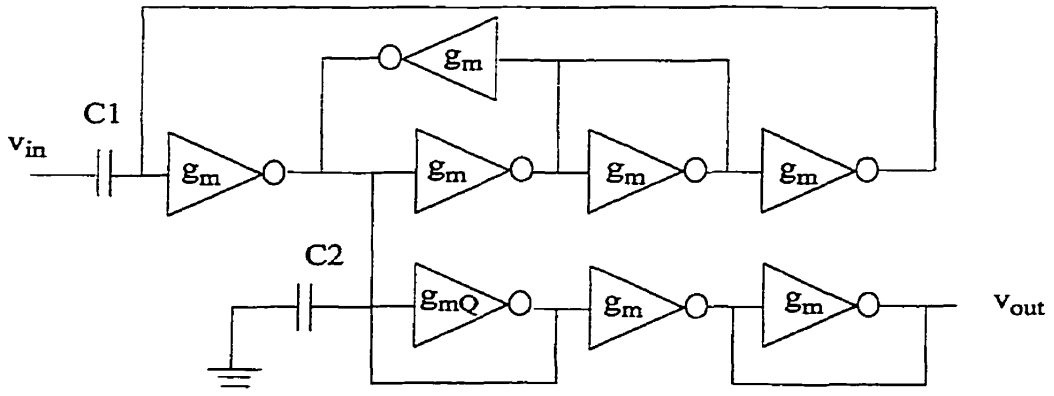


Fig. 7.10 Diagram of second-order transconductor-C bandpass filter

$$H_{BPF}(s) = \frac{g_m C_1}{C_1 C_2 s^2 + C_1(g_{mQ} - g_m)s + g_m^2} \tag{7.15}$$

The center frequency and the Q factor of filter Fig. 7.10 are $\omega_0 = \frac{g_m}{\sqrt{C_1 C_2}}$ and $Q = \frac{g_m}{g_{mQ} - g_m}\sqrt{\frac{C_1}{C_2}}$. Assuming $C_1 = C_2 = 1pF$, the g_m and g_{mQ} for each second order bandpass

section are derived and listed in Table 7.4.

Table 7.4 g_m and g_{mQ} for biquad BPF sections

section 1	section 2	section 3	section 4
g_m= 22.4982u g_{mQ}=23.4395u	g_m=23.9326u g_{mQ}=26.3673u	g_m=26.2192u g_{mQ}=28.7873u	g_m=27.795u g_{mQ}=28.958u

Now the task becomes : find the proper transistor aspect ratio *(W/L)* to achieve expected transconductance. According to eqn.(7.12), except aspect ratio, which is independent from the technology, the transconductance also depends on the K_{eff} and ΣV_t, which are process related parameters. Therefore, before choosing aspect ratios for the transistors, the technology parameters need to be specified first. The whole procedure of implementing the eighth-order bandpass filter is shown in the following flow-chart.

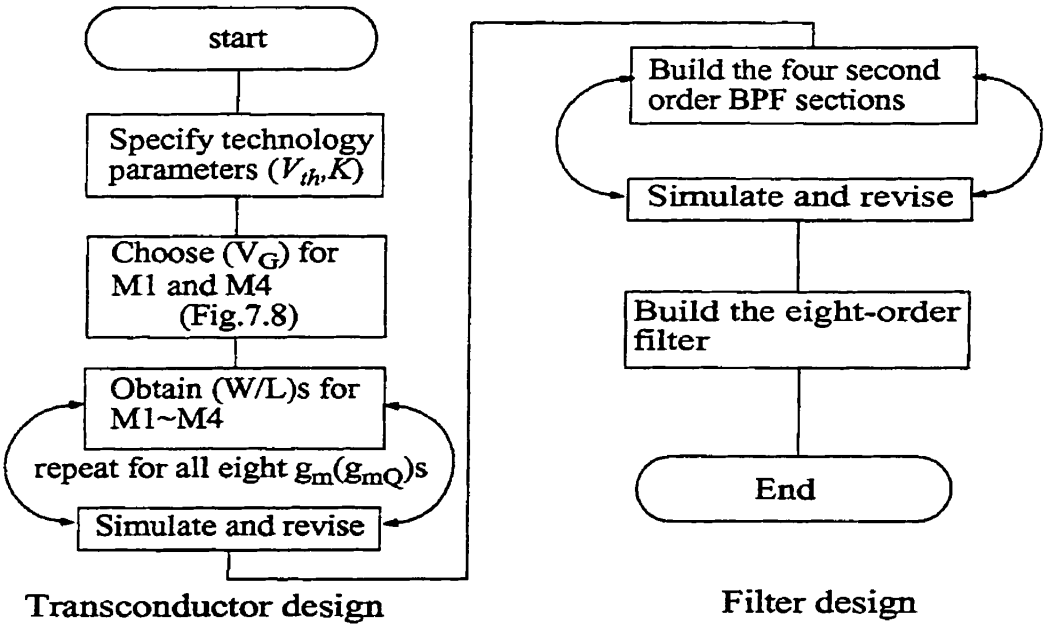


Fig. 7.11 Filter Design flow

In Fig. 7.11, the third step, where V_G for M1 and M4 are defined, is where the optimization methodology can fit in.

7.2.3 Theoretical calculations and HSPICE simulations

According to the design flow of Fig. 7.11, we first choose 1.5 μm CMOS technology to do the design. The process parameters are obtained as

$$V_{tn} = 0.8404V \quad V_{tp} = -0.7281V \quad \mu_p C_{ox} = 25.03\mu A/V^2 \quad \mu_n C_{ox} = 68.16\mu A/V^2$$

Assume $\left(\frac{W}{L}\right)_p = n\left(\frac{W}{L}\right)_n$. We found

$$K_{eff} = \frac{n(\mu_n C_{ox})(\mu_p C_{ox})}{2n(\mu_p C_{ox}) + 2(\mu_n C_{ox}) + 4\sqrt{n}\sqrt{(\mu_n C_{ox})(\mu_p C_{ox})}}\left(\frac{W}{L}\right)_n = \frac{1706n}{50.06n + 136.32 + 165.2\sqrt{n}}\left(\frac{W}{L}\right)_n \qquad (7.16)$$

The total threshold voltage ΣV_t of the transconductor (see Fig. 7.9) equals to *3.137V*. In section 7.2.1 we have found that the V_G, which will lead to best g_{ac}/P_{diss}, is *1.5685V*. In the following, we will choose two different V_G to design the transconductor and compare the power consumption of the eighth-order Chebyshev filter which is based on the transconductor. Since the supply voltages used by the original paper are ±5 V, we keep the same value for our analysis.

First trial, using $V_G = 2V$ and $n = 2$ (for eqn.(7.16)). Table 7.5 shows the calculated W/L ratios which correspond to the transconductances in Table 7.4.

Table 7.5 Calculated aspect ratios for the transconductances in Table 7.4

section 1	section 2	section 3	section 4
g_m: $(W/L)_n$=1.796 $(W/L)_p$=3.492 g_{mQ}:$(W/L)_n$=1.871 $(W/L)_p$=3.742	g_m: $(W/L)_n$=1.91 $(W/L)_p$=3.82 g_{mQ}:$(W/L)_n$=2.1 $(W/L)_p$=4.2	g_m: $(W/L)_n$=2.085 $(W/L)_p$=4.17 g_{mQ}:$(W/L)_n$=2.298 $(W/L)_p$=4.596	g_m: $(W/L)_n$=2.218 $(W/L)_p$=4.436 g_{mQ}:$(W/L)_n$=2.311 $(W/L)_p$=4.622

Choosing L=3u for all NMOS and PMOS transistors and doing HSPICE simulation, the simulated transistor aspect ratios and their corresponding transconductances are listed in Table 7.5.

Table 7.6 HSPICE simulated aspect ratios and corresponding transconductances

section 1	section 2	section 3	section 4
g_m: $(W/L)_n$=1.886 $(W/L)_p$=3.772 g_{mQ}:$(W/L)_n$=1.96 $(W/L)_p$=3.92	g_m: $(W/L)_n$=1.99 $(W/L)_p$=3.98 g_{mQ}:$(W/L)_n$=2.19 $(W/L)_p$=4.38	g_m: $(W/L)_n$=2.17 $(W/L)_p$=4.34 g_{mQ}:$(W/L)_n$=2.34 $(W/L)_p$=4.68	g_m: $(W/L)_n$=2.28 $(W/L)_p$=4.56 g_{mQ}:$(W/L)_n$=2.36 $(W/L)_p$=4.72
g_m= 22.555umho g_{mQ}=23.556umho	g_m=23.965umho g_{mQ}=26.695umho	g_m=26.468umho g_{mQ}=28.789umho	g_m=27.924umho g_{mQ}=29.062umho

When above simulated aspect ratios are used to implement the second order BPF sections, it is found that the location of the center frequency of each BPF is lower than the expected value. This is mainly due to the existence of the input parasitic capacitors of the input transistors. These parasitic capacitors are, in effect, parallel with the external capacitors (C1 and C2). Thus the effective capacitance of the filter becomes higher than the designed values. This phenomenon will be more obvious when larger transistors are used for the design as shown by the second trial. In order to achieve expected frequency performance, the transistors' aspect ratios are increased from the original ones to raise the transconductances. Table 7.6 gives the modified aspect ratios and the center frequency of each second order BPF section.

Table 7.7 Transistor aspect ratios and the center frequency of each section[1]

section 1	section 2	section 3	section 4
g_m: $(W/L)_n$=2.07 $(W/L)_p$=4.14 g_{mQ}:$(W/L)_n$=2.15 $(W/L)_p$=4.3	g_m: $(W/L)_n$=2.217 $(W/L)_p$=4.434 g_{mQ}:$(W/L)_n$=2.45 $(W/L)_p$=4.9	g_m: $(W/L)_n$=2.44 $(W/L)_p$=4.88 g_{mQ}:$(W/L)_n$=2.69 $(W/L)_p$=5.38	g_m: $(W/L)_n$=2.59 $(W/L)_p$=5.18 g_{mQ}:$(W/L)_n$=2.697 $(W/L)_p$=5.394
f_0= 3.5807MHz f_{sim}=3.556MHz	f_0= 3.809MHz f_{sim}= 3.776MHz	f_0= 4.158MHz f_{sim}= 4.17MHz	f_0= 4.4237MHz f_{sim}= 4.477MHz

1. f_0 represents expected center frequency of each BPF section. f_{sim} is the simulated center frequency of each section.

Implement the eighth-order filter by connecting the four sections in the sequence of : section 2->section 3->section 1->section 4 The reason that this sequence is adopted is to reduce the internal noise contributions of the filter (i.e., the section with lower values of f_0 and Q should precede that with higher values in the cascade connection [37]). The simulated center frequency and the bandwidth of the eighth-order Chebyshev filter is $f_0 = 3.98MHz$ and $BW = 650KHz$. The total simulated power dissipation is *532.813uW*. The simulated frequency-power ratio of the eighth-order Chebyshev filter is $f_0/P_{diss} = 7.5 \times 10^9 Hz/W$.

Now we take the frequency-power efficiency optimization of the Fig. 7.9 transconductor into consideration. We have found in section 7.2.1 that the best V_G for this particular transconductor is $\Sigma V_t/2 = 1.5685V$. In order for each transistor to operate in proper region, we take $V_G = 1.6V$ for the second trial and expect that the eighth-order Chebyshev filter based on this trial will consume less power dissipation than that of the first trial.

Using equal aspect ratio for NMOS and PMOS transistors (i.e., $n = 1$), the aspect ratios of the transistors in the transconductor of each section are shown in the first row of Table 7.8.

Table 7.8 Calculated aspect ratios for the transconductances in Table 7.4

section 1	section 2	section 3	section 4
g_m: (W/L)=36.8 g_{mQ}:(W/L)=38.34	g_m: (W/L)=39.14 g_{mQ}:(W/L)=43.126	g_m: (W/L)=42.736 g_{mQ}:(W/L)=47.084	g_m: (W/L)=45.46 g_{mQ}:(W/L)=47.36
g_m: (W/L)=14.12 g_{mQ}:(W/L)=14.66	g_m: (W/L)=14.94 g_{mQ}:(W/L)=16.33	g_m: (W/L)=16.197 g_{mQ}:(W/L)=17.72	g_m: (W/L)=17.15 g_{mQ}:(W/L)=17.815

While doing HSPICE simulation, it was found that the threshold voltages of NMOS and PMOS transistors are changing with the adjustment of transistor widths. This can be explained by the effective threshold voltage formula used by HSPICE(level=3) simulator, that is [38]

$$V_{th} = V_{t0} - \gamma\sqrt{\Phi} + \gamma f_s(\sqrt{\Phi + v_{sb}}) + \frac{8.14e-22 \cdot \eta}{C_{ox} \cdot L_{eff}^3} + f_n(\Phi + v_{sb}) \quad (7.17)$$

where V_{t0} is the zero-bias threshold voltage of a large device, γ is body effect factor, Φ is surface inversion potential, η is static feedback factor for adjusting the threshold. v_{sb} is the source-bulk voltage, f_s and f_n are parameters that describe short-channel and narrow-channel effect respectively. f_n is a function of effective channel width. It is the source of the dependency of threshold voltage on the channel width. In Fig. 7.9, the bulk terminal of each transistor is connected to its source terminal so that all transistors have zero-bias (i.e., $v_{sb} = 0V$). So eqn.(7.17) can be simplified as

$$V_{th} = V_{t0} - \gamma\sqrt{\Phi}(1 - f_s) + \frac{8.14e-22 \cdot \eta}{C_{ox} \cdot L_{eff}^3} + f_n\Phi \quad (7.18)$$

When substituting channel length of *3* μm into eqn.(7.17), for the 1.5 μm CMOS process, the short-channel term is found to be *0.02734V* and *0.03079V* for NMOS and PMOS transistor respectively. The narrow-channel term has the expression of $0.155388/(W_{eff} - 0.1279)$ and $0.1781/(W_{eff} - 0.2179)$ for NMOS and PMOS transistor respectively. The third term is much less than the other three terms and hence is neglected in the following threshold voltage estimation.

Assuming large channel widths are used for the transistors, the term associated with the narrow-channel effect in eqn.(7.18) becomes very small. The total effective threshold voltage of NMOS and PMOS transistors are *0.813V* and *-0.697V* instead of *0.8404V* and *-0.7281V*. Therefore, the analytical predictions obtained on the basis of $\Sigma V_t/2 = 1.5685V$, that is, $V_{thn} = 0.8404V$, $V_{thp} = -0.7281V$, are invalid. Substituting eqn.(7.18) (excluding the third term) into the g_m expression, we derived a new set of transistor aspect ratios for achieving desired ac transconductances. The results are listed in the second row of Table 7.8. If the channel widths are not large enough, for example, the values obtained in trial one, the narrow-channel term in eqn.(7.18) has the value close to that of the short-channel term. Therefore, the deviation of the total effective threshold voltage from V_{t0} is small. This is

the reason that the theoretical predictions obtained for trial one were close to the simulation results.

The aspect ratios obtained from simulation are given in the first row of Table 7.9. Similar to the first trial, the aspect ratios we have found from transconductor analysis do not provide the desired center frequency when the corresponding second order BPF is implemented. The revised values of aspect ratios which can meet the required filter center frequencies are given in the second row of Table 7.9.

Table 7.9 Simulated aspect ratios for transconductors of each section

section 1	section 2	section 3	section 4
g_m: (W/L)=18.7 g_{mQ}:(W/L)=19.4	g_m: (W/L)=19.8 g_{mQ}:(W/L)=21.7	g_m: (W/L)=21.5 g_{mQ}:(W/L)=23.6	g_m: (W/L)=22.8 g_{mQ}:(W/L)=23.7
g_m: (W/L)=38.67 g_{mQ}:(W/L)=40.17	g_m: (W/L)=42.53 g_{mQ}:(W/L)=44.2	g_m: (W/L)=50.73 g_{mQ}:(W/L)=52.7	g_m: (W/L)=60.77 g_{mQ}:(W/L)=63.1

Comparing the two sets of aspect ratios, the difference is remarkable. This is because the transistor widths are large for the second trial. Since a transistor's intrinsic parasitic capacitance is proportion to its area, the large transistor width results in bigger parasitic capacitances, which are in parallel with the external capacitors. These large intrinsic parasitic capacitance greatly increased the total capacitance of the filter [37] and hence reduced the center frequency of the filter by a large amount. In order to keep the center frequency at the desired value, the ac transconductance must be increased further and this is achieved by using even wider transistors. When the external capacitors are dominant, the relation between the center frequency of the filter and the transistors' width is almost linear, a proper set of transistors' widths can be found for certain frequency value. But if the intrinsic capacitors become dominant, both g_{ac} and C of the filter are in proportional to transistors' widths. So the frequency, which is determined by g_{ac}/C_{total} will be independent from transistors' widths and other techniques need to be employed to adjust the filter's frequency. For our design example, the external capacitors are remaining to be dominant in

the whole tuning range of transistors' widths. That is why we can obtain the desired center frequency by adjusting transistors' widths.

Cascading the four second order BPF sections in the sequence of (2,3,1,4), a eighth-order Chebyshev filter with center frequency of 3.98MHz and bandwidth of 690KHz is achieved. The simulated total power dissipation of the filter is *396.548uW*. Compared with *532.813uW* of trial one, the power dissipation of the second trial is reduced by 25%. The price paid for the frequency-power efficiency improvement is the increased transistor sizes. If the silicon area of the design is also a specification, one can choose the smallest V_G among those values that can meet the area requirement. By doing so, a higher frequency-power efficiency can also be achieved for the design.

7.3 Summary

In this chapter, the frequency-power efficiency optimization technique developed by previous chapters is applied to a very important transconductor-based analog signal processing system, that is, transconductor-C filter. First and second order transconductor-C filters are discussed. Three transconductor structures are used to implement second order filters. Analytical expressions and HSPICE simulations were conducted. A test chip is also fabricated using 0.35 μm CMOS technology. Test results are also provided in the chapter. Analysis, simulations and experiments show that by optimizing transconductor, the frequency-power efficiency of the filter can be improved (if not optimized).

A case study is also given in this chapter. The purpose of the case study is to demonstrate how to incorporate the optimization methodology into a design flow. The study also clearly revealed that by employing the optimization methodology, the power dissipation of an eighth-order Chebyshev filter can be reduced by 25% while the frequency performance retains. The trade-off of the power dissipation reduction is the area increasing. Thus, careful decision needs to be made according to the specifications of the design.

Chapter 8

Nonideality Consideration

The discussions in previous chapters are based on the assumption that the transconductors are operating in an ideal environment, that is, the temperature is stabilized at room temperature, the supply voltages and biases are fixed at the designed values, the noises are under tolerable limit. In addition, the geometric parameters as well as the process parameters of transistors are exactly what we have specified. However, in practice, the environment variations are unavoidable. For example, the temperature will increase by a certain rate as the operating time of electronic circuits increases. And it is impossible to physically implement two transistors with exactly the same parameters. That is why the capability of tuning is indispensable for an electronic circuit to operate properly. In this chapter, the issues of how the nonidealities affect the transconductor frequency-power optimization technique will be studied in a detailed manner.

8.1 Temperature drift

An important environmental variation is temperature drift. Although one can use special ways to stabilize the temperature outside of an IC chip, there is no way to control the temperature inside the chip. Since an IC chip consists of thousands of transistors internally, the longer these transistors are operating, the more heat they will produce and hence the higher the internal temperature will be. It has been known that most dc device parameters of MOS transistors change linearly or almost linearly with temperature. For instance, threshold voltage changes as -2 to -2.5mV/°C because of the changes of bandgap, intrinsic carrier density and junction potential. The transconductance element, $k = 0.5\mu C_{ox}(W/L)$, varies by $T^{-1.5}$ due to mobility changes. Around room temperature, k changes by 0.5 percent/°C[37]. These variations of parameters will definitely change the absolute values of the ac transconductance and dc power dissipation of a transconductor. Our concern here is how it

is going to affect the ratio of g_{ac}/P_{diss} and the optimal value of the controlling variable (i.e., χ).

8.1.1 Theoretical analysis

To find the temperature-induced changes of g_{ac}/P_{diss}, the partial differential equation of g_{ac}/P_{diss} with respect to temperature is considered.

$$\frac{\partial(g_{ac}/P_{diss})}{\partial T} = \frac{(\partial g_{ac}/\partial T)P_{diss} - (\partial P_{diss}/\partial T)g_{ac}}{P_{diss}^2} \tag{8.1}$$

To obtain the temperature coefficients of ac transconductance ($\partial g_{ac}/\partial T$) and dc power dissipation ($\partial P_{diss}/\partial T$), one needs to select the transconductor structure first. We will take balance-biased four-input-MOS transconductor structure (phase set 3) as an example. Other transconductor structures can be analyzed similarly. The g_{ac} and P_{diss} of balance-biased four-input-MOS transconductor have the expressions of eqns.(8.2) and (8.3) respectively.

$$g_{ac} = 2K(V_c + V_b - 2V_{th}) \tag{8.2}$$

$$P_{diss} = 2K[(V_c - V_{th})^2 + (V_b - V_{th})^2](V_{dd} - V_{ss}) \tag{8.3}$$

Differentiating eqns.(8.2), (8.3) with respect to T, we get

$$\frac{\partial g_{ac}}{\partial T} = \left[2\frac{\partial K}{\partial T}(V_c + V_b - 2V_{th}) + 2K\left(-2\frac{\partial V_{th}}{\partial T}\right)\right] \tag{8.4}$$

$$\frac{\partial P_{diss}}{\partial T} = \left\{2\frac{\partial K}{\partial T}[(V_c - V_{th})^2 + (V_b - V_{th})^2] + 2K\left[2(V_c - V_{th})\left(-\frac{\partial V_{th}}{\partial T}\right) + 2(V_b - V_{th})\left(-\frac{\partial V_{th}}{\partial T}\right)\right]\right\}(V_{dd} - V_{ss}) \tag{8.5}$$

where $\frac{\partial K}{\partial T} \cong -0.005K/°C$ around room temperature and $\frac{\partial V_{th}}{\partial T} = -2$ to $-2.5mV/°C$. So the temperature coefficient of the ac transconductance becomes

$$\frac{\partial g_{ac}}{\partial T} \cong 0.01K[1 - (V_c + V_b - 2V_{th})] \tag{8.6}$$

and the temperature coefficient of the dc power dissipation is

$$\frac{\partial P_{diss}}{\partial T} \equiv -0.01K(V_{dd}-V_{ss})[(V_c-V_{th})^2+(V_b-V_{th})^2-(V_c+V_b-2V_{th})] \tag{8.7}$$

Eqn.(8.7) shows that the power dissipation of the studied transconductor has negative temperature coefficient. Substitute eqns.(8.6) and (8.7) into eqn.(8.1), one can see that the temperature coefficient of g_{ac}/P_{diss} could be positive or negative depending on the temperature coefficient of g_{ac}. From eqn.(8.6), we see that the value of $\frac{\partial g_{ac}}{\partial T}$ is determined by the values of dc biases V_c and V_b.

The above analysis showed that the absolute value of the transconductor's g_{ac}/P_{diss} will vary as the environment temperature varies. However, as long as the shape of g_{ac}/P_{diss} remains unchanged, the differences of the absolute values are not very significant for our optimization methodology. But the variation of the controlling voltages which are needed to obtain optimal g_{ac}/P_{diss} is more important for the optimization technique. The reason is that if the values of the controlling voltages which correspond to optimal g_{ac}/P_{diss} are changed remarkably, they may be out of the physically acceptable voltage range. Thus an originally optimizable structure becomes non-optimizable due to the temperature drift. So we are hoping that the optimal controlling voltages of a transconductor are not too much sensitive to the temperature variation. For most voltage-biased transconductor structures we have discussed previously, their transconductance and DC power dissipation expressions are similar to eqn.(8.2) and eqn.(8.3). If transistors of the same type are sized identically, their g_{ac}/P_{diss}s will be independent of the Ks. Therefore the temperature coefficients of the optimal controlling voltages of these transconductors will only rely on the temperature coefficient of threshold voltage (V_{th}). Thus the variations of the optimal controlling voltages can be predicted by substituting the proper threshold voltage value into the corresponding formulas.

For transconductors whose g_{ac}/P_{diss} depend on both aspect ratio (K) and threshold voltage(V_{th}), the relation between optimal g_{ac}/P_{diss} and temperature drift can be analytically predicted by obtaining eqn.(8.1) for the corresponding structure and then substituting

$\frac{\partial K}{\partial T} \cong -0.005K/°C$ and $\frac{\partial V_{th}}{\partial T} = -2$ to $-2.5mV/°C$ into the expressions. The impact of temperature drift on the g_{ac}/P_{diss} optimization could be critical or non-critical depending on the structure of the transconductor.

Since the dependency of the optimal bias condition on the temperature drift of a transconductor structure can be analytically predicted, the optimization methodology will still be valid even with temperature drift. To include temperature drift into the optimization scheme, the aspect ratio (K) and the threshold voltage(V_{th}) in the objective function (i.e., g_{ac}/P_{diss}) have to be represented as temperature dependent variable (instead of the constants).

8.1.2 HSPICE Simulation

A HSPICE simulation is carried out to study the optimal controlling voltage at different operating temperature. Balance-biased four-input-MOS transconductor structures and single variable optimization procedure are employed for the simulations. The optimal controlling voltages at three different temperatures are obtained and listed in Table 8.1 .

Table 8.1 Optimal controlling voltages at different temperature

Transconductor	Temperature(°C)	Optimal controlling voltage V_{GS1} (V)
Phase set 1	0	≅ 0.88
	25	≅ 0.85
	75	≅ 0.774
Phase set 2	0	1.18
	25	1.13
	75	1.11

Table 8.1 Optimal controlling voltages at different temperature

Transconductor	Temperature(°C)	Optimal controlling voltage V_{GS1} (V)
Phase set 3,4,9	0	≅ 0.88
	25	≅ 0.85
	75	≅ 0.774
Phase set 5,6,8	0	1.6
	25	1.6
	75	1.6

For phase set 1 and phase set 3,4,9, the theoretical optimum presents at the threshold voltage of input NMOS transistors. The drift of threshold voltage with respect to the operating temperature can be clearly seen from the simulation results and is consistent with our approximation (i.e., *-2~-2.5mV/oC*). The optimal V_cs of phase set 2 at different temperature agreed with the calculated results very well. Since the optimal V_c of phase set 5,6,8 equals to the bias V_b and is independent from the threshold voltage, it does not change with temperature variation.

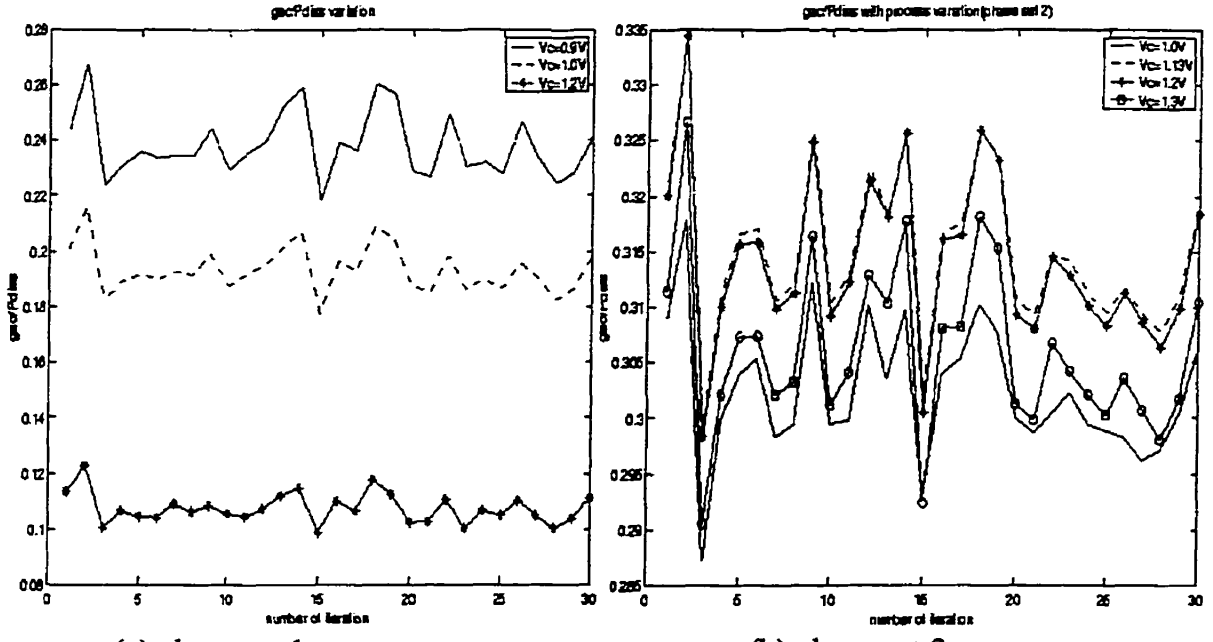
8.2 Process Variations

Process variations refer to the deviations of transistor parameters from their designed values due to the variations of semiconductor fabrication process. The most obvious process variations are geometrical variations. The channel length, width as well as the thermal oxide thickness between the polysilicon gate and the channel of a transistor will not be exactly the values as a designer specified. They are usually variating within certain range of the designed values. The statistical variation-ranges are different for different process technology. The influences of the process variation on a MOS transistor's performances are the drifts of threshold voltage, mobility, (W/L) ratio and the static drain current (I_{ds}). In Chapter 5, we have discussed mismatches of threshold voltage and K (i.e., $\mu C_{ox}(W/L)$).

These mismatches, in fact, are the results of process variations. The tables presented in Chapter 5 showed the second-order effect of mismatches on different CMOS transconductor structures. Now we will study the statistical effect of process variations on the g_{ac}/P_{diss} characteristic of CMOS transconductors. Still, we will use balance-biased four-input-MOS transconductors as example.

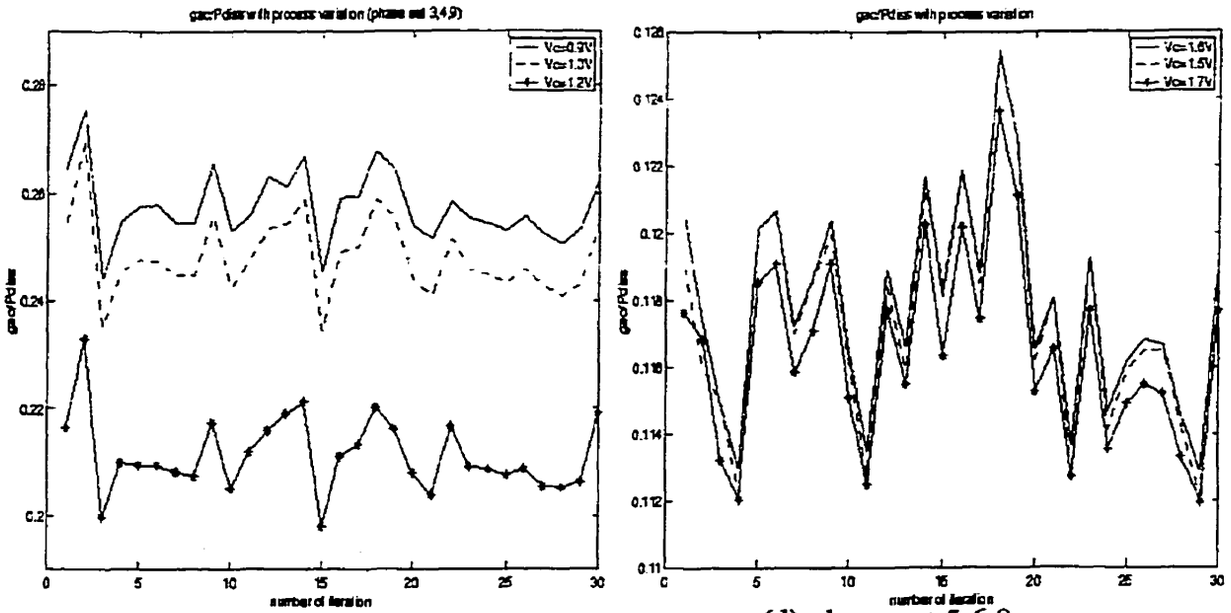
8.2.1 Monte Carlo Analysis

The statistical variations of the geometrical values can be modeled by Monte Carlo analysis. Monte Carlo analysis uses a random number generator to create several kinds of statistical distribution functions. Assume that the process variations of the critical geometric parameters (W_{eff}, L_{eff}) and the threshold voltages of NMOS and PMOS transistors have Gaussian distribution functions and the relative variations are around 5% of the nominal values. Fig.8.1 illustrates the distribution of g_{ac}/P_{diss} versus the choice of the bias voltage (V_c).



(a) phase set 1 (b) phase set 2

Fig. 8.1 g_{ac}/P_{diss} versus process variations



(c) phase set 3,4,9 (d) phase set 5,6,8

Fig.8.1 g_{ac}/P_{diss} versus process variations (Cont'd)

In Fig.8.1, the solid lines of (a),(c),(d) and the dash line of (b) correspond to the g_{ac}/P_{diss} of the transconductors at optimal biasing conditions. It can be seen that although the absolute value of g_{ac}/P_{diss} changes with the process variation, for any specific physical implementation (i.e., the parameters are fixed), the g_{ac}/P_{diss} optimization methodology and the results obtained in previous chapters are still valid.

8.3 Noise analysis

8.3.1 Theoretical analysis of transconductors' noise feature

The simplified noise model of a MOS transistor at low and medium frequency is given in Fig.8.2.

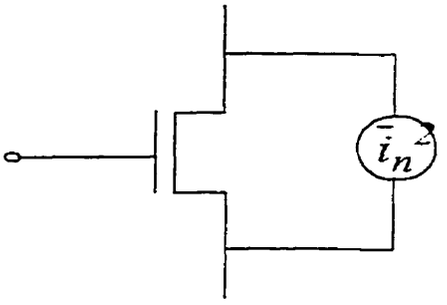


Fig.8.2 Noise model of MOS transistor

where $\overline{i_n}^2$ is the total noise current spectral density. The equation of $\overline{i_n}^2$ in Fig.8.2 includes thermal noise ($4kT(2/3)g_m$) and flicker noise ($kg_m^2/(WLC_{ox}f)$). g_m is the transconductance of the transistor [38], [5]. Replacing MOS transistors in transconductors by the model of Fig.8.2 and then draw the small signal equivalent circuits for the transconductors (see Fig.8.3), we can obtain the output noise current spectral density for different transconductor structures. In Fig.8.3, input transistors are assumed to be N-type and current-mirror type of active load is employed for saturated operating transconductor structures (i.e., the input transistors of the transconductors are operating in saturation region).

In Fig.8.3, g_{no} and g_{po} are drain-source conductance of NMOS and PMOS transistor respectively, g_{mp} is transconductance of PMOS transistor, i_n^2 and i_p^2 are noise current spectral density for NMOS and PMOS transistor respectively, v_n^2 is noise voltage spectral density and it depends on the structure of the transconductor. For Fig.8.3(a),

$$v_n^2 = (i_n^2 + i_p^2)(g_{mp} + g_{no} + g_{po})^2 \equiv (i_n^2 + i_p^2)g_{mp}^2 \tag{8.8}$$

For Fig.8.3(b),

$$v_n^2 = (i_{n1}^2 + i_{n2}^2 + i_p^2)(g_{mp} + g_{no1} + g_{no2} + g_{po})^2 \equiv (i_{n1}^2 + i_{n2}^2 + i_p^2)g_{mp}^2 \tag{8.9}$$

For Fig.8.3(c) and (d), v_n^2 can be expressed by eqns.(8.10) and (8.11).

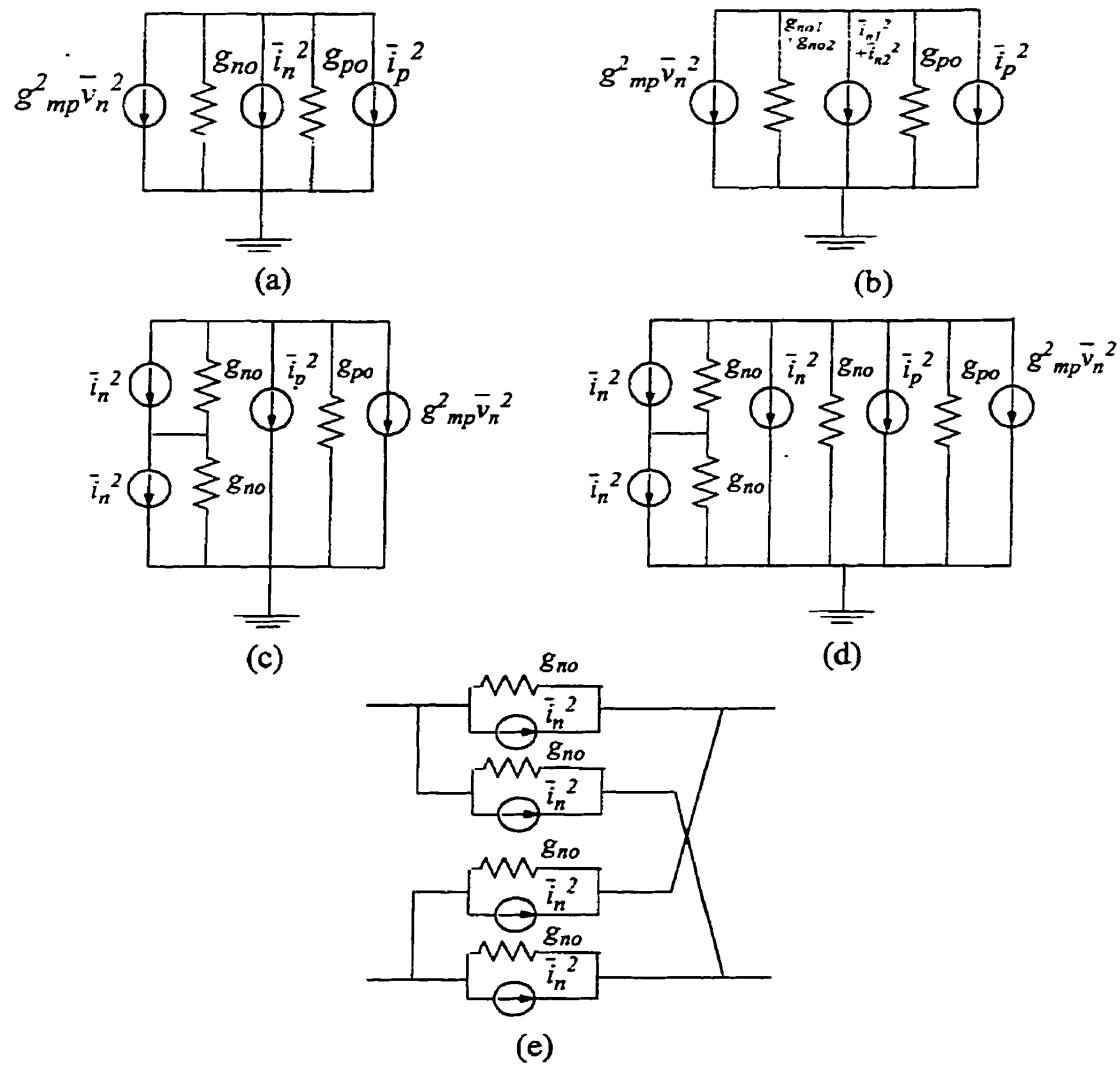


Fig.8.3 Small signal equivalent circuits of gate-biased transconductors for noise consideration : (a) Two saturated input-MOS structure (b) Four saturated input-MOS structure (c) Mixed input-MOS structure (Fig.3.7) (d) Mixed input-MOS structure (Fig.3.8) (e) Triode input-MOS structure

$$\bar{v}_n^2 = (g_{mp} + g_{po} + g_{no1} \| g_{no2})^2 (\bar{i}_n^2 + \bar{i}_p^2) \tag{8.10}$$

$$\bar{v}_n^2 = (g_{mp} + g_{po} + g_{no1} + (g_{no1} \| g_{no2}))^2 (\bar{i}_{n1}^2 + \bar{i}_{n2}^2 + \bar{i}_p^2) \tag{8.11}$$

From Fig.8.3 and equations (8.8) to (8.11), one can observe that the noise spectral densities of the transconductors are functions of large signal transconductance (g_m). Since g_m is proportional to the operating point of a transistor, which is determined by the dc biases of the

input transistors, the noise level will change when adjusting dc biases of a transconductor. In order to minimize output noise current spectral density, it is desirable to have smaller g_m. However, optimal bias condition does not necessarily correspond to minimum g_m, and besides, for practical application, certain amount of g_m needs to be reached for a transconductor to achieve its specifications. Thus, a transconductor usually has non-minimum noise. Therefore, for those transconductors whose optimal bias voltages can lead to small g_m, the noise effect is also reduced. But the price paid is that to achieve certain value of g_m, larger transistor sizes are needed. For the transconductors whose optimal bias voltages correspond to bigger g_m, the noise effect is increased. But the advantage of such transconductors is that small transistor sizes can be used to meet the g_m requirement.

In addition to the noises of transistors, there are noises from the positive and negative power supplies and other periphery circuits, such as the biasing circuit. As far as power-supply-induced noises of gate-biased transconductor structures are concerned, if designed properly, the power supply reject ratio (PSRR) can be made very high. For structures with lower PSRR, such as drain/source-biased transconductor, they are better to be employed in the applications that noise is not a great concern. The effect of periphery-circuit-induced noises can be equivalent to an input noise voltage sources of input transistors. Further, the input noise voltage source can be reflected to the output of the transistor and then included into the output noise current spectral density.

8.3.2 HSPICE Simulation

Simulating noise performances of gate-biased transconductor structures around their respective optimal biasing condition, we obtained the relation between output noise current and the frequency range of the input ac signal as shown in Fig.8.4.

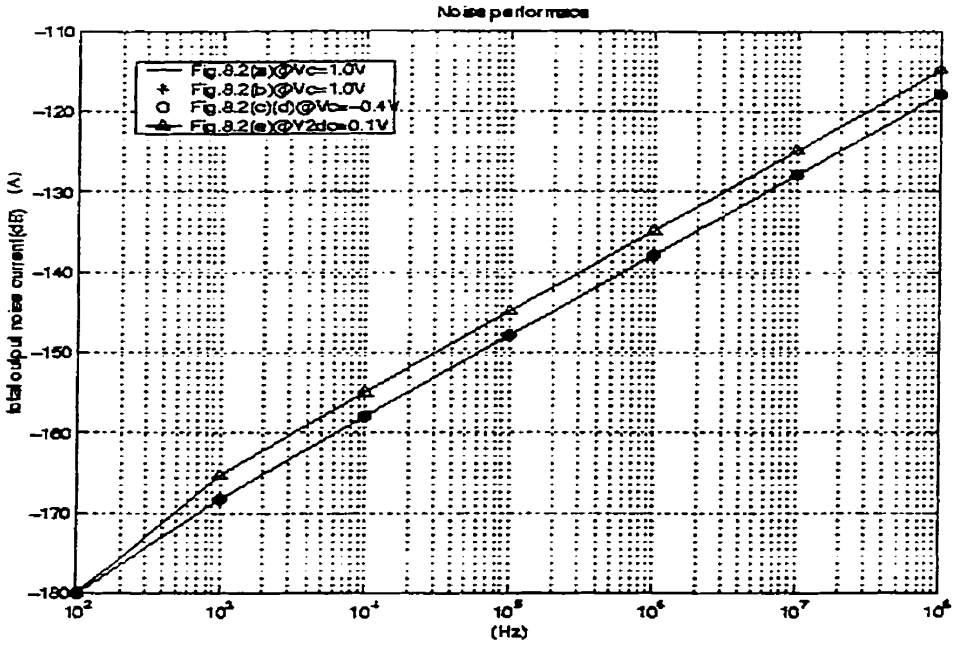


Fig.8.4 Noise performance of transconductors using small signal models in Fig.8.3

Because the circuit structure and the bias condition used are similar for Fig.8.3(a)-(d), their output noise current characteristics are very close to each other. The Fig.8.3(d) has distinctive structure and bias setting, therefore showed different noise characteristic. Obviously, wider input signal frequency range will lead to higher output noise current.

8.4 Short-channel/Narrow-channel consideration

All analyses and simulations of the preceding chapters and sections are based on transistors with longer channels. With the development of semiconductor technology, deep submicron level feature sizes are becoming available. The shrinking feature sizes make very high density integration to be a practical task. However, as the sizes are reduced, many second order factors, which were ignored by large feature-size circuits, must be taken into consideration.

A short-channel device refers to the device which has channel length (L) not much larger than the sum of the source and drain depletion widths. A narrow-channel device refers to the device which has channel width (W) not much larger than the depletion region depth

under the gate [5]. Both short-channel and narrow-channel devices need to be studied using two-dimensional analysis because a significant part of the electrical field lines have components along both x and y directions [5]. Thus modeling of short-channel and narrow-channel devices are more complicated than modeling of longer and wider channel devices. Many aspects of a device are affected when its channel length or width is decreased. The most significant effects associated with short- or narrow-channel devices are: mobility degradation, reduced r_{ds} (or channel length modulation) and hot carrier effects [38]. In chapter 5, we have discussed about the case of mobility reduction. This is taken care of by modifying the constant mobility μ_0 by an effective mobility μ_{eff} which has the expression of $\mu_0/(1+\theta V_{GS})$, where θ is a process determined parameter and V_{GS} is the gate-source voltage of the transistor. This modification is effective for long channel transistor model. When short-channel transistor is used, because of velocity saturation effect, the degradation of mobility is no longer linear. More complicated formulas are required to accurately describe the changes of mobility. The reduction of transistor's drain-source resistance (r_{ds}) for short- or narrow-channel transistor will make the channel length modulation to be more trouble-some and hence the linearity of a circuit will be degraded. Hot carrier effect is related to high electric field and is caused by the high energy electrons or holes (hot electrons or holes) which can enter oxide and are trapped in oxide. Such hot carriers accumulate with time and gradually degrade the device performance, such as increase the threshold voltage and decrease the control of the gate on the drain current [5]. Therefore, after some time, the performance of the device will be unacceptable.

The frequency-power-efficiency optimization methodology can also be applied to short-channel-device based electronic circuits. But the equations employed to describe the current-voltage transfer characteristic and the second-order effects must be modified using short-channel device model. Due to the complication and inaccuracy of short channel device model, the optimization task will never be easy to do manually. Computer-aided analysis will be the only way.

Since our work here is to illustrate the feasibility of the frequency-power-efficiency optimization methodology, to be on the safe side, we would like to see it works for long channel devices which are understood well and modeled accurately. Therefore all the theoretical analyses and the HSPICE simulations we have conducted in the previous chapters are based on long channel transistor models. The channel length of the transistors are chosen to be at least 6 times minimum feature size. The transistors of the fabricated chips are also designed to be long channel (i.e., at least 6 times minimum feature size).

8.5 Summary

This chapter discussed the practical nonideal issues and their influences on transconductor's frequency-power efficiency optimization methodology. HSPICE simulations are used to illustrate the effects of those nonideal factors quantitatively. This chapter also explains that on the purpose of evaluating a new optimization methodology (i.e., g_{ac}/P_{diss}), conservative designs are employed. Therefore short-channel or narrow-channel effects which are usually associated with more aggressive designs can be ignored and simple long-channel transistor models are used for all analyses in this work.

Chapter 9

Conclusion

A novel performance evaluation criterion, that is, the ratio of g_{ac}/P_{diss}, is proposed to describe the frequency-power efficiency characteristic of CMOS transconductors. Transconductors with input transistors operating in different regions were analyzed in terms of their g_{ac}/P_{diss} in a detailed manner. It was found that at certain biasing status, the g_{ac}/P_{diss}s can be optimized. The optimal biasing conditions of different transconductors were derived analytically and verified by numerical calculations, HSPICE simulations as well as experimental measurements.

On the basis of transconductor optimization, a more complicated transconductor-based analog system - transconductor-C filter was studied. Analyses showed that by employing the transconductor optimization technique, the frequency-power efficiency of the transconductor-C filter can also be improved if not optimized. HSPICE simulations and experimental tests were also performed. The test results were not satisfactory. It could because of the influence of various parasitic factors, such as the parasitic capacitance and resistance introduced by the pads, parasitic paths among different filter structures and so on. Since the testing issue wasn't taken into consideration while designing the filter chip, the exact reason of the discrepency and the distortions could not be pin pointed. A carefully designed self-testable filter circuit needs to be developed in order to obtain a successful test chip.

Other important design issues, such as the impacts of environmental variations, noises, etc, were also examined for the optimization methodology.

The proposed frequency-power efficiency optimization methodology revealed the feasibility and importance of improving analog circuit's performance-power efficiency, such as, frequency-power efficiency for transconductors (which has been discussed in this thesis),

gain-power efficiency for operational amplifier, bandwidth-power efficiency for filters, etc. By taking the performance-power efficiency into consideration, a circuit can be designed not only satisfying the required specifications but also providing higher performance-power efficiency. For example, when many biasing conditions can meet the required specifications, the one which will lead to highest performance-power efficiency of the circuit should be a good choice. Generally speaking, introducing the concept of performance-power efficiency gives designers more insight into the designs so that when they have some freedoms in designing a circuit, they can conveniently tune the design to better performance direction instead of randomly picking up a value.

This thesis covered most of the important issues of frequency-power efficiency optimization of CMOS transconductors. Future work will include

- investigating other transconductor-based analog systems;

By applying the optimization methodology to various transconductor-based analog systems, the effectiveness and the limitation of the scheme can be further examined. Thus, the algorithm of the optimization can be improved to provide better results.

- extending the methodology to short-channel/narrow-channel circuit implementations;

By doing so, the newly developed transconductor structures which are based on state-to-art technologies can also be optimized using the same concept.

- developing a CAD routine to enhance the automation of transconductor design;

This is an analog design automation issue. If we can quantitatively describe the main performances of transconductor structures, such as, transconductance, linearity, power dissipation, etc, we can build a knowledge-based transconductor library. When the design specifications are given, one or more transconductors can be chosen by comparing the performances they can provided with the performances required. If the performance-power efficiency of each transconductor is also stored in the library, it can be used for us to pick up a structure with higher performance-power efficiency.

- applying the optimization methodology, including the multivariable optimization

scheme, to other important building blocks, such as OPAMP, current conveyor, etc., to obtain higher performance-power efficiency.

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Appendix A

Optimal bias voltages for unbalance-biased gate-biased four-input-MOS transconductors

Phasing No.	Independent Case	Dependent Case
1 & 2	$V_{GS1\|opt} = V_{GS3} + \sqrt{(V_{GS3} - V_{diff} + V_{th})^2 + (V_{GS3} - V_{th})^2}$ $V_{GS3\|opt} = V_{GS1} + \sqrt{(V_{GS3} - V_{diff} + V_{th})^2 + (V_{GS1} - V_{th})^2}$ $V_{diff\|opt} = \left(\frac{V_{GS1} + V_{GS3}}{2}\right) - V_{th}$	$V_{r\|opt} = \sqrt{\frac{V_{th}^2 + (V_{diff} + V_{th})^2}{\alpha_1^2 + \alpha_2^2}}$ $V_{diff\|opt} = \frac{(\alpha_1 + \alpha_2)V_r}{2} - V_{th}$
3 & 4	$V_{GS1\|opt} = -(V_{GS4} - V_{diff} - 2V_{th}) + \sqrt{(V_{GS4} - V_{diff} - V_{th})^2 + (V_{GS4} - V_{th})^2}$ $V_{GS4\|opt} = -(V_{GS1} - V_{diff} - 2V_{th}) + \sqrt{(V_{GS1} - V_{diff} - V_{th})^2 + (V_{GS1} - V_{th})^2}$ $V_{diff\|opt} = \left(\frac{V_{GS1} + V_{GS3}}{2}\right) - V_{th}$	$V_{r\|opt} = x + \sqrt{y}$ $x = (2V_{th} + V_{diff})/(\alpha_1 + \alpha_2)$ $y = x^2 - \frac{2(V_{diff} + 2V_{th})V_{th}}{(\alpha_1^2 + \alpha_2^2)}$ $V_{diff\|opt} = \frac{(\alpha_1 + \alpha_2)V_c}{2} - V_{th}$
5 & 8	$V_{GS1\|opt} = -t_1 + \sqrt{(-t_1 - V_{th})^2 + b^2 + c^2 + d^2}$ $V_{GS2\|opt} = -t_2 + \sqrt{(-t_2 - V_{th})^2 + a^2 + d^2 + c^2}$ $V_{GS3\|opt} = -t_3 + \sqrt{(-t_3 - V_{th})^2 + a^2 + d^2 + b^2}$ $V_{GS4\|opt} = -t_4 + \sqrt{(-t_4 - V_{th})^2 + b^2 + c^2 + a^2}$ $t_1 = -V_{GS2} - V_{GS3} - V_{GS4} + 2V_{th}$ $t_2 = -\overline{-V_{GS1} + V_{GS3}} + V_{GS4} - 2V_{th}$ $t_3 = -V_{GS1} + V_{GS2} + V_{GS4} - 2V_{th}$ $t_4 = -V_{GS1} + V_{GS2} + V_{GS3} - 2V_{th}$ $a = (V_{GS1} - V_{th})$ $b = (V_{GS2} - V_{th})$ $c = (V_{GS3} - V_{th})$ $d = (V_{GS4} - V_{th})$	*
6 & 7	$V_{GS1\|opt} = -t_1 + \sqrt{(-t_1 - V_{th})^2 + b^2 + c^2 + d^2}$ $V_{GS2\|opt} = -t_2 + \sqrt{(-t_2 - V_{th})^2 + a^2 + d^2 + c^2}$ $V_{GS3\|opt} = -t_3 + \sqrt{(-t_3 - V_{th})^2 + a^2 + d^2 + b^2}$ $V_{GS4\|opt} = -t_4 + \sqrt{(-t_4 - V_{th})^2 + b^2 + c^2 + a^2}$ $t_1 = -V_{GS2} + V_{GS3} + V_{GS4} - 2V_{th}$ $t_2 = -V_{GS1} - V_{GS3} - V_{GS4} + 2V_{th}$ $t_3 = -V_{GS2} + V_{GS1} + V_{GS4} - 2V_{th}$ $t_4 = V_{GS1} - V_{GS2} + V_{GS3} - 2V_{th}$ $a = (V_{GS1} - V_{th})$ $b = (V_{GS2} - V_{th})$ $c = (V_{GS3} - V_{th})$ $d = (V_{GS4} - V_{th})$	*

Optimal bias voltages for unbalance-biased gate-biased four-input-MOS transconductors

Phasing No.	Independent Case	Dependent Case
9 & 12	$V_{GS1\|opt} = -r_1 + \sqrt{(-r_1 - V_{th})^2 + b^2 + c^2 + d^2}$ $V_{GS2\|opt} = -r_2 + \sqrt{(-r_2 - V_{th})^2 + a^2 + d^2 + c^2}$ $V_{GS3\|opt} = -r_3 + \sqrt{(-r_3 - V_{th})^2 + a^2 + d^2 + b^2}$ $V_{GS4\|opt} = -r_4 + \sqrt{(-r_4 - V_{th})^2 + b^2 + c^2 + a^2}$ $r_1 = V_{GS2} - V_{GS3} + V_{GS4} - 2V_{th}$ $r_2 = V_{GS1} - V_{GS3} + V_{GS4} - 2V_{th}$ $r_3 = V_{GS1} + V_{GS2} + V_{GS4} - 2V_{th}$ $r_4 = V_{GS1} + V_{GS2} - V_{GS3} - 2V_{th}$ $a = (V_{GS1} - V_{th})$ $b = (V_{GS2} - V_{th})$ $c = (V_{GS3} - V_{th})$ $d = (V_{GS4} - V_{th})$	*
10 & 11	$V_{GS1\|opt} = -q_1 + \sqrt{(-q_1 - V_{th})^2 + b^2 + c^2 + d^2}$ $V_{GS2\|opt} = -q_2 + \sqrt{(-q_2 - V_{th})^2 + a^2 + d^2 + c^2}$ $V_{GS3\|opt} = -q_3 + \sqrt{(-q_3 - V_{th})^2 + a^2 + d^2 + b^2}$ $V_{GS4\|opt} = -q_4 + \sqrt{(-q_4 - V_{th})^2 + b^2 + c^2 + a^2}$ $q_1 = V_{GS2} + V_{GS3} - V_{GS4} - 2V_{th}$ $q_2 = V_{GS1} + V_{GS3} - V_{GS4} - 2V_{th}$ $q_3 = V_{GS1} + V_{GS2} - V_{GS4} - 2V_{th}$ $q_4 = -V_{GS1} - V_{GS2} - V_{GS3} + 2V_{th}$ $a = (V_{GS1} - V_{th})$ $b = (V_{GS2} - V_{th})$ $c = (V_{GS3} - V_{th})$ $d = (V_{GS4} - V_{th})$	*
13 & 14	$V_{GS1\|opt} = -p_1 + \sqrt{(-p_1 - V_{th})^2 + b^2 + c^2 + d^2}$ $V_{GS2\|opt} = -p_2 + \sqrt{(-p_2 - V_{th})^2 + a^2 + d^2 + c^2}$ $V_{GS3\|opt} = -p_3 + \sqrt{(-p_3 - V_{th})^2 + a^2 + d^2 + b^2}$ $V_{GS4\|opt} = -p_4 + \sqrt{(-p_4 - V_{th})^2 + b^2 + c^2 + a^2}$ $p_1 = -V_{GS2} + V_{GS3} - V_{GS4}$ $p_2 = -V_{GS1} - V_{GS3} + V_{GS4}$ $p_3 = V_{GS1} - V_{GS2} - V_{GS4}$ $p_4 = -V_{GS1} + V_{GS2} - V_{GS3}$ $a = (V_{GS1} - V_{th})$ $b = (V_{GS2} - V_{th})$ $c = (V_{GS3} - V_{th})$ $d = (V_{GS4} - V_{th})$	*

Optimal bias voltages for unbalance-biased gate-biased four-input-MOS transconductors

Phasing No.	Independent Case	Dependent Case
15 & 16	$V_{GS1\|opt} = -o_1 + \sqrt{(-o_1 - V_{th})^2 + b^2 + c^2 + d^2}$ $V_{GS2\|opt} = -o_2 + \sqrt{(-o_2 - V_{th})^2 + a^2 + d^2 + c^2}$ $V_{GS3\|opt} = V_{GS4\|opt} = V_{th}$ $o_1 = V_{GS2} - 2V_{th}$ $o_2 = V_{GS1} - 2V_{t.}$ $a = (V_{GS1} - V_{th})$ $b = (V_{GS2} - V_{th})$ $c = (V_{GS3} - V_{th})$ $d = (V_{GS4} - V_{th})$	$V_{c\|opt} = l + \sqrt{l^2 + m}$ $l = 2V_{th}/(\alpha_1 + \alpha_2)$ $m = \frac{(c^2 + d^2 - 2V_{th}^2)}{(\alpha_1^2 + \alpha_2^2)}$ $c = (V_{GS3} - V_{th})$ $d = (V_{GS4} - V_{th})$
17 & 18	$V_{GS1\|opt} = V_{GS2\|opt} = V_{th}$ $V_{GS3\|opt} = -n_1 + \sqrt{(-n_1 - V_{th})^2 + b^2 + a^2 + d^2}$ $V_{GS4\|opt} = -n_2 + \sqrt{(-n_2 - V_{th})^2 + b^2 + c^2 + a^2}$ $n_1 = V_{GS4} - 2V_{th}$ $n_2 = V_{GS3} - 2V_{th}$ $a = (V_{GS1} - V_{th})$ $b = (V_{GS2} - V_{th})$ $c = (V_{GS3} - V_{th})$ $d = (V_{GS4} - V_{th})$	$V_{c\|opt} = l + \sqrt{l^2 + m}$ $l = 2V_{th}/(\alpha_1 + \alpha_2)$ $m = \frac{(b^2 + a^2 - 2V_{th}^2)}{(\alpha_1^2 + \alpha_2^2)}$ $a = (V_{GS1} - V_{th})$ $b = (V_{GS2} - V_{th})$

* In this case, the dependency can be assumed between any two of the four biasing voltages. For example, one can assume $V_{GS1} = \alpha V_{GS2}$ and $V_{GS3} = \beta V_{GS4}$ or $V_{GS1} = \alpha V_{GS3}$ and $V_{GS2} = \beta V_{GS4}$ with α, β being equal or unequal. Given an assumption, the optimum results can be easily derived according to case 2 of section I. However, the optimum results will be different with different assumptions. Therefore no general results can be given in the table.

Appendix B

1st, 2nd and 3rd order coefficients of v_{id} for Four-MOS unbalance-biased transconductors

phase	Second Order factor	Coefficient for v_{id}	Coefficient for v_{id}^2	Coefficient for v_{id}^3
set 1	mobility reduction	$2K_n(A-D)-3K_n\theta(A+D-V_{diff})(A-D)$ $A = V_{GS1}-V_{th}$ $D = V_{GS3}-V_{th}$ $V_{diff} = V_{GS1}-V_{GS2} = V_{GS3}-V_{GS4}$	0	$\frac{\theta K_n}{2}$
	mismatches	$2K_n(A-D)+\Delta K_a(V_{diff}-2\Delta V_{ta})$ $+\Delta K_b(V_{diff}-2\Delta V_{tb})$	$\frac{\Delta K_a-\Delta K_b}{2}$	0
set 2	mobility reduction	$2K_0(A+D)-3\theta K_0\left(A^2+D^2+(A-V_{diff})^2+(D-V_{diff})^2\right)$ $A = V_{GS1}-V_{th}$ $D = V_{GS3}-V_{th}$ $V_{diff} = V_{GS1}-V_{GS2} = V_{GS4}-V_{GS3}$	$\frac{3\theta K_0}{2}V_{diff}$	$-\frac{\theta K_n}{2}$
	mismatches	$2K_n(A+D-V_{diff})+\Delta K_a(V_{diff}-2\Delta V_{ta})$ $+\Delta K_b(V_{diff}-\Delta V_{tb})$	$\frac{\Delta K_a-\Delta K_b}{2}$	0
set 3	mobility reduction	$\zeta_n(A-B-D-E)+\frac{3\theta K_n}{2}\left(B^2-A^2+D^2+E^2\right)$ $A = V_{GS1}-V_{th}$ $B = V_{GS2}-V_{th}$ $D = V_{GS3}-V_{th}$ $E = V_{GS4}-V_{th}$	$\frac{\theta K_n}{4}$ *(-3B+3A+D-E)*	$\frac{3\theta K_n}{4}$
	mismatches	$K_n(A-B-D-E)+\Delta K_a(A+B)$ $-\Delta K_b(D-E-2\Delta V_{tb})$	$\frac{\Delta K_a-\Delta K_b}{2}$	0
set 4	mobility reduction	$K_n(A-B+D+E)+\frac{3\theta K_n}{2}\left(B^2-A^2+D^2-E^2\right)$ $A = V_{GS1}-V_{th}$ $B = V_{GS2}-V_{th}$ $D = V_{GS3}-V_{th}$ $E = V_{GS4}-V_{th}$	$\frac{\theta K_0}{4}$ *(3A-3B+5E-5D)*	$\frac{3\theta K_n}{4}$
	mismatches	$K_n(A-B+D+E-2\Delta V_{tb})+\Delta K_a(A+B)$ $-\Delta K_b(D-E)$	$\frac{\Delta K_a-\Delta K_b}{2}$	0
set 5	modifying set 4 coefficients by: V_4 replaces V_1, V_3 replaces V_2, V_1 replaces V_3, V_2 replace V_4			
set 6	modifying set 4 coefficients by: V_3 replaces V_1, V_4 replaces V_2, V_1 replaces V_3, V_2 replace V_4			
set 7	mobility reduction	$K_n(A-B+D-E)\frac{3\theta K_n}{2}\left(A^2-B^2+D^2-E^2\right)$ $A = V_{GS1}-V_{th}$ $B = V_{GS2}-V_{th}$ $D = V_{GS3}-V_{th}$ $E = V_{GS4}-V_{th}$	$\frac{\theta K_n}{2}$ *(B-A+D-E)*	0
	mismatches	$K_n(A-B+D-E-2\Delta V_{ta}-2\Delta V_{tb})$ $+\Delta K_b(D+E+2\Delta V_t)+\Delta K_a(A+B)$	$\frac{\Delta K_a-\Delta K_b}{2}$	0
set 8	same as unbalanced Two MOS coefficients			
set 9	modifying set 8 coefficients by: V_3 replaces V_1, V_4 replaces V_2			

Appendix C

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Multivariable optimization for Two MOS Unbalance-biased transconductor
%                    Ning Guo
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%-------------------------------------------------------------
% Objective function :
% P(X)=(-theta*X(1)^3+X(1)^2)+(-theta*X(2)^3+X(2)^2)*4*(-Vss)
% g(X)=(-3*theta*X(1)^2+2*X(1))+(-3*theta*X(2)^2+2*X(2))
% min f(X)=P(X)^2/g(X)^2
% subject to: 0<=X<=Vdd
% -theta*X(1)^3+X(1)^2-theta*X(2)^3+X(2)^2 /= 0
% constraint: DIS2=abs(Num1(X)/Den1(X)) < n%
% Num1(X)=3*theta*(X(1)-X(2))
% Den1(X)=4*(X(1)+X(2))-6*theta*(X(1)^2+X(2)^2)
% DIS3=abs(Num(X)/Den(X))<m%
% Num(X)=-theta
% Den(X)=Den1(X)
%  X(1)=Vgs1-Vth  X(2)=Vgs2-Vth
%  Pdiss/Gac=(Vdd-Vss)*sqrt(f(X))
%-------------------------------------------------------------
% ////////////// PART ONE : Obtain the theoretical graph /////////
%-------- Constants Vth=0.8V Vdd=-Vss=2.5V ----------
Vss = -2.5;
n = 0.01; % initial value for the percentage error
th = 0.041; % initial value for the theta
% Plot 3-D graph of Gac/Pdiss function
for i = 1:1:25
  counti(i) = i;
  a = 0.1*i;
  for j = 1:1:25
     countj(j) = j;
     b = 0.1*j;
     gp1(i,j)=(2*(a+b)-3*th*(a^2+b^2))/(10*((a^2+b^2)-th*(a^3+b^3))+0.0001);
```

```
  end
end
mesh(counti,countj,gp1);
xlabel('10*X1');
ylabel('10*X2');
zlabel('Gac/Pdiss(X1,X2)');
grid;
% ////////////// PART TWO : Optimization ////////////////////////////
%-------- Bounds ----------------------------
VLB = [0.01,0.01]; % Lower bounds X>0.01
VUB = [-Vss,-Vss]; % Upper bounds X<-Vss
%---------Initial guess  ----------------------
x0 = [0.01,0.01];
%---------Define global variables ---------------
global th
global n
%--------  Objective function (M-file)-------
type m2u_objfun
%--------  Constraints Function (M-file)
type m2u_confun
%--------- Set optimization options:-----------
% Turn off the large-scale algorithms (the default)
% and turn on the Display of results at each iteration:
options = optimset('LargeScale','off','Display','iter');
% We have no linear equalities or inequalities, so pass [] for those arguments
[x,fval,exitflag,output]=fmincon('m2u_objfun',x0,[],[],[],[],VLB,VUB,'m2u_confun',options);
%--------  Show current x and constraints
x
[cu, cueq] = m2u_confun(x)
%--------- Modifying the constraints to get an acceptable result-------------
while ((max(cu(1),cu(2))>(n+0.01))&(n<=0.1))
global n
n = n+0.01;
[x,fval,exitflag,output]=fmincon('m2u_objfun',x0,[],[],[],[],VLB,VUB,'m2u_confun',options);
x
[cu, cueq] = m2u_confun(x)
```

```
end
%---------- Checking the nonzero property of the denominator ----------
if (abs('m2u_num')<=1e-04)
disp('Error: Zero Denominator!');
else
%---------- Checking the feasibility of the results ----------
if (x(1)>=2.8|x(2)>=2.8)
    disp('Out of upper bound');
elseif (x(1)<0|x(2)<0)
    disp('Out of lower bound');
else
    disp('terminate successfully');
end
% ////////////// PART THREE : Printout the results ////////////////////
%******* The solution is: ************************************
x
%******* The function value at the solution is: **************
fout = 1/(5*sqrt(fval)) % fout=(g/P)
%******* The total number of function evaluations is:***********
iter_num = output.funcCount
%******* The value of constraint ***************************
[cu, cueq] = m2u_confun(x)
n
end
```

Appendix D

1. Test circuit set up for multivariable constrained transconductor optimization

Figure D-1 illustrates the testing set up and the connections between the test equipments and the test chip.

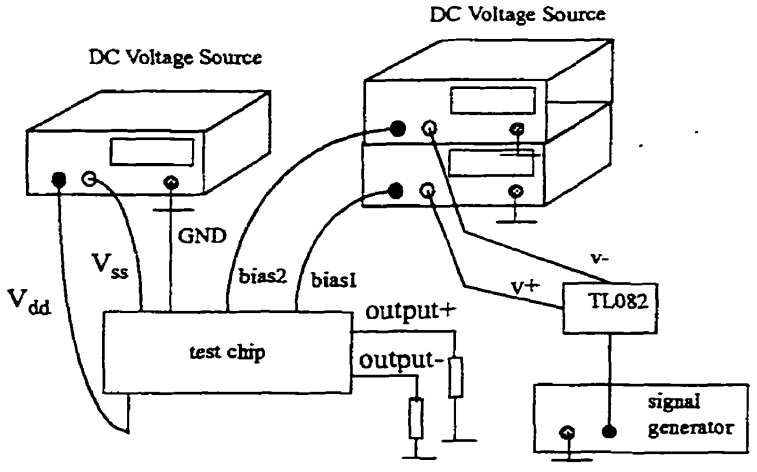

Figure D-1 Transconductor g_{ac}/P_{diss} testing set up

In Figure D-1, TL082 is used to invert the ac signal coming from signal generator so that differential ac inputs can be achieved. The reason that *v+* also uses the output of TL082 is to make *v+* and *v-* terminals present similar input impedence. The transconductance equals to the difference of the two output ac voltages dividing the load resistance. The DC power dissipation is obtained by measuring the DC current and then multiplying the current by the supply voltage (i.e., 2.5-(-2.5)=5V).

2. Test circuit set up for linearity measurement

Figure D-2 illustrates the test circuit set up employed for measuring the linearity character-

istic of various transconductors.

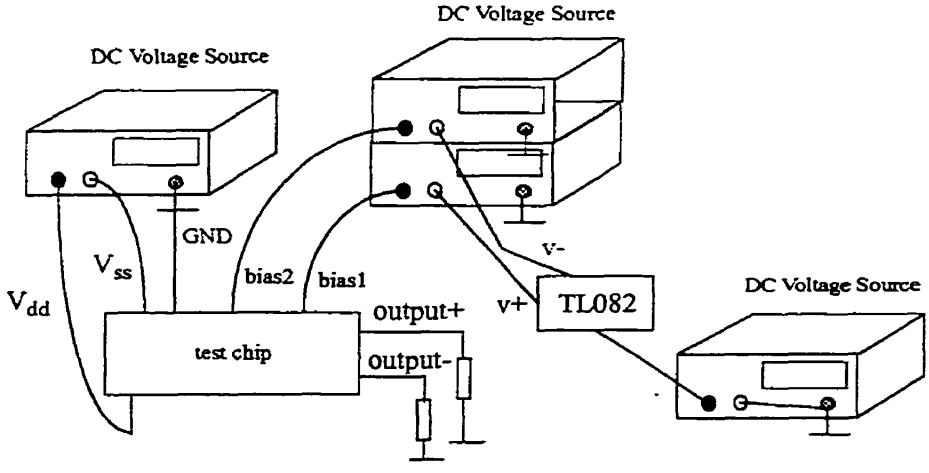

Figure D-2 Testing circuit set up for linearity measurement

TL082 is also used to provide differential DC input signal. The input DC signal changes from -1V to +1V, the difference between the two output voltages ($v_{output+} - v_{output-}$) are measured. The transconductance can be obtained by dividing the output voltage difference by the load resistance.