

THE UNIVERSITY OF CALGARY

**CMOS Analog Signal Processing for a Smart  
Antenna System**

by

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A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES  
IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE  
DEGREE OF MASTER OF SCIENCE

DEPARTMENT OF ELECTRICAL AND COMPUTER  
ENGINEERING

CALGARY, ALBERTA

October, 1999

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0-612-49671-6

# Abstract

Limited bandwidth and the demand for increased capacity on wireless systems has prompted new schemes of multiple access. The smart antenna is one such tool that is currently under development at the TR Labs Wireless Research Center in Calgary.

This thesis describes how an analog implementation can be included in the signal processing of a smart antenna system. In order to increase the data rates and to reduce the load on software components of the overall system, dedicated integrated circuits are investigated. The specific building block discussed in order to incorporate analog components is that of a four-quadrant multiplier, the R-2R Ladder.

The issues regarding component sizes, bandwidth, linearity, distortion and overall accuracy are discussed. Comparison is made between simulation and measurement on fabricated multiplier cells. Precautions that must be noted in order to achieve a successful full-scale implementation are elaborated and the suitability of the specific multiplier cell is discussed.

## Acknowledgements

I thank my supervisor Dr. J.W. Haslett for his guidance and encouragement. Special acknowledgement must be given for his advice and allowance for me to learn from my own mistakes. Also, his generous financial support was greatly appreciated.

I am additionally grateful for the financial assistance provided by NSERC, the Telecommunications Research Laboratories and the Department of Electrical and Computer Engineering.

Great appreciation is given towards Dr. Ivars Finvers and Dr. Brent Maundy. Their input allowed me to increase my understanding of how to attack and solve various circuitry problems.

Sincere thanks are due to the many friends that I have made during my studies. Too numerous to mention, their support and encouragement allowed me to maintain my sanity. In particular I would like to thank Saeed Aghtar, Wei Huang and Caitlin Davis for the many useful discussions that we had.

The help of the technical staff was fantastic during the completion of this project. Thanks must be given to Ed Evanik and John Shelley for their comments and assistance during the duration of my studies.

I am grateful to the Canadian Microelectronics Corporation for the assistance that was given in the fabrication of various integrated circuits. The support given to the VLSI Group make it possible for the completion of many of the projects here.

Most important of all, my father has always been there to support me no matter what decisions I made. Words alone can not express my feelings towards what he has done for me. The sacrifices he has made did not go unnoticed, and I am forever grateful.

*To My Family*  
*Past and Present*

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# List of Symbols and Abbreviations

$\gamma$	Body-effect coefficient
$\Delta T$	Temperature deviation from nominal
$\epsilon_{ox}$	Permittivity of silicon dioxide, pF/cm
$\phi$	Input state of bits, labelled $\phi_n$ to $\phi_1$
$\phi_p$	Bulk potential
$\phi_o$	Built-in potential of a p-n junction
$\mu_n$	Electron mobility
$\mu_p$	Hole mobility
a	Wiper setting of potentiometer
A/D	Analog to Digital
C	Various capacitor values
$C_j$	Total junction capacitance per unit area of a p-n junction
$C_{jo}$	Junction capacitance per unit area of a p-n junction at zero bias
CMC	Canadian Microelectronics Corporation

$C_{oxide}$	Oxide capacitance of MOS transistor
$D_{\#}$	Denominator coefficient of adjustable current mirror
D-FF	D-type flip-flop
DMI	Direct Matrix Inversion
DSP	Digital Signal Processor
HD	Harmonic Distortion
$I_1, I_2, I_3, I_4$	Input currents to Raytheon
i, r	Imaginary, real components
$i_c$	Current caused by parasitic capacitance
IC	Integrated Circuit
$I_C$	Collector current
$I_{ES}$	Reverse saturation current
$I_{in}$	Input current
$I_{out}$	Output current
I/Q	Inphase/Quadrature
k	Boltzmann's constant, $1.38 \times 10^{-23}$ J/K
K	Scaling factor of analog multiplier
$L_{eff}$	Effective length of drawn device
LD	Lateral diffusion
LSB	Least significant bit
LMS	Least Mean Squares algorithm
$\mathcal{M}$	Number of receiving elements
M	Maximum gain for adjustable current mirror

MSB	Most significant bit
n	Number of bits
$\mathcal{N}$	Number of transmitters
$N_{\#}$	Numerator coefficient of adjustable current mirror
q	Electron charge, $1.6 \times 10^{-19}$ C
$Q_p$	Charge on parasitic capacitance
QPSK	Quadriphase Shift Keying
R	Resistor
$R_{diffusion}$	Sheet resistance of diffusion resistors
RF	Radio Frequency
RLS	Recursive Least Squares
$R_o$	Resistance value of drawn resistor
$R_{on}, (R_{on})_n, (R_{on})_p$	Channel-resistance of switch
$R_{poly}$	Sheet resistance of poly resistors
$R_s$	Sheet resistance
$R_{total}$	Total resistor value
$R_{TG}$	On-resistance of transmission gate
SAS	Smart Antenna System
SO	Signal Output
$t_f$	Fall time
$t_{ox}$	Oxide thickness, cm
$t_{pL-H}, t_{pH-L}$	Propagation delay of low-to-high and high-to-low transistion, respectively



$t_r$	Rise time
T	Temperature, K
$T_{C1}, T_{C2}$	Temperature coefficients of resistors
$T_{I/Q}$	Total number of multipliers for output signal
THD	Total Harmonic Distortion
$T_{Mult}$	Total number of multipliers
U	Received Signals
$v$	various node voltages
$V_{BE}$	Base-emitter voltage of bi-polar transistor
$V_{DD}, V_{SS}$	Power supply rails
$V_{DS}$	Drain-to-source voltage
$V_{in}$	Input voltage
$V_{GS}$	Gate-to-source voltage
$V_{out}$	Output voltage
$V_R$	Reverse-bias voltage on p-n junction
$V_{SB}$	Source to bulk voltage
$V_t$	Thermal voltage, 0.026 V
$V_{Tn}, V_{Tp}$	Threshold voltages
$V_{TON}, V_{TOP}$	Threshold voltage with $V_{SB} = 0$ , for n and p-type
$W_{\#, \#}$	Applied weights
W, L	Width and Length of an MOS transistor
$W_{eff}$	Effective width of drawn device
X, Y	Input variables of analog multiplier
Z	Multiplier output

# Chapter 1

## Introduction

Through a collaborative effort a Smart Antenna System is being developed at the Telecommunications Research Laboratories (TR Labs), Calgary office. The project has been and is presently being worked on by various graduate students. The abundance of effort and interest in this project is a result of the advantages offered by a smart antenna. For this thesis the discussion is directed to the current system under development, specifically a smart receiver.

Due to the ever-increasing number of users on any given wireless system, a smart antenna system has advantages. The smart antenna allows for multiple transmitted signals to be received over the same frequency band. It also provides benefits such as signal acquisition and tracking, it allows for increase in system capacity and a resulting data rate increase, and provides wireless internet connections [1, 2, 3]. In order to better understand the overall capabilities of the smart antenna system, the overall signal processing is discussed.

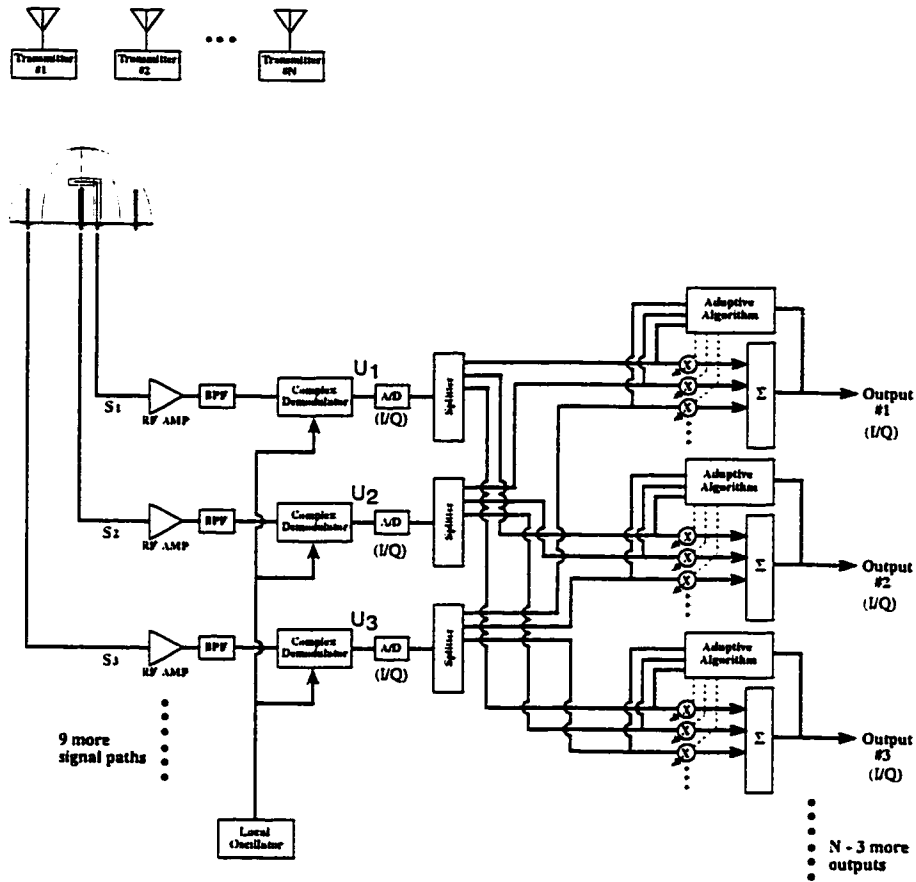


Figure 1.1: Smart Antenna System.

### 1.1 Current Signal Processing

The overall implementation of the system is shown in Figure 1.1, taken from [4]. The system has multiple stages that have been implemented through various hardware and software components. All transmitted signals are modulated on the same carrier frequency. Initially the transmitted signals are received by the antenna array, which has multiple receiving elements. Each of the antenna elements receives components of all the transmitted signals, because of co-channel interference as illustrated in Figure 1.2. The number of received signals is dependent on the number of elements on the

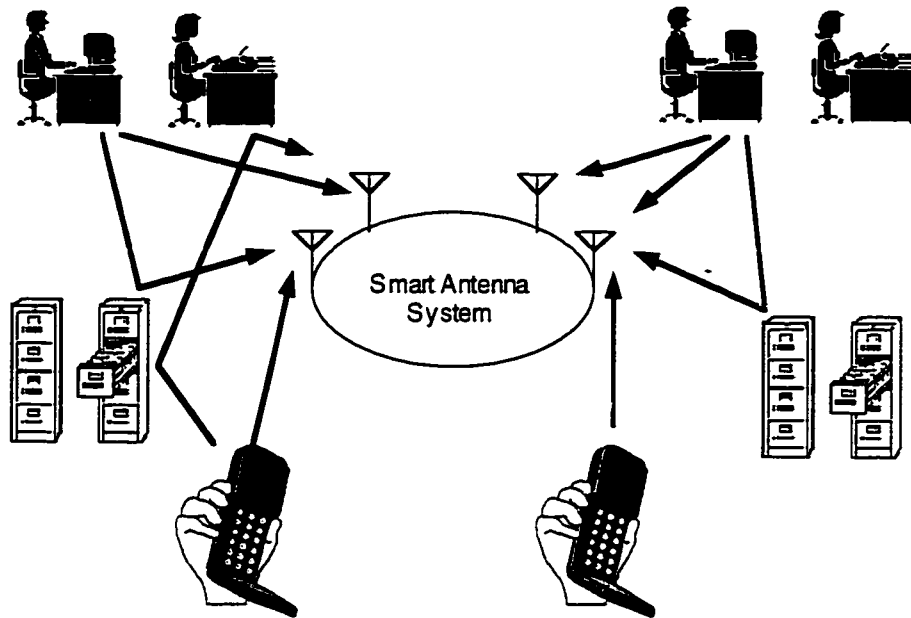


Figure 1.2: Co-Channel Interference.

receiving antenna array. Each received RF signal ( $S_1, S_2, \dots$ ) is then amplified and passed through a band-pass filter.

The RF signal is then demodulated to the baseband signal, via complex demodulators. The data transmission is quadriphase shift keying (QPSK), and therefore the demodulated signals are an Inphase/Quadrature (I/Q) pair modulated onto a sine/cosine carrier. With each received demodulated signal, the reconstruction of the original transmitted signal can begin. In order to recombine the received signals to the transmitted signals, a weighted summation of all I/Q signals is required. This is necessary in order to suppress, by selection of weights, all interfering received elements and isolate each single transmitted signal.

Each of the various signals is weighted through multipliers which are then appropriately combined to produce a recovered transmitted signal. The signal pro-

cessing can be done either in a digital or analog domain. In order to complete the overall signal processing for a given system the total number of multipliers required can be expressed as:

$$T_{Mult} = (2\mathcal{N}) \cdot (2\mathcal{M}) \quad (1.1)$$

where  $\mathcal{N}$  and  $\mathcal{M}$  represent the number of transmitters and receiving elements, respectively. Therefore, for each transmitted signal the required number of multipliers to produce the combined signal, I/Q pair, can be expressed by the following:

$$T_{I/Q} = 2 \cdot 2 \cdot \mathcal{M} \quad (1.2)$$

A more detailed illustration of the reconstruction of the output signals is shown in Figure 1.3 [5]. This diagram clarifies the number of required multipliers for any given system. It also makes apparent the need for splitters in order to reconstruct all output signals, as seen in Figure 1.1.

The recombination of the received signals is weighted in the following manner.

$$\begin{bmatrix} SO_1 \\ SO_2 \\ \vdots \\ SO_{\mathcal{N}} \end{bmatrix} = \begin{bmatrix} W_{1,1} & W_{2,1} & \cdots & W_{\mathcal{M},1} \\ W_{1,2} & W_{2,2} & \cdots & W_{\mathcal{M},2} \\ \vdots & \vdots & \ddots & \vdots \\ W_{1,\mathcal{N}} & W_{2,\mathcal{N}} & \cdots & W_{\mathcal{M},\mathcal{N}} \end{bmatrix} \cdot \begin{bmatrix} U_1 \\ U_2 \\ \vdots \\ U_{\mathcal{M}} \end{bmatrix} \quad (1.3)$$

where SO represents the output channels, U values are baseband received signals and W values are applied weights. Since the transmission is QPSK each baseband signal is modulated onto a sine and cosine carrier. These orthogonal signals can be represented by [6]

$$U_k = (U_k)_r + j(U_k)_i \quad k = 1, 2, 3 \dots \quad (1.4)$$

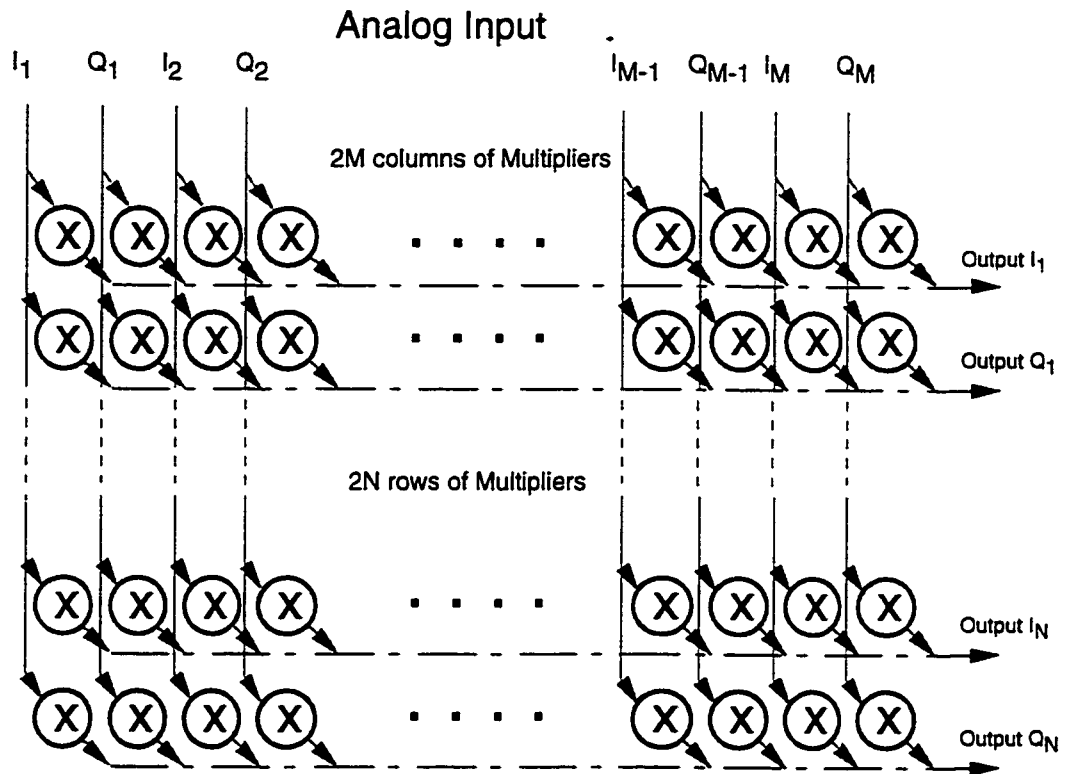


Figure 1.3: Combining of Received Signals.

where  $r$  and  $i$  indicate real and imaginary components which are interchangeable with quantities of  $I$  and  $Q$ . In addition, the weights can be written as

$$W_{k,1} = (W_{k,1})_r + j(W_{k,1})_i \quad k = 1, 2, 3 \dots \quad (1.5)$$

By performing the complex matrix multiplication, the first output signal (Output #1) can be re-written as,

$$SO_1 = [(W_{1,1})_r + j(W_{1,1})_i] \cdot [(U_1)_r + j(U_1)_i] + \dots \quad (1.6)$$

which can be resolved into the complex components of

$$(SO_1)_r = (W_{1,1})_r \cdot (U_1)_r - (W_{1,1})_i \cdot (U_1)_i + \dots \quad (1.7)$$

and

$$(SO_1)_i = (W_{1,1})_r \cdot (U_1)_i + (W_{1,1})_i \cdot (U_1)_r + \dots \quad (1.8)$$

The selection of all weights is accomplished by an adaptive algorithm, which must continuously update each weight in order to allow for changes in received signals. As the positioning of the transmitters changes, the resulting multi-path interference changes. Thus, the signal processing must constantly adapt in order to ensure cancellation of the interfering signals.

### 1.1.1 Specifics on Current System

The RF transmitted carrier frequencies are all 1.7 GHz, for the system's receiving antenna [7]. The current system allows up to eight transmitters and twelve receiving elements. The maximum number of baseband signals, results in 12 I/Q pairs or 24 analog signals in total.

The process of calculating the individual weights has been previously implemented in software by another MSc. student, Keith Winand. The methods of calculating the weights will not be discussed here, but can be found in reference [6]. The adaptive algorithms that were presented in that work included: least means squares algorithm (LMS), recursive least squares algorithm (RLS), and the direct matrix inversion algorithm (DMI).

The combining of the received signals can be done in either an analog or digital domain. For the initial implementation the signal processing was done via software. In Figure 1.1 the point at which all processing is done in software is after the input signals are sampled by the analog-to-digital converters (A/D). The system consisted

of a Macintosh Quadra 700 computer and a 33 MHz Texas Instruments TMS320C30 DSP [8] for the real-time signal processing. Also included in the computer were two dedicated PC boards [6]. The A/D converters were all sampled synchronously to allow for processing to be done by the DSP. In addition, in order to process the data, the various adaptive algorithms used to calculate the different signal weights were performed using Matlab. The resulting output signals were reconstructed in a purely software domain. The system was able to process data rates between 10 kHz and 20kHz.

For the initial implementation of the Smart Antenna System, an increase in the number of transmitted signals would reduce the speed at which the output signals could be processed. Thus, in order to increase the number of transmitters without decreasing the data rate of the processed signals it would be required that the computer and DSP hardware speed be increased.

## 1.2 Proposed Analog Signal Processing

The objective of the analog signal processing is to introduce added circuitry which will perform the reconstruction of the transmitted signal. The analog signal processing will eliminate the computer required by the system, and allow for an increase in the data rates which can be processed. This can be understood since the data rate is dictated by the number of floating point operations required to process the output channels in a purely digital domain.

Due to the limitations on the availability of resources in fabrication grant space, an implementation has been chosen that will allow for up to 4 transmitters and 6 receivers. While only allowing for a system that is one-half of the maximum size,



concern must be placed on further expansion, ie. an increased number of transmitter and receiving elements. Therefore, it was necessary to make a design that allowed for upgrading without a large amount of extra hardware or the need for redesign. Thus, modularity was a an overall concern.

From 1.1 the number of multipliers required by the proposed implementation was nintey-six, while the maximum system capacity would require ( 8 transmitters, 12 receiving elements) 384 multipliers. The analog implementation was therefore designed such that the overall structure could be simply expanded to handle the extra requirements.

### 1.2.1 Customized Integrated Circuits

A feasible solution for the implementation of the analog signal processing is in the design and fabrication of dedicated integrated circuits (IC's). Since the University of Calgary is a participant in the University Program with the Canadian Microelectronics Corporation (CMC), access is available to various fabrication processes; Mitel 1.5  $\mu\text{m}$  CMOS, Mosis 0.5  $\mu\text{m}$  CMOS and TSMC 0.35  $\mu\text{m}$  CMOS [9]. With the use of dedicated IC's, the weighting and routing of the all baseband signals can be done on-chip. Presented in this work is the suggested implementation for the multiplier cells with the use of dedicated chips.

The specifications for the multiplier cell are outlined in Table 1.1 [10].

Each of the input signals (I and Q) will have a range of  $\pm 1V$ , however after the final combination output channels were to attain levels of  $\pm 2V$  [11].

An additional requirement for the fabricated chip is the clock speed that will be required for the updating of multiplier weights from the DSP. For the first imple-

<i>Characteristic</i>	<i>Requirement</i>
Gain Range	0:1
Linearity or Repeatability	1 %
Harmonic Distortion	1 %
Bandwidth	20 MHz
Input Range	$\pm 1$ V
Range of Combined Output Signal	$\pm 2$ V

Table 1.1: Specifications for Multiplier Cells .

mentation, the goal was to allow for speeds of 1 MHz [11].

### 1.2.2 Additional Hardware

With the addition of the dedicated chips, additional circuitry will also be required. In the original system the DSP monitored the input signals via A/D converters. Correlation of the input and output signals was easily done since the software reconstruction allowed for instant access to output signals. When dedicated IC's are introduced, it is necessary to add the required A/D converters in order to also sample the reconstructed transmitted signals.

## 1.3 Overview

With an understanding of the analog signal processing requirements, Chapter 2 is presented as an overview of the various types of analog multipliers that were considered. The benefits and concerns of the multiplier cells, with regards to the specified requirements, are discussed. In addition details are given to decide which fabrication processes are acceptable. Included is an investigation of an adjustable cell that had been previously fabricated.

The building blocks having been discussed, Chapter 3 describes the chosen method of implementation. Specifics are given for the IC's that were submitted for fabrication. As well, digital circuitry required to control the multipliers is presented, and the implementation to allow for modularity is described.

Included in Chapter 4 are the results from the testing of the implementation. The maximum attainable 3 dB bandwidth of the fabricated IC's is compared with simulation. The digital circuitry was also tested in order to illustrate that the fabricated chip could update weights of the multipliers at the required clock speed.

Finally in Chapter 5 conclusions and further improvements for the system are given.

## Chapter 2

# Analog Multipliers

In order to perform the analog signal processing required for the smart receiver, specific devices need to be investigated. This chapter describes various methods of implementation using analog multipliers, hereforth called multipliers. When making a selection, thought must not only be given to suitability from a signal processing point of view, but to the physical implementation. The CMOS fabrication resources that were available included the following technologies: Mitel 1.5  $\mu\text{m}$ , Mosis 0.5 $\mu\text{m}$ , TSMC 0.35  $\mu\text{m}$ . When making a choice of technologies, the timing schedule was considered in order to achieve a successful completion date for fabrication and testing.

Multipliers are suitable for performing the analog signal processing since the SAS signal processing required multiplying two variables as shown by

$$Z = K \cdot X \cdot Y \quad . \quad (2.1)$$

The input variables X and Y are multiplied together and scaled by the factor K, inherent to the multiplier, to produce the output Z. One signal is a signal weight

(positive or negative) controlled by the adaptive algorithm of the DSP. The weight consists of a nine-bit binary signal. Therefore, depending on the multiplier chosen there may be a necessity for an extra D/A converter to convert the multiplier weight. In this chapter, three specific implementations will be discussed in detail.

Before deciding on a specific implementation for the multiplier, it is necessary to understand the specific types of multipliers being investigated. Limitations on the signs of the variables of the multipliers are a concern. For the specific application it is a requirement that both multiplier variables be allowed to attain a positive or negative value, i.e. a four-quadrant multiplier is required.

A one-quadrant multiplier allows for the input variables to represent positive quantities only. Two-quadrant multipliers produce a product that is a positive quantity. Neither a one or two-quadrant multiplier is acceptable for required signal processing for the smart receiver. The third possibility is a four-quadrant multiplier which allows for any sign of input or output. Figure 2.1 provides a graphical depiction of the various n-quadrant multipliers.

Many multipliers have been investigated in the past, including the classical Gilbert multiplier [12] which employs differential pairs to provide four-quadrant multiplication. Simple multipliers can be implemented using current mirrors and an additional control voltage on the source of one transistor to allow for variations in current gain. Other All-MOS implementations have also been developed [13] [14], however a wide range of gains is difficult to achieve.

The remaining sections of this chapter will focus on three methods of implementation for the analog multipliers.

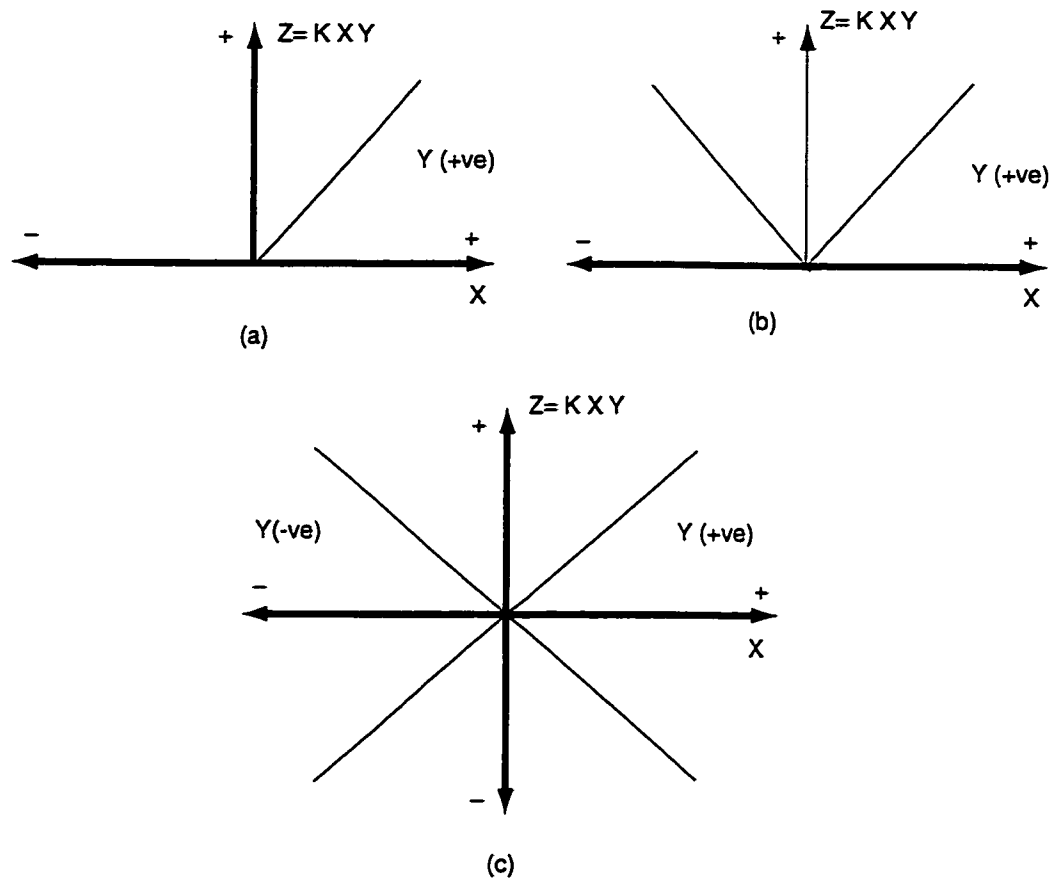


Figure 2.1: Multipliers (a) one-quadrant (b) two-quadrant (c) four-quadrant multiplier

## 2.1 Raytheon

A building block that can be used to form a four-quadrant multiplier is shown in Figure 2.2, which is a diagram for an RC4200 (Raytheon) integrated circuit [15]. A simplified expression can be found relating the currents  $I_1$ ,  $I_2$ ,  $I_3$  and  $I_4$ . While performing the analysis all transistors are assumed to have identical characteristics, and the operational amplifiers are taken as ideal. The initial analysis begins with the basic relationship, derived from the Ebers-Moll equation [16], between the base-

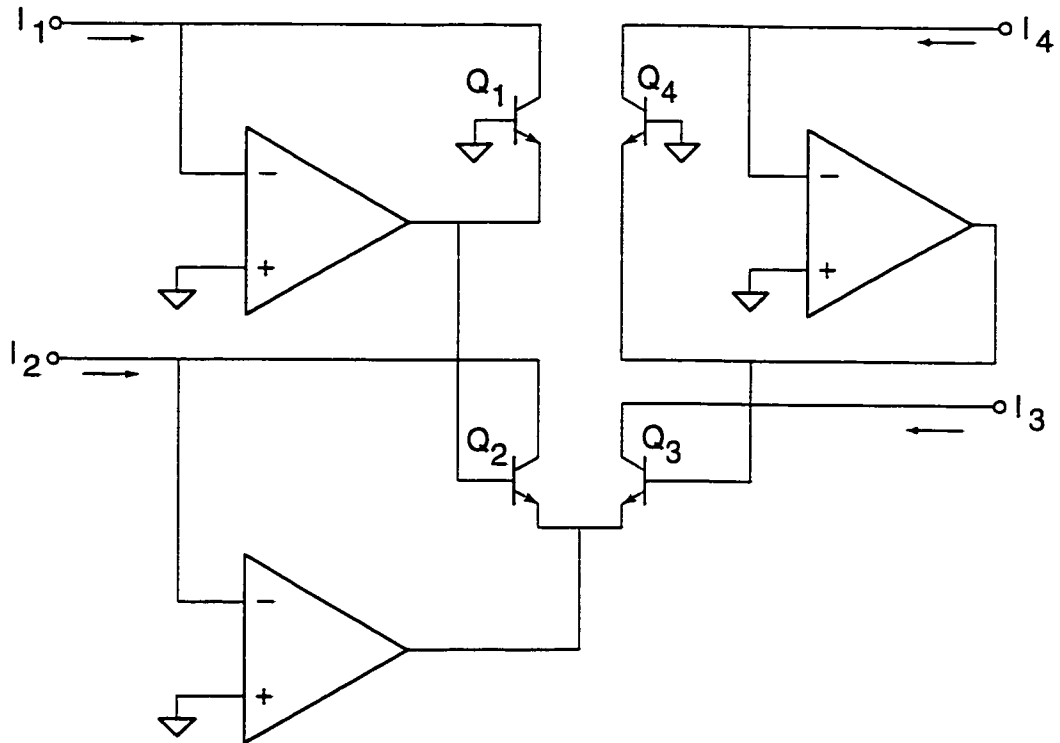


Figure 2.2: RC4200 (Raytheon)

emitter voltage  $V_{BE}$ , and the collector current  $I_C$  expressed as:

$$V_{BE} = V_t \ln \left( \frac{I_C}{I_{ES}} \right) \quad (2.2)$$

where  $V_t = kT/q$  is the thermal voltage and  $I_{ES}$  is the reverse saturation current.

Using this relationship with the assumptions that the amplifier open-loop gains are infinite and all currents are positive gives

$$V_t \ln \left( \frac{I_1}{I_S} \right) + V_t \ln \left( \frac{I_2}{I_S} \right) = V_t \ln \left( \frac{I_3}{I_S} \right) + V_t \ln \left( \frac{I_4}{I_S} \right) \quad (2.3)$$

which once simplified can be expressed as:

$$I_1 \cdot I_2 = I_3 \cdot I_4 \quad (2.4)$$

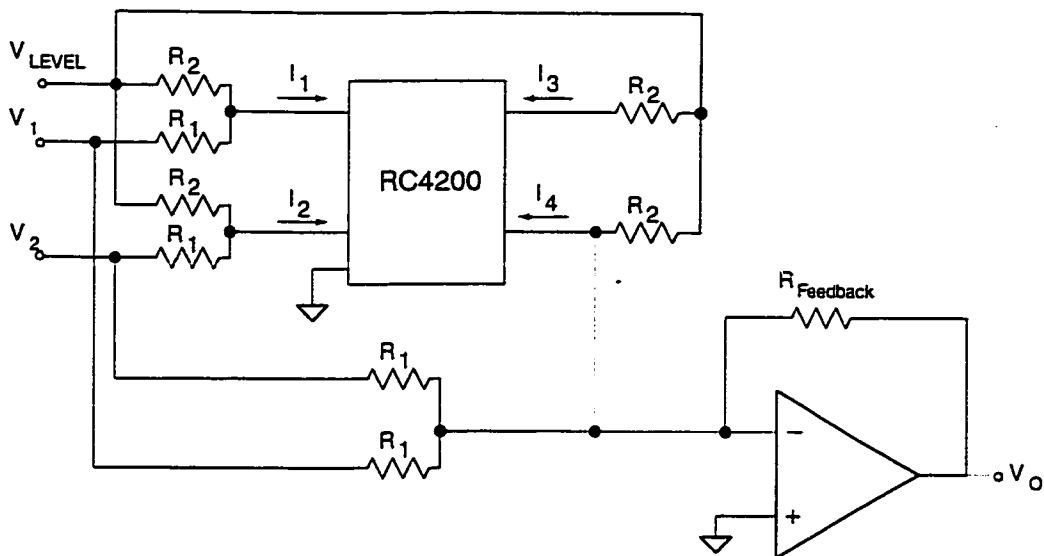


Figure 2.3: Four Quadrant Analog Multiplier.

This building block can be used to realize a multiplier as shown in Figure 2.3. Using (2.4) along with the understanding that the inputs to the Raytheon circuit are virtual grounds, a simplified expression for the output voltage is found to be

$$V_o = \frac{V_1 V_2}{V_{LEVEL}} \cdot \frac{R_2 R_{Feedback}}{R_1^2} \quad (2.5)$$

The resistor values can be used to adjust the scaling factor.  $V_{LEVEL}$ , in conjunction with the resistor values, is used to set the operating limits. In order for the circuit to function properly,

$$V_1 \geq -V_{LEVEL} \cdot \frac{R_1}{R_2} \quad (2.6)$$

and

$$V_2 \geq -V_{LEVEL} \cdot \frac{R_1}{R_2} \quad (2.7)$$

Provided these constraints are met, a four-quadrant multiplier can be designed.



## 2.2 Adjustable Current Mirror

Another circuit which allows for an adjustable gain in a current mirror is shown in Figure 2.4 [17]. Table 2.1 lists the various sizes for transistors. This current mirror is controllable over eight decades of signal current [18]. The adjustable gain of the circuit is controlled via the gate-to-source voltage of  $M_3$ . The voltage level of  $V_{GS3}$  is set by the potentiometer (R) and the gate-to-source voltages of  $M_1$  and  $M_2$ . The voltage levels  $V_{GS1}$  and  $V_{GS2}$  are set by the input current and although drain currents in  $M_1$  and  $M_2$  are equal the corresponding different  $W/L$  ratios set different gate-to-source voltages. It should be noted that the purposes of transistors  $M_4$  and  $M_5$  are to serve as buffer transistors.

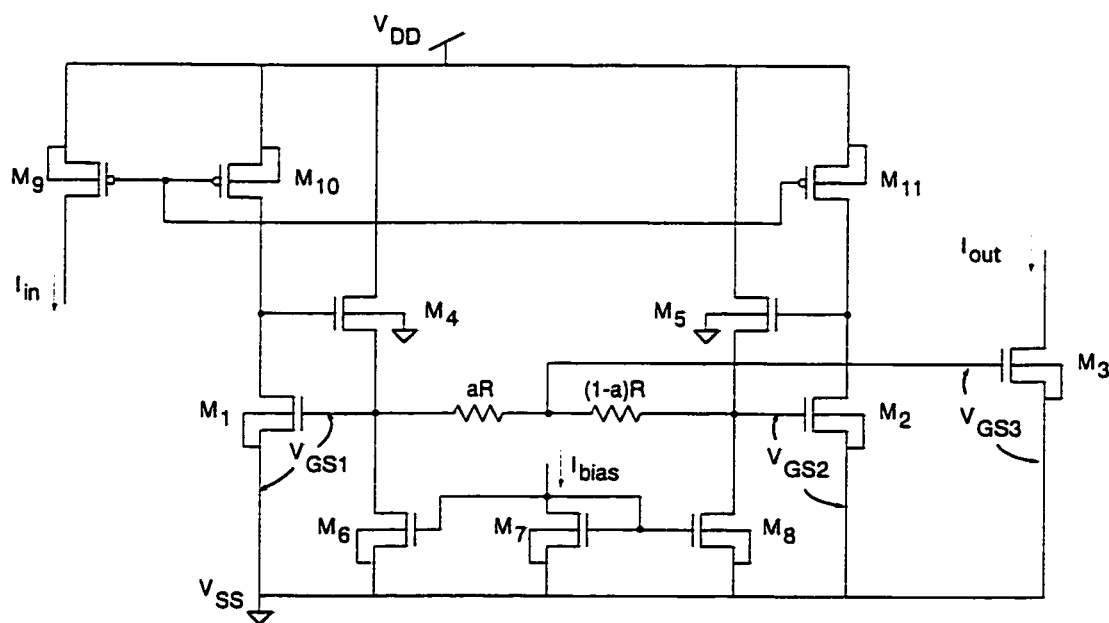


Figure 2.4: Adjustable Current Mirror.

Transistors	W/L
$M_1, M_3$	320/16
$M_2$	80/16
$M_4, M_5$	80/19.2
$M_6, M_7, M_8$	80/16
$M_9, M_{10}, M_{11}$	240/16

Table 2.1: Sizes of transistors for Adjustable Current Mirror

The regions of operation for this circuit include sub-threshold and strong inversion, which are dictated by the input and bias currents. For that reason it is possible to obtain two different equations for the current gain. However, due to the low-speed nature when operating in sub-threshold, only the specific case of strong inversion will be considered.

As previously mentioned,  $V_{GS3}$  is the controlling voltage for the output current and is determined by:

$$V_{GS3} = (1 - a) V_{GS1} + a V_{GS2} \quad . \quad (2.8)$$

In the case of strong inversion the drain currents in saturation, ignoring channel-length modulation, can be expressed as

$$I_D = I_{in} = \frac{\mu_n C_{ox} W}{2 L} (V_{GS} - V_{TO_n})^2 \quad (2.9)$$

where  $\mu_n$  is the electron mobility,  $C_{ox}$  is the oxide capacitance per unit area,  $W/L$  is channel width/length of the specific transistor and  $V_{TO_n}$  is the threshold voltage at  $V_{SB} = 0V$ . The resulting equation for  $V_{GS}$  become:

$$V_{GS} = V_{TO_n} + \sqrt{\frac{I_{in}}{\frac{\mu_n C_{ox} W}{2 L}}} \quad . \quad (2.10)$$

Using equation 2.8 along with corresponding equations for  $V_{GS1}$  and  $V_{GS2}$  the output current in strong inversion can be expressed as:

$$I_{out} = k_n \left( \frac{W}{L} \right)_3 \left( \sqrt{\frac{I_{in}}{k_n \left( \frac{W}{L} \right)_1}} + a \left( \sqrt{\frac{I_{in}}{k_n \left( \frac{W}{L} \right)_2}} - \sqrt{\frac{I_{in}}{k_n \left( \frac{W}{L} \right)_1}} \right) \right)^2 \quad (2.11)$$

where  $k_n = \frac{\mu_n C_{ox}}{2}$ .

Now, for the case where  $(W/L)_1 = (W/L)_3$  a simplified expression for  $I_{out}$  can be determined.

$$I_{out} = \left( \frac{W}{L} \right)_1 I_{in} \left( \sqrt{\frac{1}{\left( \frac{W}{L} \right)_1}} + a \left( \sqrt{\frac{1}{\left( \frac{W}{L} \right)_2}} - \sqrt{\frac{1}{\left( \frac{W}{L} \right)_1}} \right) \right)^2 \quad (2.12)$$

Equation 2.12 can be re-written as

$$\frac{I_{out}}{I_{in}} = M \left( a + \frac{1-a}{\sqrt{M}} \right)^2 \quad (2.13)$$

where  $M = (W/L)_1/(W/L)_2$ , which is the maximum achievable gain for the circuit.

Figure 2.5 shows the gain as a function of 'a' with M as a parameter.

### 2.2.1 Small Signal Analysis

The small signal equivalent circuit for the adjustable current mirror is shown in Figure 2.6. The various capacitor values in the diagram correspond to a combination of multiple parasitics which are retained to permit analysis for all regions of operation.

An elaboration for each capacitance is as follows, the notation of g, s, d and b are

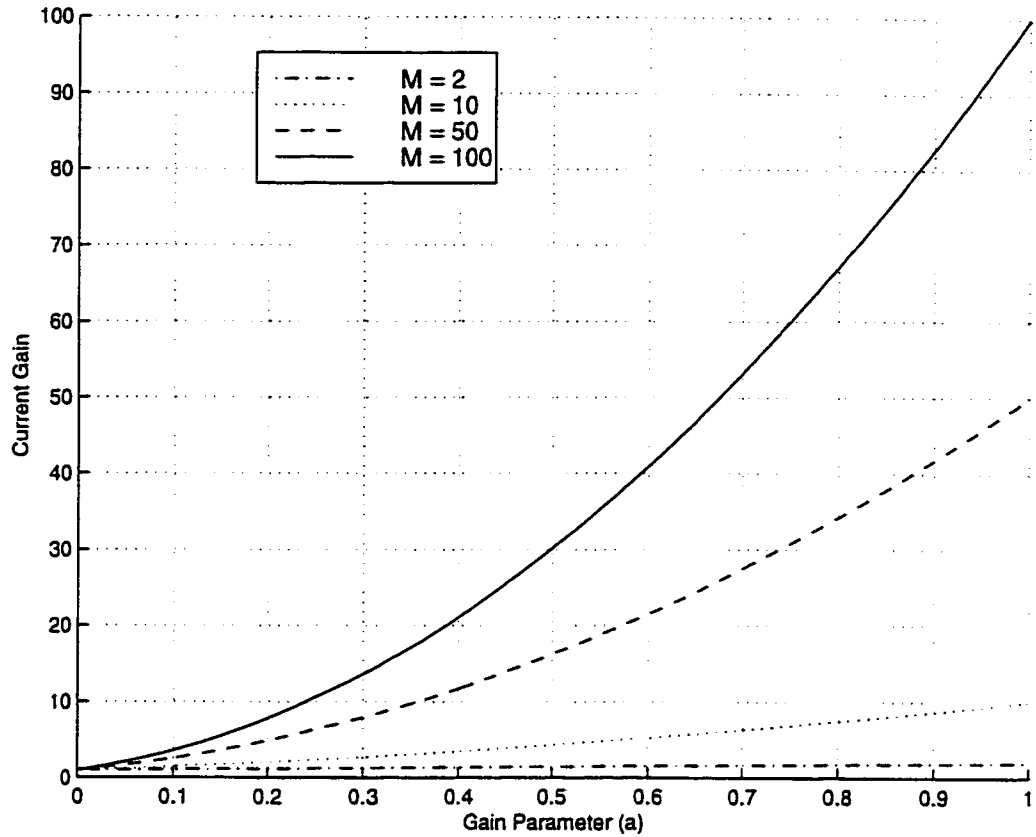


Figure 2.5: Gain of Adjustable Current Mirror in Heavy Inversion, for varying maximum achievable gain values.

used for the gate, source, drain and bulk respectively.

$$C_1 = C_{gs4} + C_{gd1}$$

$$C_2 = C_{gd4} + C_{gb4} + C_{db1}$$

$$C_3 = C_{gs1} + C_{gb1} + C_{sb4}$$

$$C_4 = C_{gs3} + C_{gb3}$$

$$C_5 = C_{gs2} + C_{gb1} + C_{sb5}$$

$$C_6 = C_{gd5} + C_{gb5} + C_{db2}$$

$$C_7 = C_{gs5} + C_{gd2}$$

A detailed analysis for the current gain can be found in Appendix A, where it is shown that

$$\frac{i_{out}}{i_{in}} = (C_{gd3} \cdot s - g_{m3}) \cdot \frac{N_3 \cdot s^3 + N_2 \cdot s^2 + N_1 \cdot s + N_0}{D_5 s^5 + D_4 \cdot s^4 + D_3 \cdot s^3 + D_2 \cdot s^2 + D_1 \cdot s + D_0} \quad (2.14)$$

where the coefficients of the equation ( N and D ) are given in detail in Appendix A. This general equation does not make any assumptions with regard to regions of operation for various transistors.

In order to validate equation 2.14 simulations were also performed with the equivalent small-signal circuit model, using values of parameters from the output file of transistor-level simulations. A comparison between the transistor-level simulated data and that of the small signal circuit, and the analytical expression is shown in Figure 2.7. The figure shows that the small signal circuit and expression are equivalent.

From equation 2.14 and using the explanation of coefficients from Appendix A, the effect of the size of the potentiometer can be seen. When calculating the coefficients for the denominator, specifically  $D_5$  and  $D_3$ , the value of the potentiometer (R) has a significant influence. This influence indicates that as R is increased the 3dB bandwidth of the circuit will decrease, due to the higher frequency coefficients having a greater effect. Figure 2.8 shows how an increasing value of the potentiometer affects the circuit.

Since the adjustable current mirror was designed and fabricated by a previous graduate student of the University, access was permitted to test the actual device. Figure 2.9 shows the effect of a larger valued potentiometer on the frequency response of the circuit.

Although the elaborate equation for frequency response is useful, it is not easily

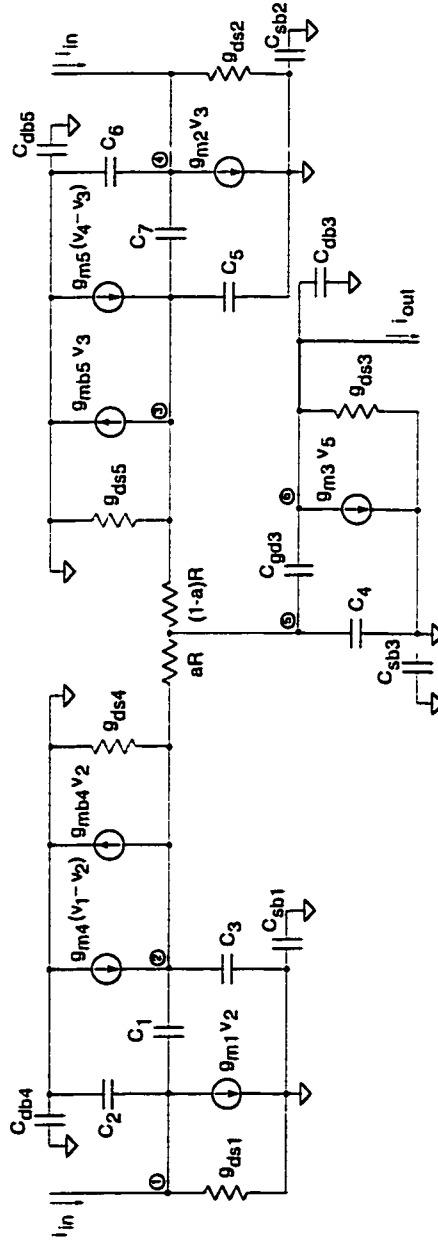


Figure 2.6: Small signal equivalent circuit of adjustable current mirror.

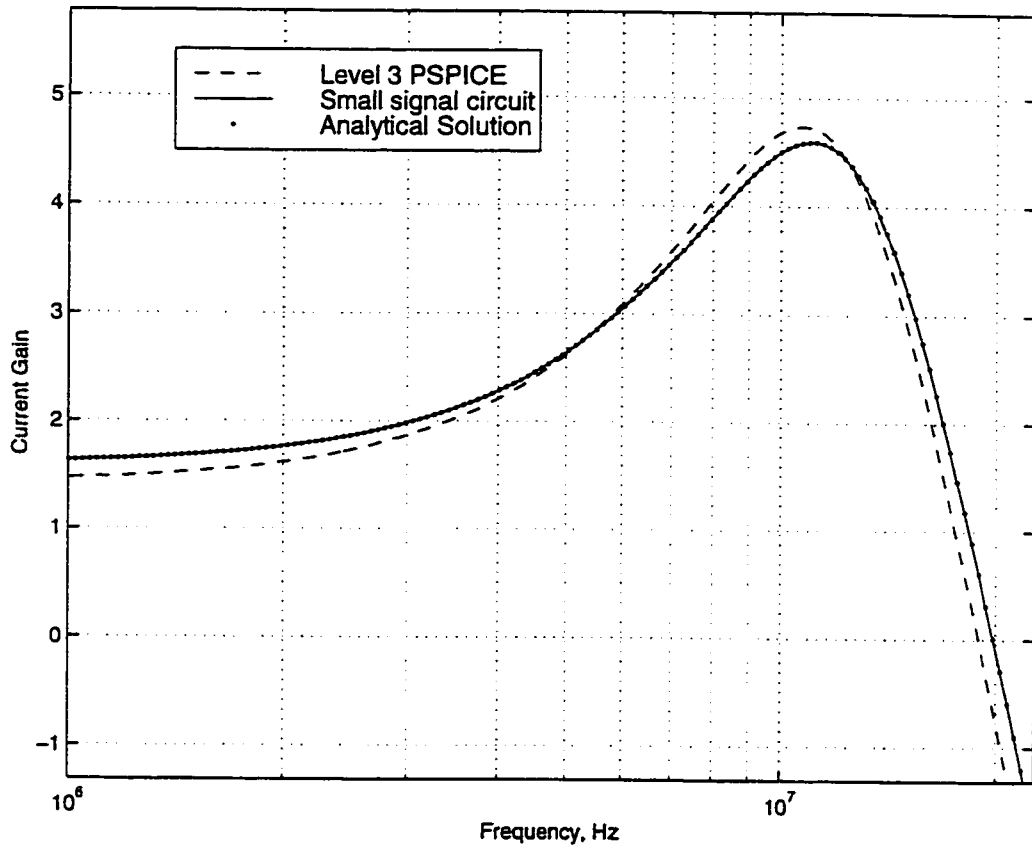


Figure 2.7: Current gain for  $a = 0.1$ ,  $R = 10 \text{ k}\Omega$ , LEVEL 3 SPICE MODEL.

usable to evaluate the 3dB bandwidth. For the case when all transistors are in heavy inversion, a simplification is possible by eliminating certain capacitances. In heavy inversion, with transistors in saturation the dominant capacitances will be the values of  $C_{GS}$ , thus values for  $C_{GD}$  and  $C_{GB}$  can be neglected [19]. With this simplification values of  $C_2$ ,  $C_6$  and  $C_{gd3}$  can be eliminated. However, even with this simplification it would be required to have some form of program to evaluate the 3dB frequency. The key point to be noted here is that a small size potentiometer is required. Also, in order to increase the 3dB bandwidth to a suitable level for the required application,

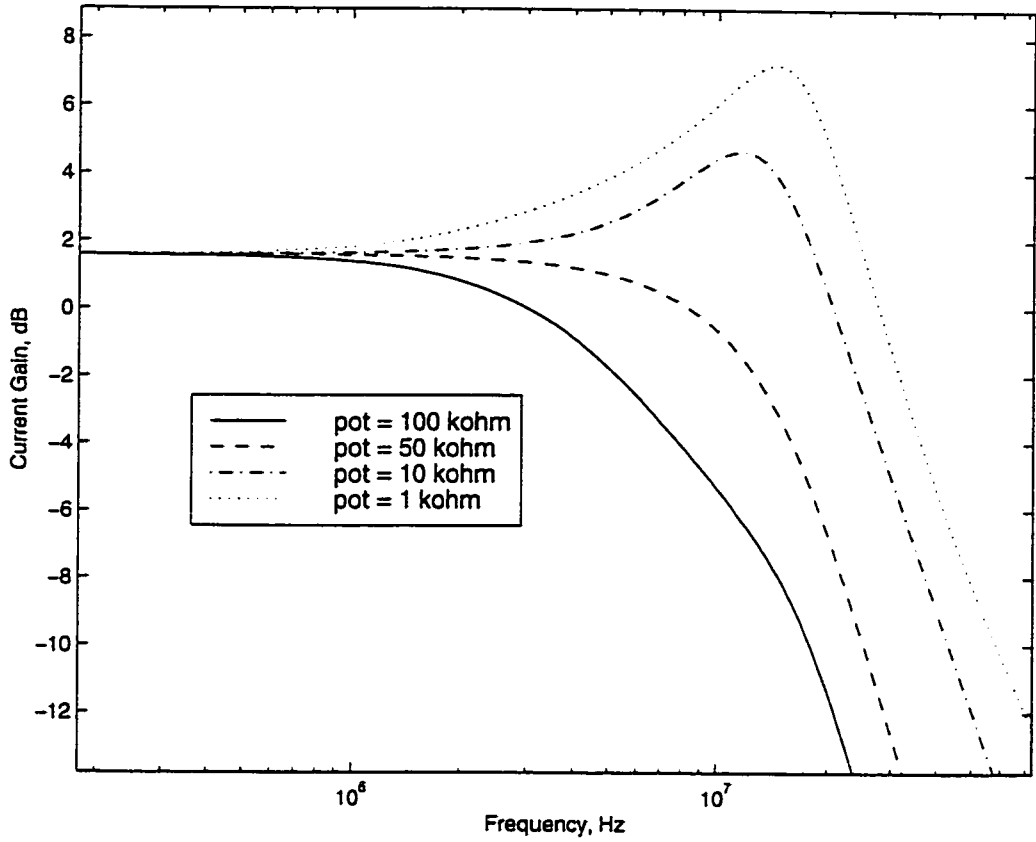


Figure 2.8: Frequency effect of various potentiometer sizes.

a larger DC input bias current level is required as indicated from Figure 2.9.



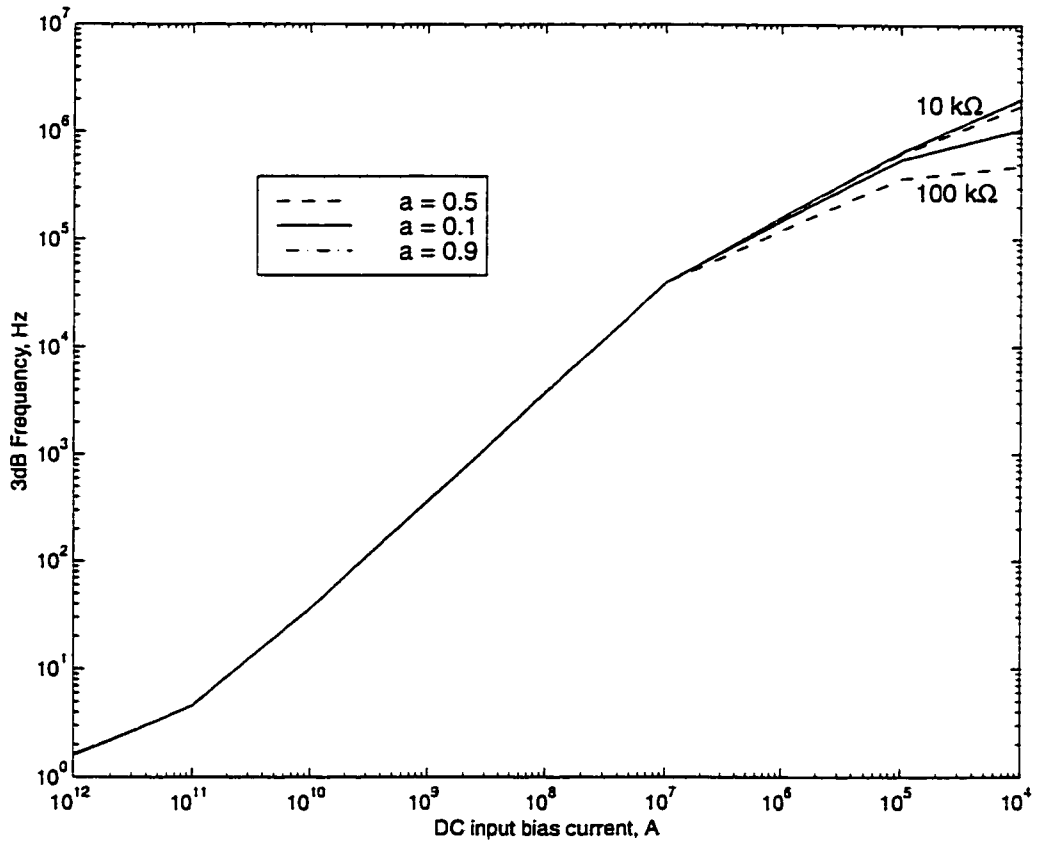


Figure 2.9: Bandwidth of Adjustable Current Mirror over a range of DC bias currents, using a potentiometer for gain control.

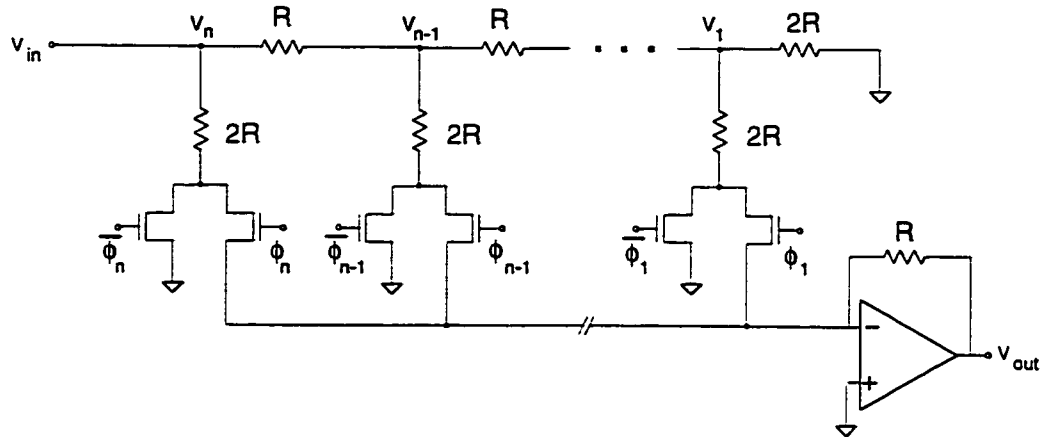


Figure 2.10: R-2R Ladder.

## 2.3 R-2R Ladders

A simple multiplier that involves a resistor network, called an R-2R ladder [12, 20], is shown in Figure 2.10. The network, with the aid of an amplifier can be used to multiply an analog signal with a given weight. The value by which the analog input is multiplied is controlled by a digital bit-stream. The number of bits is equal to the number of  $2R$  resistor branches being controlled by two analog switches, as shown. In each of these branches only one of the two analog switches will be conducting at a given time. Thus, the signal passing through each branch will either be connected to an analog ground or to the virtual ground of the amplifier. So by virtue of the switch positions, a weighted version of the analog signal will appear at the output of the amplifier.

When calculating the output voltage ( $V_{out}$ ) in terms of the input voltage ( $V_{in}$ )

it is important to note the overall structure of the ladder. The node voltages at the terminals of the  $2R$  resistors,  $v_n$  through  $v_1$  in Figure 2.10, can be calculated using a simple voltage divider. These voltages can be summed into the amplifier via the  $2R$  resistors by shorted switches. Since the  $2R$  branches in the ladder are either connected to the virtual ground of the amplifier or analog ground the node voltages equate to the following:

$$v_1 = \frac{1}{2}v_2, v_2 = \frac{1}{2}v_3, \dots, v_{n-1} = \frac{1}{2}v_n, v_n = v_{in} \quad (2.15)$$

where  $n$  represents the number of  $2R$  branches with switches (number of bits required). For completeness 2.15 should be expressed in terms of  $v_{in}$ .

$$v_1 = \frac{1}{2^n}v_{in}, v_2 = \frac{1}{2^{n-1}}v_{in}, \dots, v_{n-1} = \frac{1}{2}v_{in}, v_n = v_{in} \quad (2.16)$$

The on or off state of the analog switches will also be required to produce a general expression of  $V_{out}$ . Using the node voltages from 2.16 a final expression results as follows:

$$v_{out} = - \left[ \frac{1}{2}v_{in}\phi_n + \frac{1}{2 \cdot 2}v_{in}\phi_{n-1} + \dots + \frac{1}{2^{n-1}}v_{in}\phi_2 + \frac{1}{2^n}v_{in}\phi_1 \right] \quad (2.17)$$

where the values of  $\phi_n$  through  $\phi_1$  represent the state of each corresponding analog switch. The bits are labeled as indicated with  $n$  being the most-significant-bit (MSB) and 1 being the least-significant-bit (LSB). A value of one indicates that the appropriate switch is connecting the  $2R$  resistor to the amplifier, and a value of zero to analog ground. The negative sign is due to the inverting amplifier configuration.

A plot of the range of multiplier weights can be seen in Figure 2.11, for a circuit having 8-bits of precision.

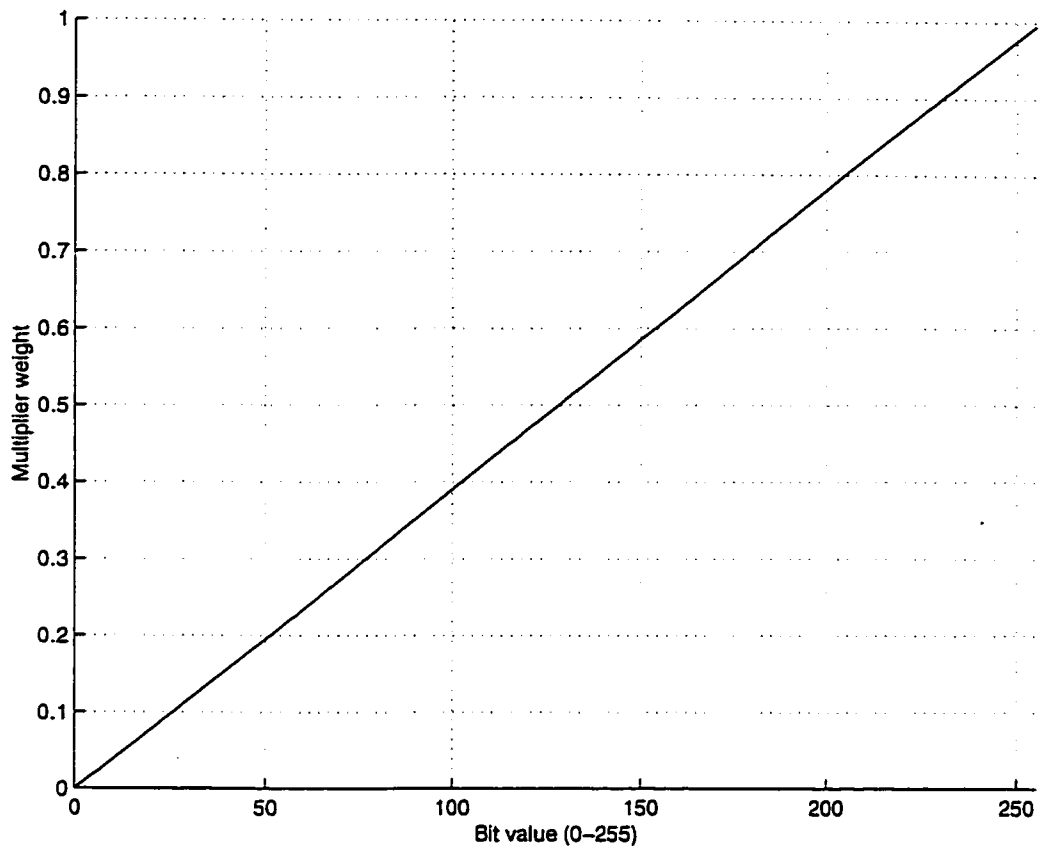


Figure 2.11: Multiplier weights for eight-bits of precision.

The plot indicates that the response of the R-2R ladder is indeed linear, as required. The number of distinct levels of multiplication in the ladder will be  $2^n$ , ranging from 0 to  $(1 - \frac{1}{2^n})$ . Therefore depending on the accuracy required for the multiplier, an appropriate number of bits will need to be chosen. For the required application, the number of bits used to control the weight is 8. A ladder with 8 bits will therefore allow for a precision of  $\frac{1}{256}$  between each voltage level.

As can be understood from equation 2.15 the varying values of the weights can only attain negative values. Due to this the circuit does not initially act as a four-quadrant multiplier. However, with additional circuitry it is possible to expand its

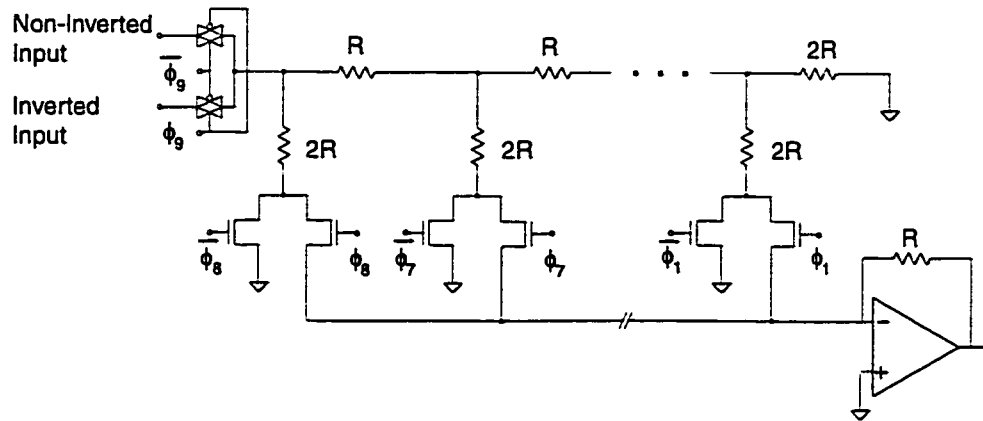


Figure 2.12: Four Quadrant R-2R Ladder.

operation to four-quadrant operation. This can be easily done by inverting the input signal, which will result in the same effect as having both  $\pm$  multiplier weights. In order to select which analog signal will be used as input, additional switches (transmission gates) will be required. Figure 2.12 shows a complete ladder configuration implementing both the four-quadrant multiplier and the number of bits required for the current system. If a larger number of bits is required at a later date, for precision purposes, the number of branches in the ladder need only be increased. For the purposes of the desired system the number of bits required is eight and all the necessary components are shown in the diagram.

### 2.3.1 Resistors

For layout and precision purposes, the particular method of implementation for the resistors must be investigated. Although the chip area that is required to lay out the resistors is a constraint, variation in the resistor values must be minimized in order to increase the level of precision. Therefore good matching is required. The two main methods that were investigated were poly-resistors and diffusion resistors, although some comparison in parameters will be given for well-type resistors. Figure 2.13 shows the different structures for poly and diffused resistors. It should be noted that for the diagrams shown, an n-well process (p-substrate) has been assumed.

The dimensions of the resistor body are outlined in Figure 2.14. Firstly, a general expression for the calculated resistance value ( $R_o$ ) for the drawn resistor is given by:

$$R_o = R_s \cdot \frac{L_{eff}}{W_{eff}} \quad (2.18)$$

where  $R_s$  is the sheet resistance per square, and the effective length and width are  $L_{eff}$  and  $W_{eff}$ , respectively. This expression can be used to calculate the total resistance for each proposed method. For the various methods of implementation values of sheet resistance can vary from process to process. Generally however it can be said that well resistors have a sheet resistance in the range of kohms/square, while poly and diffused components have sheet resistances of 50-80 ohms/square and 100-150 ohms/square, respectively.

As well, an expression indicating the temperature dependence of the resistors is given in the following equation:

$$R_{total} = R_o (1 + T_{C1} \cdot \Delta T + T_{C2} \cdot (\Delta T)^2) \quad (2.19)$$

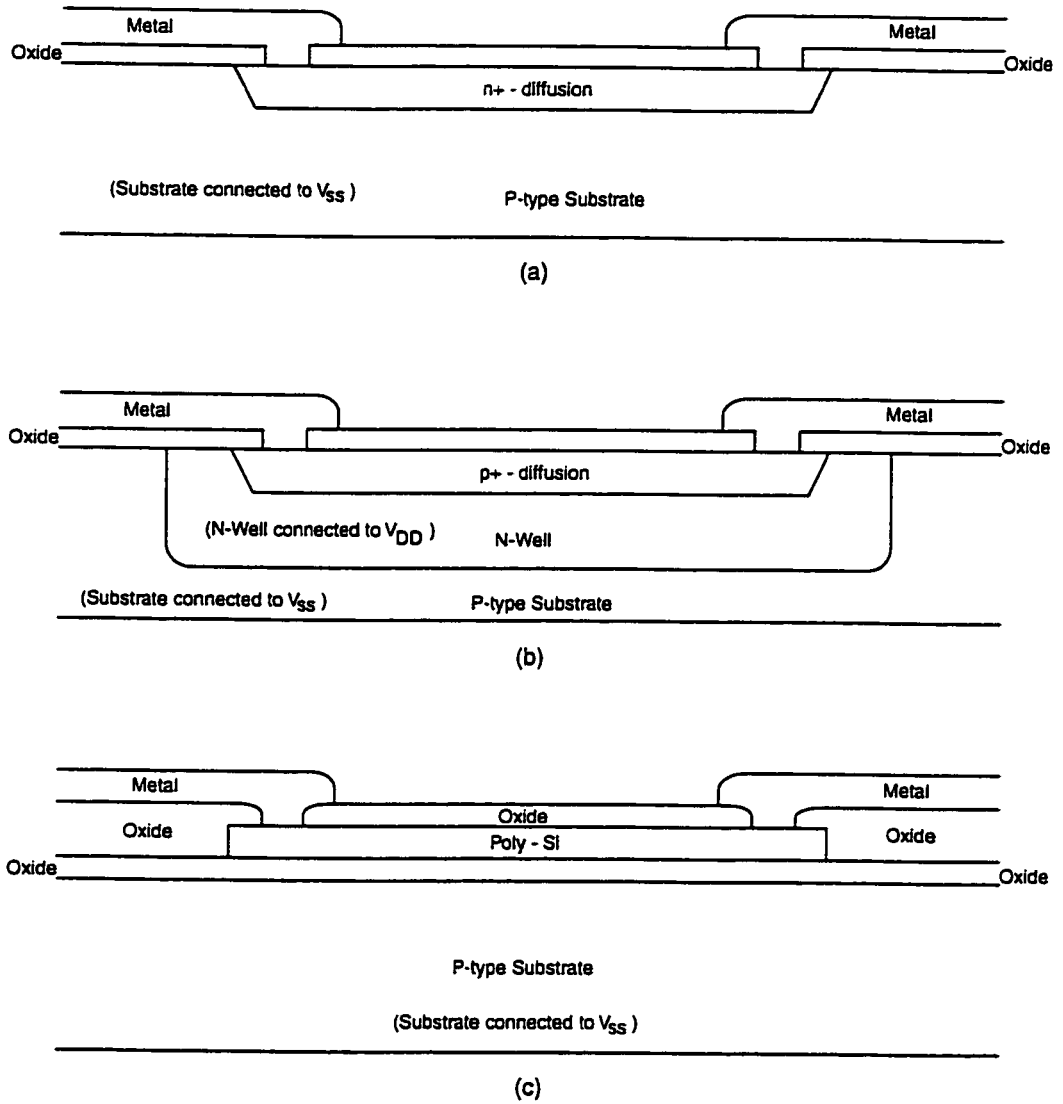


Figure 2.13: Various types of resistors (a) n+ diffusion (b) p+ diffusion (c) poly-resistor.

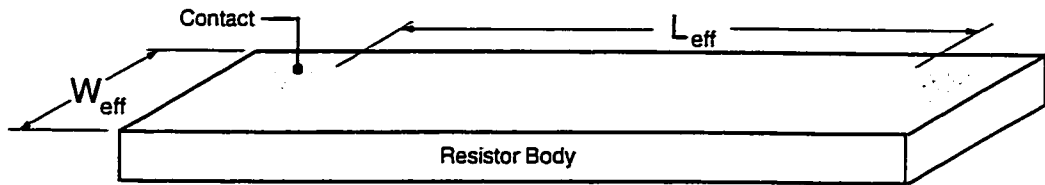


Figure 2.14: Effective dimensions of resistors.

where  $R_{total}$  is the total resistor value,  $\Delta T$  is the deviation from the nominal operating temperature, and  $T_{C1}$  and  $T_{C2}$  are the temperature coefficients for the particular type of resistor. The temperature coefficients are process dependent and equation 2.19 can be expanded to a higher order equation if parameters are available. A typical comparison of temperature effects on various resistors for a CMOS process is shown in Figure 2.15. The process shown is a dual-poly/n-well technology.

Voltage dependence of various types of components is also a concern. For the different fabrication processes available at the University, general voltage coefficient data is not available from supplied specifications. However the discussion would not be complete without mention of this aspect. The specific coefficients for well-type resistors are significantly greater than those of diffused and poly resistors. In order to give a comparison, an approximation from [19] can be shown in order to indicate the inadequacies of the well-type components.

$$\text{poly} (\approx 100 \text{ ppm/V}) < \text{diffused} (\approx 200 \text{ ppm/V}) < \text{well} (\approx 10,000 \text{ ppm/V})$$

When selecting the type of resistor to use in the layout, accuracy is an obvious concern. Accuracy is measured in two ways, absolute and relative. Absolute accuracy is the percent deviation of the sheet resistance for a given fabrication. This



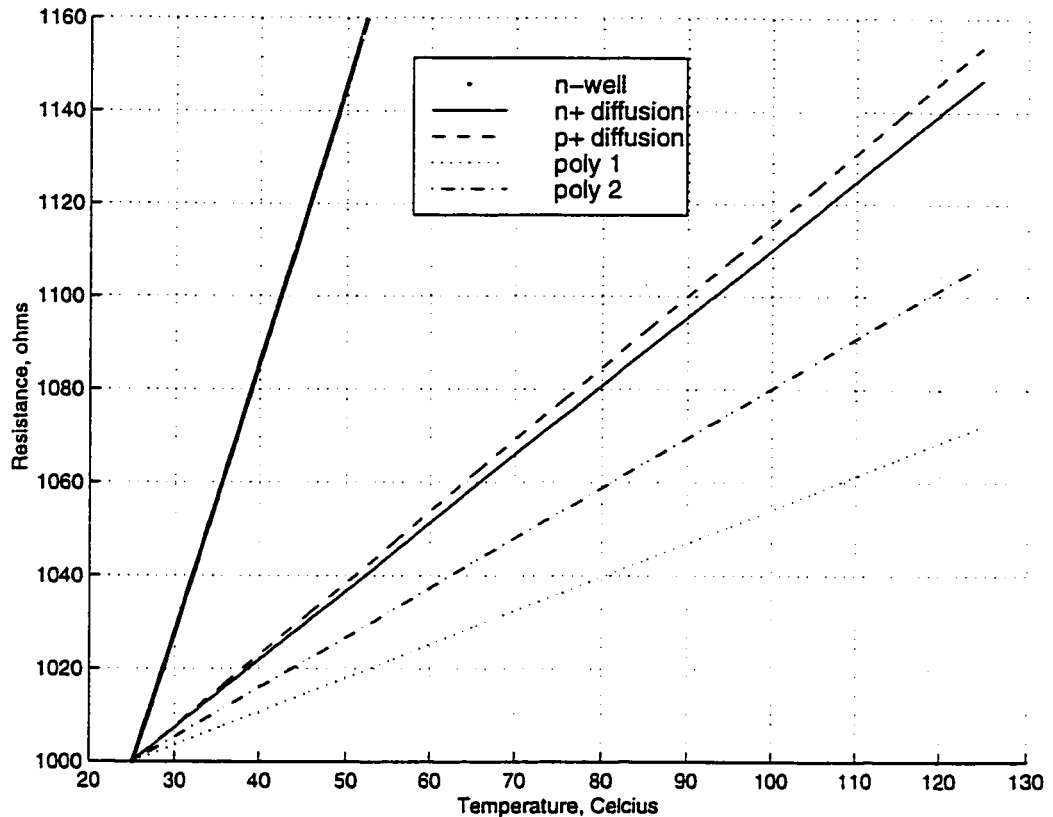


Figure 2.15: Temperature variation for a  $1\text{ k}\Omega$  resistor, nominal temperature  $25^\circ\text{ C}$ .

includes wafer to wafer deviation, and also the deviation within a single wafer. Relative accuracy (ratio tolerance) is the deviation that can occur between two identical components. The absolute accuracy can range wildly for different fabrication processes, due to doping levels required. In order to minimize the error due to both deviations, it is necessary to have individual components that require better matching in close proximity. Some typical values for different type of resistors for a CMOS process are:

Absolute: diffused ( $\pm 30\%$ ) < poly ( $\pm 40\%$ ) < well ( $\pm 45\%$ )

Relative: diffused and poly ( $\approx 1$  to  $2\%$ ), well ( $\approx 5\%$ )

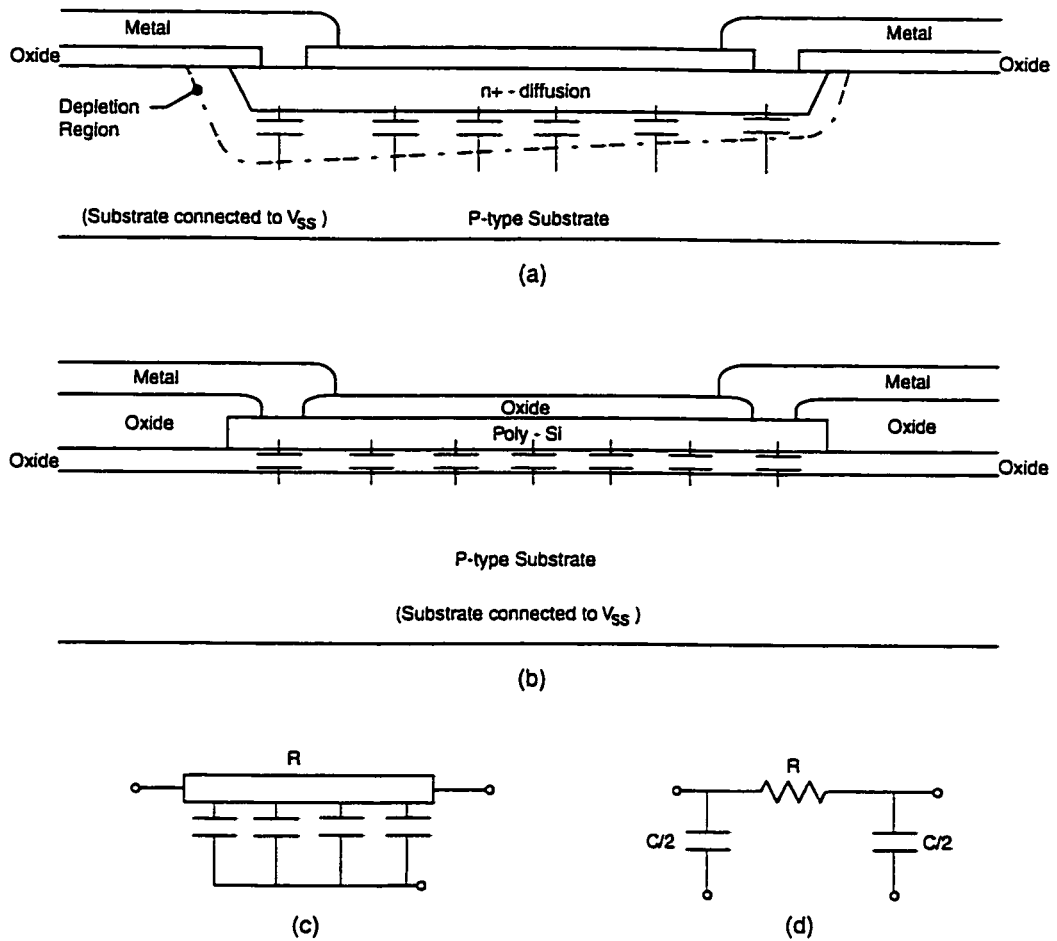


Figure 2.16: Parasitic capacitance (a) n+ diffusion (b) poly (c) general resistor model (d) T-terminal equivalent circuit.

Frequency response of the resistors is also important. Therefore, the parasitic capacitances involved are inspected. Figure 2.16 show the capacitances associated with poly and diffusion resistors. Along the body of the resistors are parasitics, which can be lumped together in an equivalent circuit as shown in Figure 2.16(d).

In the case of the poly-resistor the distributed capacitance along the body is equivalent to a single lumped capacitance. Although the capacitance per unit area

can be calculated from permittivity and thickness of the oxide layer, typically this value will be provided from fabrication specifications.

The parasitics associated with diffused resistors are voltage dependent. The reverse-bias p-n junction forming the body of the device and the resulting depletion region form the parasitics. However, since there is a varying voltage across the body of the device the associated capacitance will also vary. The general equation used to calculate the capacitance per unit area ( $C_j$ ) for an abrupt p-n junction can be described as [16, 21]:

$$C_j = \frac{C_{j0}}{\sqrt{\frac{V_R}{\phi_0} + 1}} \quad (2.20)$$

where  $C_{j0}$  is the junction capacitance per unit area at zero bias,  $V_R$  is the reverse-bias voltage on the junction, and  $\phi_0$  is the built-in potential of the junction.

Typically the specifications will provide values for  $C_{j0}$  only, making it difficult to obtain a precise value for a lumped-sum value of parasitics. However, simple calculations can be completed using  $C_{j0}$ , since it will provide a worst-case situation for the device.

All of the above discussions provide information that must be considered when making a final decision in the specific choice of device. However, between the two device types of poly and diffused resistors the dominating factors will be chip area and parasitics. The matching properties of each type are similar and low, as required by the specific application.

### 2.3.2 Analog Switches

Now that the overall structures of the R-2R ladder and resistors have been presented, the switching elements in the circuit will be discussed. The input levels for the smart receiver have been specified to be  $\pm 1$  V. Due to this requirement the substrate must have a voltage level that will prevent substrate diode forward bias in any switches used.

For any given fabrication process it would be unwise, for the current application, to set values of  $V_{DD}$  and  $V_{SS}$  to maximum-supply and zero volts, respectively. The control levels for the switches, for a state of on or off, would be chosen likewise. Thus, with an input of -1V individual switches may be able to have an on-state when the opposite is desired. In order to eliminate this problem from any of the chosen implementations of switches, dual supplies of plus/minus one-half the maximum supply can be used.

There are two specific types of switches that will be discussed, a single-transistor switch and a transmission gate. Each type of analog switch can be used for two different purposes in the R-2R ladder. As will be shown the transmission gate would be appropriate for the switches at the input of the ladder. The single transistor switches are applicable for the resistor branches. The single transistor switches in this case will be grounded switches, either to the system's analog ground or the virtual ground of the amplifiers. In the next two subsections the specific analog switches will be discussed.

### 2.3.2.1 Single Transistor Grounded Switches

An NMOS single transistor switch has already been shown in Figure 2.10. In order to use the switch properly it is necessary to minimize the on-resistance ( $R_{on}$ ), in order not to effect the overall circuit. The switches will be ideally required to short-circuit the resistor branches to either the analog or virtual ground. When the switch is on it will be operating in the triode region and the drain current can be expressed as:

$$I_{Dn} = \frac{\mu_n C_{ox} W}{L} \left( (V_{GS} - V_{Tn}) V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (2.21)$$

where  $\mu_n$  is the electron mobility,  $C_{ox}$  is the oxide capacitance per unit area,  $W/L$  is channel width/length of the specific transistor,  $V_{GS}$  is the gate-to-source voltage,  $V_{DS}$  is the drain-to-source voltage, and  $V_{Tn}$  is the threshold voltage. For the purposes of this discussion channel length modulation effects will be neglected ( ie.  $[1 + \lambda V_{DS}] = 1$ , thus  $\lambda = 0$  which is the channel length modulation factor ) [22].

The large-signal value of the transistor  $(R_{on})_n$  is found from

$$(R_{on})_n = \frac{1}{\frac{\Delta I_D}{\Delta V_{DS}}} = \frac{1}{\frac{dI_D}{dV_{DS}}} \quad (2.22)$$

so that from (2.21)

$$(R_{on})_n = \frac{1}{\frac{\mu_n C_{ox} W}{L} ((V_{GS} - V_{Tn}) - V_{DS})} \quad (2.23)$$

Since ideally the value of  $V_{DS} \approx 0$ , the value for the on-resistance can be simplified to

$$(R_{on})_n = \frac{L}{\mu_n C_{ox} W (V_{GS} - V_{Tn})} = \frac{L}{\mu_n C_{ox} W (V_G - V_{Tn})} \quad (2.24)$$

Mathematically it can be readily seen that as  $V_{GS} - V_{Tn}$  approaches zero the on-resistance becomes infinite. Physically this means that as the transistor cuts off

the channel-resistance becomes large. Thus, values of  $V_{GS} > V_{Tn}$  that ensure the transistor is completely on are required to maintain a low resistance.

An added complication arises caused by the threshold voltage. Due to the body effect the threshold voltage will depend on the source voltage [22]

$$V_{Tn} = V_{TO_n} + \gamma \left( \sqrt{2\phi_p + |V_{SB}|} - \sqrt{2\phi_p} \right) \quad (2.25)$$

where  $V_{TO_n}$  is the threshold voltage with  $V_{SB} = 0$ ,  $\gamma$  is the body-effect coefficient,  $\phi_p$  is the bulk potential and  $V_{SB}$  is the source-to-bulk voltage. For the given grounded switch, the value of  $V_{SB}$  will be a constant value. Therefore, although there will be threshold modulation, the value will remain constant for a given value of  $V_G$ . The value of the switch on-resistances will also be constant and can be found from the combination of equations 2.24 and 2.25.

The on resistance for the given grounded switches will be dictated by the W/L ratio of the transistors. The larger the ratio the smaller the value of  $(R_{on})_n$ , which is desired. However, a trade-off exists since large W/L will increase gate capacitance and slow the circuit down.

### 2.3.2.2 Transmission Gate

With the requirement of a four-quadrant multiplier, additional switches are needed at the input of the R-2R Ladder. However, in comparison to the single transistor switches used, the input will not have the benefit of having the source tied to ground. The on-resistance will therefore be dependent on the input voltage  $V_{in}$ . Equation 2.24 can be modified for this dependence as follows:

$$(R_{on})_n = \frac{L}{\mu_n C_{ox} W (V_G - V_{in} - V_{Tn})} \quad (2.26)$$

So as the value of  $V_{in}$  ranges in values from  $-1V$  to  $+1V$ , the on-resistance will increase, given that  $V_G$  is constant. For a single PMOS transistor the characteristic curve for the on-resistance will decrease as  $V_{in}$  changes from a negative to a positive quantity. For a PMOS transistor the on-resistance can be expressed as:

$$(R_{on})_p = \frac{L}{\mu_p C_{ox} W (|\bar{V}_G| + V_{in} - |V_{Tp}|)} \quad (2.27)$$

where  $\mu_p$  is the hole mobility and  $\bar{V}_G$  is the dc-level to turn a PMOS device on. For completeness the corresponding equation for  $V_{Tp}$  is [22]:

$$V_{Tp} = V_{TOp} - \gamma \left( \sqrt{2\phi_p + |V_{SB}|} - \sqrt{2\phi_p} \right) \quad (2.28)$$

In comparison with the single grounded transistor, the threshold modulation due to the body-effect will have a greater effect in the on-resistance. The value of  $V_{SB}$  will now change with  $V_{in}$  and result in the corresponding change to equations 2.25 and 2.28.

Due to the varying value of the on-resistance, a single transistor switch will not be suitable for the input switches. A parallel combination of n-type and p-type transistors, forming a transmission gate, is appropriate. This will allow for a low on-resistance for the valid range of  $V_{in}$ , which can be calculated from:

$$(R_{on})_{total} = \frac{1}{\mu_n C_{ox} \frac{W_n}{L_n} (V_G - V_{in} - V_{Tn}) + \mu_p C_{ox} \frac{W_p}{L_p} (|\bar{V}_G| + V_{in} - |V_{Tp}|)} \quad (2.29)$$

where the subscripts of n and p have been included on W and L to differentiate between NMOS and PMOS transistor sizes. It should be noted that  $V_G$  and  $\bar{V}_G$  are set to the opposing rails  $V_{DD}$  and  $V_{SS}$ , respectively. This will ensure that both transistors are fully on at the same time.

Therefore the benefit of having the parallel combination of both NMOS and PMOS transistors is that it provides lower on-resistance over the full range of  $V_{in}$ .

Care must be taken when choosing sizes for each transistor type. In order to maintain a more uniform on-resistance value across all ranges of input, the appropriate ratios of  $W/L$  must be chosen. This will be further discussed on during the implementation stage of the design.



## Chapter 3

# Implementation

Several building blocks for the implementation of the analog multiplier chip are discussed in Chapter 3. A final selection for the multiplier cell must be made to ensure that the criteria for a successful design can be met. The most suitable solution appears to be the R-2R Ladder, due to its excellent linearity and repeatability. Other methods, such as the adjustable current mirror, will have difficulty achieving a large range of gain-values without having increased chip area. The potentiometer would also require an implementation in order to attain varying values of gain.

In order to achieve a successful implementation a suitable fabrication process must be chosen. Comparing the different fabrication processes available, the two most likely candidates were the Mitel 1.5  $\mu\text{m}$  CMOS and TSMC 0.35  $\mu\text{m}$  CMOS processes. Due to the large number of resistors that were required, it was mandatory to choose a process that had reasonably large values for sheet resistances, in order to minimize chip area. Each of the two technologies has comparable values for the sheet resistances of each type of resistor. However the TSMC technology has slightly larger values for the various types of resistors. Also, due to the smaller minimum

geometry sizes for the TSMC technology, it was more suitable for the digital control circuitry for the ladder. For these reasons, along with a suitable submission deadline, the TSMC 0.35  $\mu\text{m}$  CMOS process was chosen for the implementation. With this selection it should also be noted that it is a 3.3 V technology.

A confidentiality agreement was required in order to gain access to this technology. In order to comply with these agreements, there will be no specific details given with respect to any parametric information. The space that was requested and granted by CMC was  $3300 \times 3300 \mu\text{m}$ . The overall layout and implementation can be seen in Figure 3.1. For the implementation of the multiplier chip 96 R-2R Ladders are required. This number is required due to the necessity of 6 receiving elements and 4 transmitted signals ( $(4 \times 2) \times (6 \times 2) = 96$ ) as described in Chapter 1. Therefore, this equates to a total of 1,536 resistors, 1,536 single transistor switches and 192 transmission gates required to implement the multipliers.

The overall pad structure for the IC is shown in Figure 3.2. The larger analog pads are drawn to illustrate where the larger current flow will occur in the circuit. Included in the layout, Figure 3.1, are the 96 analog multipliers, along with the additional digital control circuitry for the weights of the multipliers. The system for which this IC was designed allows for four transmitters and six receiving elements. The multipliers are arranged such that each row of multipliers is summed to an external pad which can be connected to an amplifier. Each of these pads results in an output for either an I or Q signal for one of the transmitted signals. This accounts for a total of eight pads for the four pairs of transmitted I/Q signals.

The total number of inputs required for the R-2R Ladder is doubled due to the four-quadrant multiplication requirement. In total this equates to 24 signal inputs

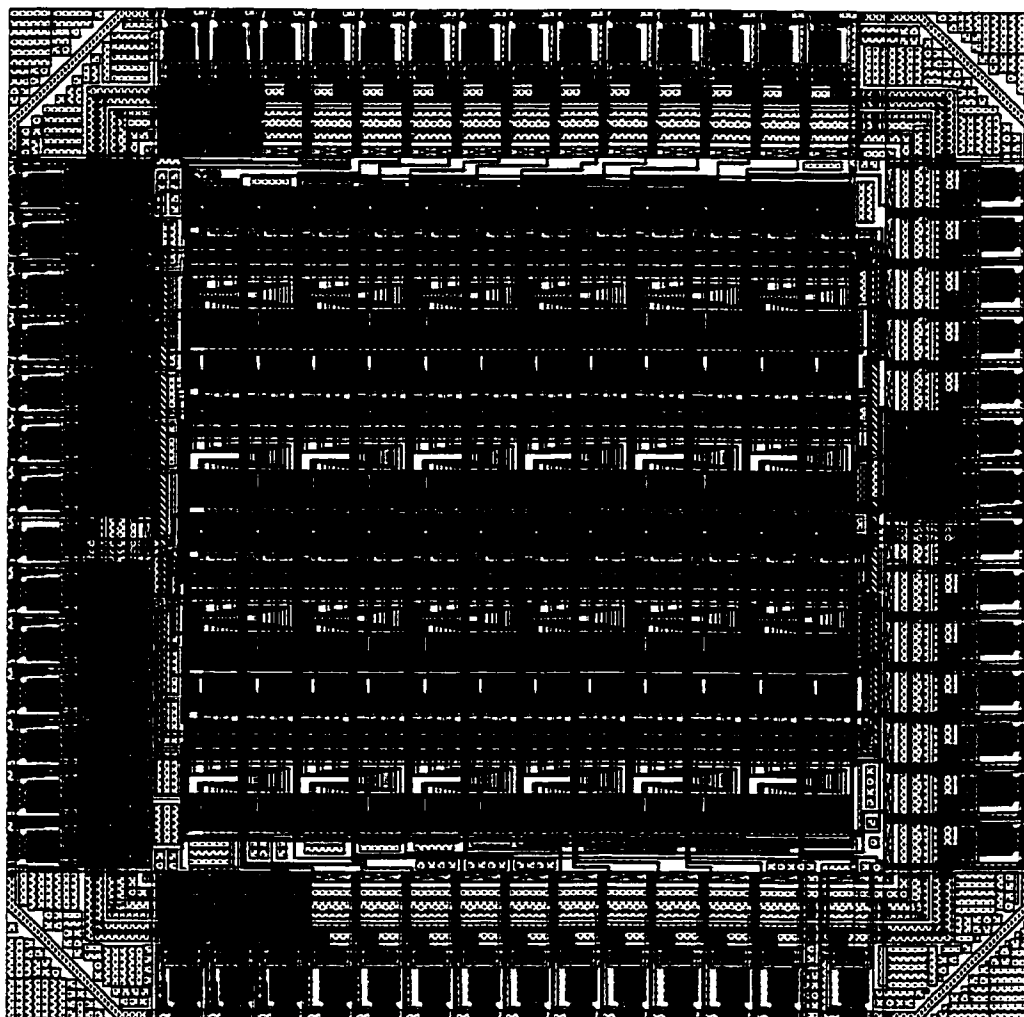


Figure 3.1: Multiplier Chip Implementation, ICDCYSA1,  $3300 \mu\text{m} \times 3300 \mu\text{m}$ .

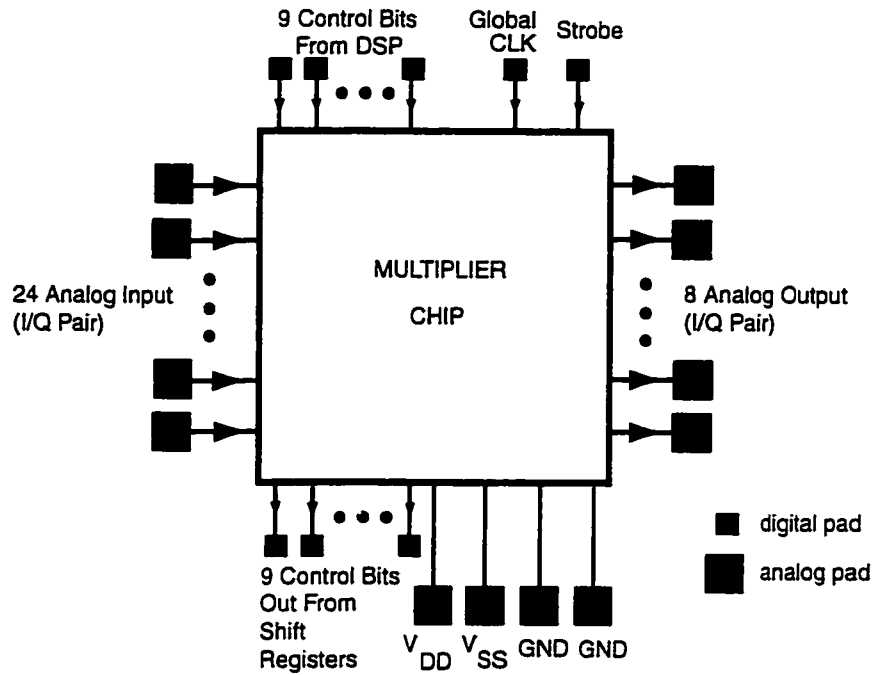


Figure 3.2: Pad usage for multiplier chip, ICDCYSA1.

for the six receiving elements, thus 24 pads. The number of bits that the multipliers require are nine, eight for the actual weight and one for the sign. The digital control for the multipliers was performed by the use of shift registers which also require additional signals to clock in the weights as they are fed from the DSP. A strobe signal was also needed to load the weights to the multipliers themselves.

Since the maximum number of transmitted/received signals could be doubled in order to attain the maximum capacity for the system, modularity in the design was also required. This was achieved by simply allowing the final stage of the shift registers to be brought out to additional pads. This allows for multiple IC's to be stacked by simply connecting the output bit stream from one chip to the input stream of the next chip. However, in order to increase the capacity of the system to its maximum,

<i>Signal</i>	<i>No. of Pads</i>
Inverting Input	12
Non-Inverting Input	12
Output to Summers	8
Digital Input	9
Digital Output	9
Clock	1
Strobe	1
Analog Ground	2
$V_{DD}, +1.6 V$	1
$V_{SS}, -1.6 V$	1
Total	56

Table 3.1: Pads required for ICDCYSA1.

four individual chips are required in order to increase the number of multipliers to 384. The stacking of chips to work in tandem however, will result in an error that will be determined by the absolute accuracy of the fabrication run. Therefore an overall accuracy of 1 % can not be guaranteed.

To allow for modularity the implementation as shown in Figure 3.1 required the breakdown of pads listed in Table 3.1. Due to the space that was granted the layout was pad-limited. Typically two additional pads would provide separate analog and digital dual-sources ( $V_{DD}$  and  $V_{SS}$ ).

### 3.1 R-2R Ladder Implementation

Due to the large number of components required for the analog building blocks, the resistors chosen were p+ diffusion resistors. Although diffusion resistors are more temperature dependent than the poly-resistors, the diffusion layer was chosen for the higher sheet resistance ( $R_{diffusion} \approx 3 \times R_{poly}$ ). In particular, p+ diffusion was

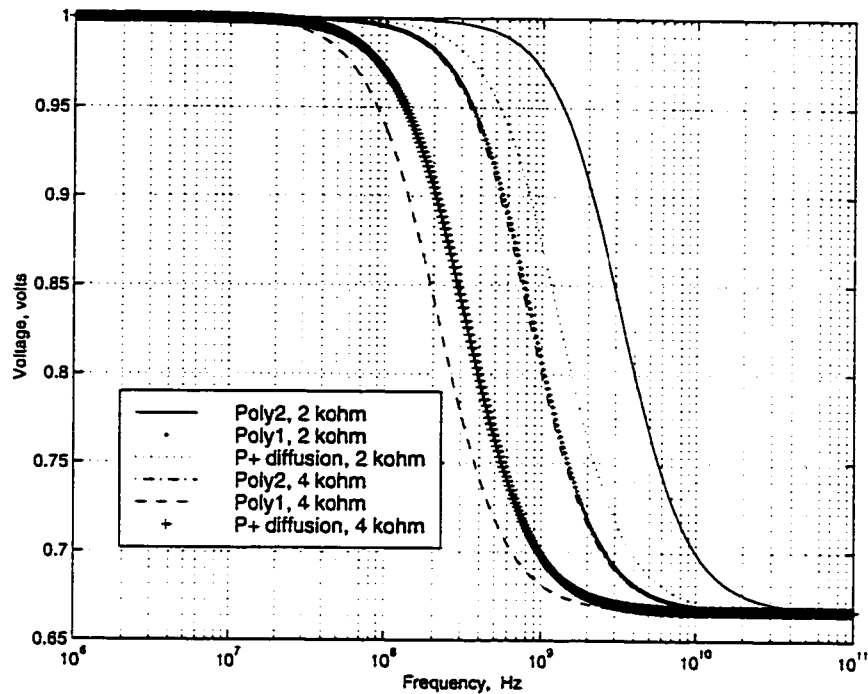


Figure 3.3: Frequency Response of various Resistors.

selected over n+ since it could achieve the largest sheet resistance for the TSMC 0.35  $\mu\text{m}$  CMOS technology.

It can be seen from Figure 3.3 that the poly-2 resistors have the widest frequency response, however the p+ diffused resistors have a better frequency response over the poly-1. When simulating the data a simple voltage divider of ideal resistors was used. The load resistor was modeled with the parasitics that are expected for the appropriate type of device. This forms a network that has a resistance in parallel with the parasitic capacitance, which forms a transfer function having a single pole and zero. This is evident in Figure 3.3, but the variation in the frequency response is the feature to be noted.

Although the frequency response of the poly-2 resistors is wider than that of

the p+, an increased area of three times is unacceptable at this stage. Also, the reduced response of the p+ diffused devices is still acceptable for the desired 20 MHz bandwidth of the overall ladder, depending on the chosen sizes of resistor values.

### 3.1.1 Resistor Size

When selecting a size for the R value in the R-2R ladder, there must be a trade-off between chip area, parasitic capacitance and loading effect caused by the ladder. The loading effect is due to the connection for each input pad, there is a parallel combination of eight ladder circuits.

For the given dimensions of the chip, R for the ladder was chosen to be 2 k $\Omega$ . This results in a load of 250 ohms at each input pad, since eight ladders are stacked at each input pad. Figure 3.4 shows the general layout for the common building blocks for resistors. The scale at the right of the diagram is in units of microns. Each vertical block represents one 2 k $\Omega$  resistor with an approximate area of 150  $\mu m^2$ . In order to achieve better matching for the values of 2 and 4 k $\Omega$  resistors, due to the R and 2R nature of the ladder, copies of these blocks are combined to produce the larger sized resistor. This will allow the 2R resistors to have exactly twice the number of via's and contacts, thus keeping the additional resistive values to be proportional. This is an important consideration with regard to the overall matching of devices.

### 3.1.2 Switch Sizes

The sizes that were selected for the analog switches were based on transistors that had a minimum channel length, 0.35  $\mu m$ . As previously stated there is a trade-off between the low on-resistance and gate capacitance for larger transistors. Using the

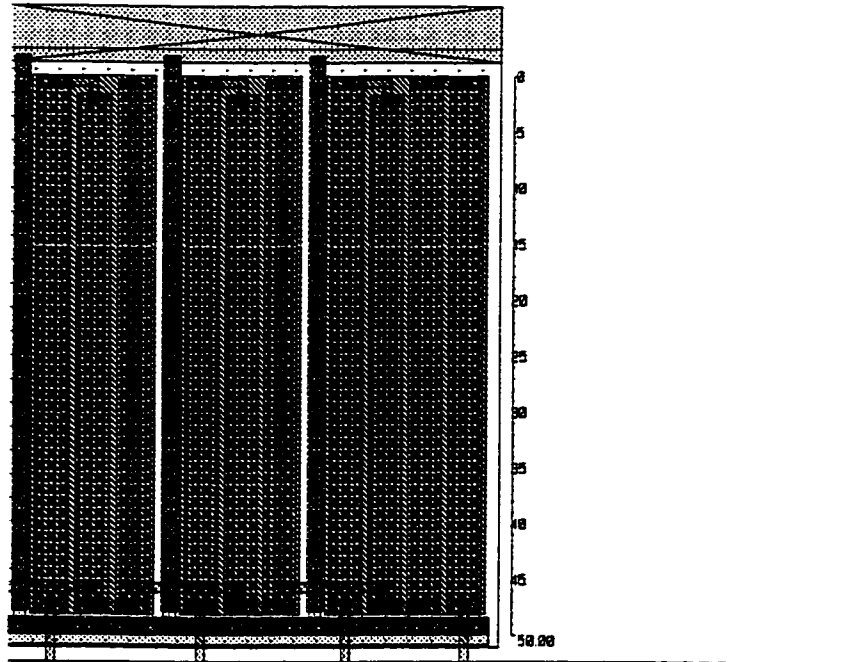


Figure 3.4: Resistor Layout, ICDCYSA1.(units in  $\mu\text{m}$ )

minimum geometry size for the length will provide a greater  $W/L$  ratio and maintain a low area for parasitics.

When considering parasitic capacitance, the gate to source capacitance ( $C_{gs}$ ) should be noted. For the switches the capacitance  $C_{gs} \approx \frac{1}{2}C_{oxide}$  [16], where the oxide capacitance can be described as:

$$C_{oxide} = \frac{\epsilon_{ox}}{t_{ox}} \times W \times L \quad (3.1)$$

where  $\epsilon_{ox} \approx 0.35 \text{ pF/cm}$  which is the permittivity of silicon dioxide and  $t_{ox}$  is the thickness of the oxide which was taken to be  $7 \times 10^{-7} \text{ cm}$ . Therefore for a transistor size of  $100 \mu\text{m}/0.35 \mu\text{m}$   $C_{oxide} \approx 175 \text{ fF}$ , resulting in a  $C_{gs} = 87.5 \text{ fF}$ .



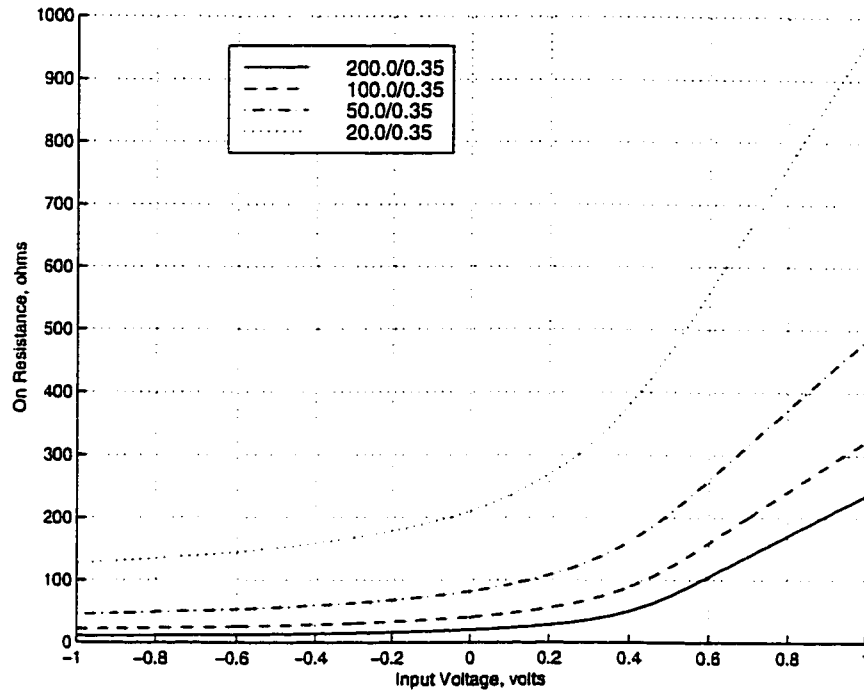


Figure 3.5: On Resistance of Single Transistor NMOS Switches. HSPICE Level 28.

### 3.1.2.1 Single Transistor Size

Using Figure 3.5, the on-resistance can be seen to vary with the input voltage to the transistor and the transistor size. For the present switch, the main area of interest is at an input voltage of zero volts, since the switch is grounded and operating in the triode region. This specific region is shown in Figure 3.6.

When selecting an appropriate size for the transistor switch, its effect on the  $2R$  branch resistance must be taken into account. It is possible to decrease the size of the  $4\text{ k}\Omega$  resistor to incorporate the on-resistance of the switch, thus decreasing the error at the output. When making the final selection for the switch an allowance of 1% of the  $2R$  branch resistance was given for the on-resistance. To achieve a transistor with an on-resistance of  $40\ \Omega$  a  $W/L$  ratio of  $100/0.35\ \mu\text{m}$  was selected.

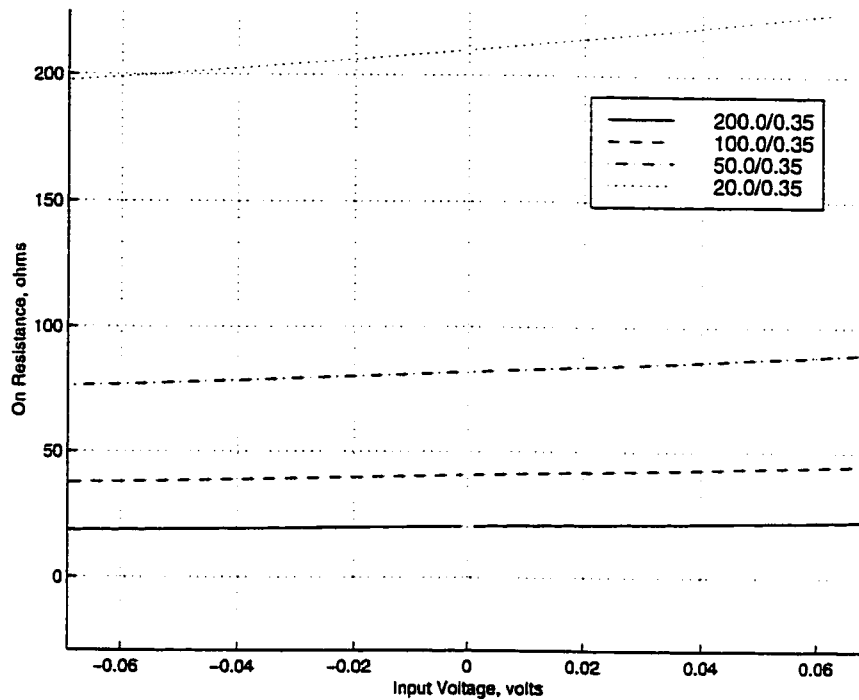


Figure 3.6: On Resistance for a Grounded NMOS Switch. HSPICE Level 28.

Another concern with regard to the final selection of transistor size is the distortion that occurs due to the switch. Figure 3.7 shows the distortion that occurs as a function of switch size. The hand analysis for the distortion is shown in Appendix B, where the cause is the variation of the drain-to-source voltage on each switch due to the input voltage for each  $2R$  branch. The distortion being investigated is the deviation, of the output, from the general shape of the applied input voltage, that is applied into a single branch of the ladder structure. The hand analysis referred to in

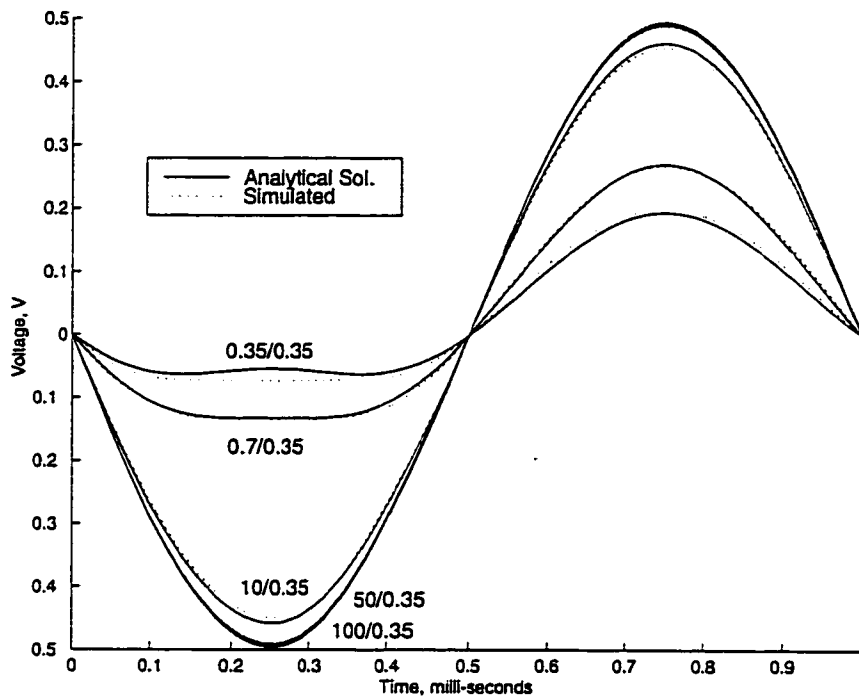


Figure 3.7: Distortion caused by varying sizes (W/L) of a single transistor switch for the MSB of the R2R Ladder. Input of  $2V_{PP}$ , 1 kHz with expected output of  $-1V_{PP}$ . HSPICE LEVEL 28.

Figure 3.7 is plotted using:

$$\begin{aligned}
 V_{out} = & \frac{1}{32b^3R^2\beta_n^2} + \frac{45}{6144b^7R^4\beta_n^4} \\
 & - \left( \frac{1}{2} - \frac{1}{4R\beta_nb} - \frac{9}{384b^5R^3\beta_n^3} \right) \cdot \sin \theta \\
 & - \frac{1}{2} \left( \frac{1}{16b^3R^2\beta_n^2} + \frac{15}{768b^7R^4\beta_n^4} \right) \cdot \cos 2\theta \\
 & - \frac{3}{384b^5R^3\beta_n^3} \cdot \sin 3\theta + \frac{15}{6144b^7R^4\beta_n^4} \cdot \cos 4\theta + \dots \quad (3.2)
 \end{aligned}$$

where R is the R-value for the R2R ladder,  $\beta_n = \mu_n C_{ox} \frac{W}{L}$ ,  $a = \frac{1}{4R\beta_n} + \frac{V_{GS} - V_{Tn}}{2}$  and  $b = \frac{1}{2R\beta_n} + V_{GS} - V_{Tn}$ . The input waveform was a  $2V_{PP}$  1 kHz signal, which should result in an inverted  $1V_{PP}$  output signal.

The accumulative harmonic distortion (HD) caused by the higher frequency components can be calculated from [23],

$$HD = \sqrt{\frac{\sum_{i=2}^4 |X_i|^2}{|X_1|^2}} \cdot 100\% \quad (3.3)$$

where  $X_i$  is the magnitude of the  $i^{th}$  harmonic, and  $X_1$  is the magnitude of the fundamental frequency. The calculated values of HD are 27.49%, 16.92% , 0.264% , 0.0118% and 0.003 % for W/L ratios of 0.35/0.35, 0.70/0.35, 10/0.35, 50/0.35 and 100/0.35, respectively. In order to validate calculated values of HD, the total harmonic distortion (THD) for a single branch was simulated and calculated using HSPICE which resulted in comparative values of 22.14% 15.99% , 0.2457% , 0.010% and 0.0026%. The accumulative distortion caused by all branches in the ladder will have a worst case value of eight times that of the MSB-branch, which was calculated above. This is due to the largest variations in drain-to-source voltage being the greatest in that branch.

At this point it can be shown how the on-resistance of the switch should be incorporated into the branch resistance. The branch error for a 100/0.35  $\mu\text{m}$  switch is shown in Figure 3.8. Both the hand-analysis and simulated results have the same sinusoidal shape with approximate amplitude of 1  $V_{pp}$ , and only a difference of 0.04 % occurs between the two. These results assume that the on-resistance of the switch has not been compensated by adjusting the 4 k $\Omega$  (2R) branch resistance. Once the 4 k $\Omega$  resistors have been reduced by the switch resistance, the percent deviation attains a significantly smaller value, as shown in Figure 3.9.

The selection of 100/0.35  $\mu\text{m}$  switch geometry was found to be suitable. By adjusting the branch resistances, the error can be minimized for each branch. The chosen size of switch also has a low value for HD, which is also a desirable factor.

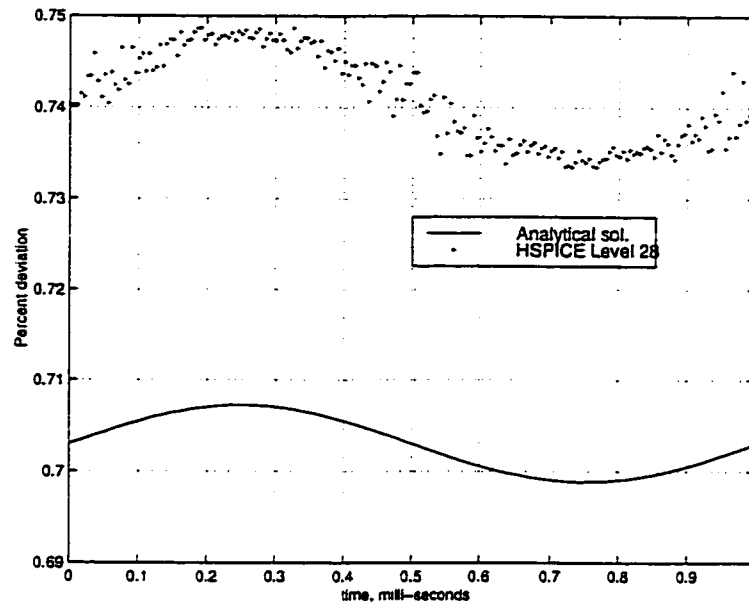


Figure 3.8: Deviation from expected output, for a 1kHz input signal.

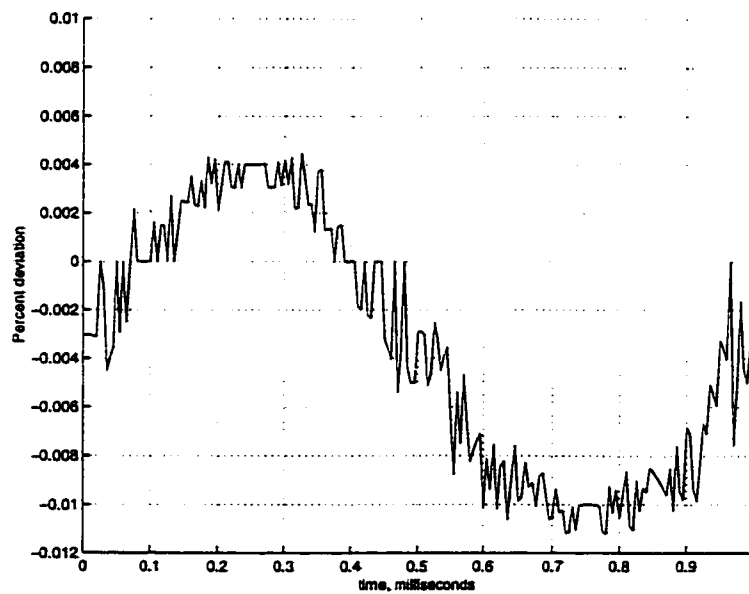


Figure 3.9: Deviation from expected output, for a 1kHz input signal with corrected branch resistance : HSPICE LEVEL 28.

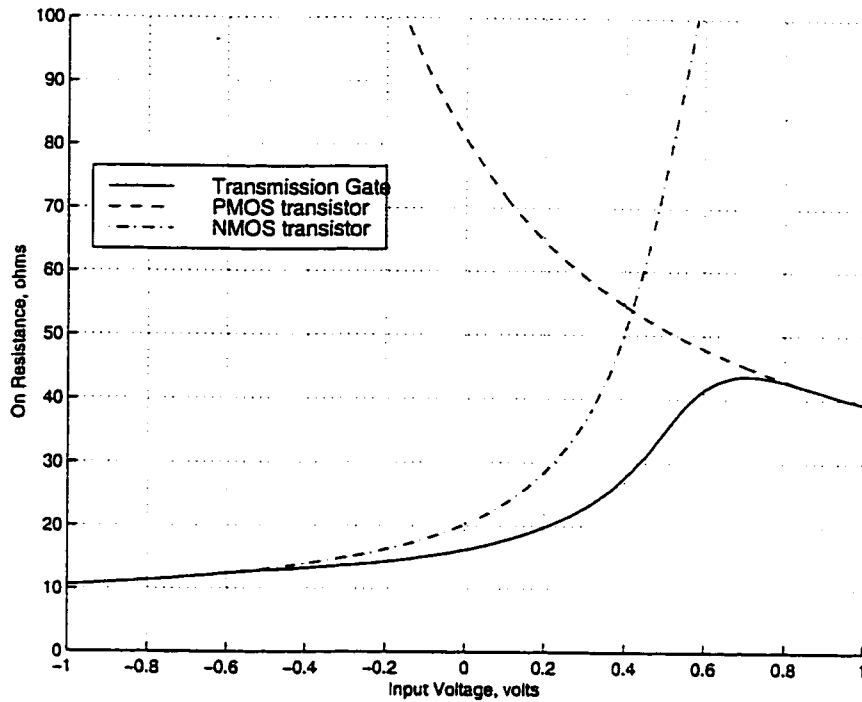


Figure 3.10: Transmission Gate with both transistors having a  $W/L$  of 200.0/0.35  $\mu\text{m}$ . HSPICE Level 28.

### 3.1.2.2 Transmission Gate Size

When selecting transistor sizes for the transmission gates, the correct ratios for transistor sizes must be selected for n and p-type transistors. Since the on-resistance will vary with the input voltage, it is preferable to minimize the variation of this value. Figure 3.10 shows a design where both types of transistors have the identical  $W/L$  ratios. This variation of the on-resistance is not desirable, and by adjusting the  $W/L$  ratio for the NMOS transistor a suitable response can be attained. Figure 3.11 identifies the case where the on-resistance varies by less than  $10\ \Omega$  as input voltage varies from  $-1\text{V}$  to  $+1\text{V}$ .

The varying on-resistance of the transmission gates causes additional error at

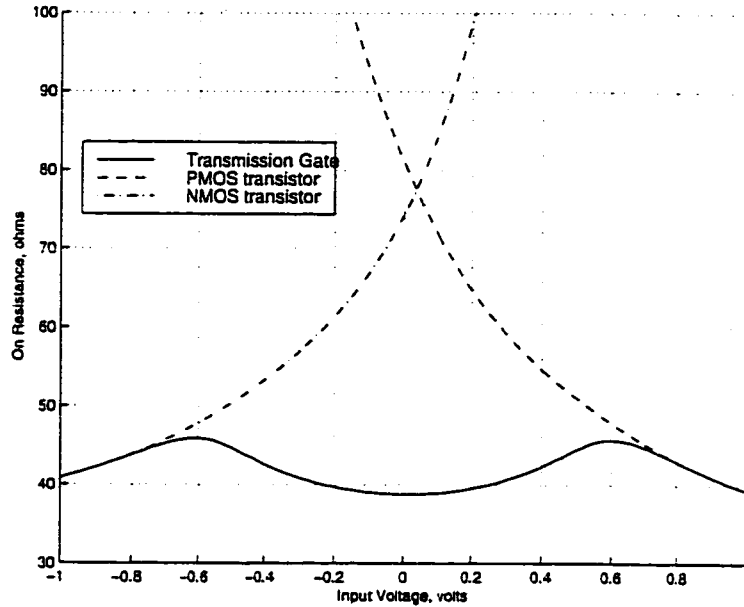


Figure 3.11: Transmission Gate with 200.0/0.35  $\mu\text{m}$  PMOS, and 55.0/0.35  $\mu\text{m}$  NMOS. HSPICE Level 28 .

the output. However, this can be compensated by increasing the feedback resistor in the output amplifier by the same amount as the on-resistance of the transmission gate. The direct input to the ladder becomes,

$$v_{new} = v_{in} \frac{R}{R + R_{TG}} \quad (3.4)$$

where  $v_{in}$  is the original input signal,  $R_{TG}$  is the on-resistance of the transmission gate and  $v_{new}$  is the new input signal directly applied to the ladder structure. Since the node voltages of the ladder will now be adjusted by the new input, the gain of the overall circuit will need to be increased to compensate for the attenuated input. The general equation describing the output can be modified from the original equation

2.17 as follows:

$$\begin{aligned}
 v_{out} &= -\frac{R + R_{TG}}{R} \left[ \frac{1}{2} v_{new} \phi_n + \frac{1}{2 \cdot 2} v_{new} \phi_{n-1} + \dots + \frac{1}{2^{n-1}} v_{new} \phi_2 + \frac{1}{2^n} v_{new} \phi_1 \right] \\
 &= -\frac{R + R_{TG}}{R} \left[ \frac{1}{2} v_{in} \frac{R}{R + R_{TG}} \phi_n + \frac{1}{2 \cdot 2} v_{in} \frac{R}{R + R_{TG}} \phi_{n-1} + \dots \right. \\
 &\quad \left. + \frac{1}{2^{n-1}} v_{in} \frac{R}{R + R_{TG}} \phi_2 + \frac{1}{2^n} v_{in} \frac{R}{R + R_{TG}} \phi_1 \right] \tag{3.5}
 \end{aligned}$$

When simplified by cancellation of the terms  $(R + R_{TG})$ , equation 3.5 reduces to the original equation for  $v_{out}$ . The percent error in the output will therefore be dictated by the variation in the on-resistance of the transmission-gate. The variation due to the chosen sizes of transistors results in an error of approximately  $\pm 0.2\%$ , for an input voltage varying from  $-1V$  to  $+1V$ .



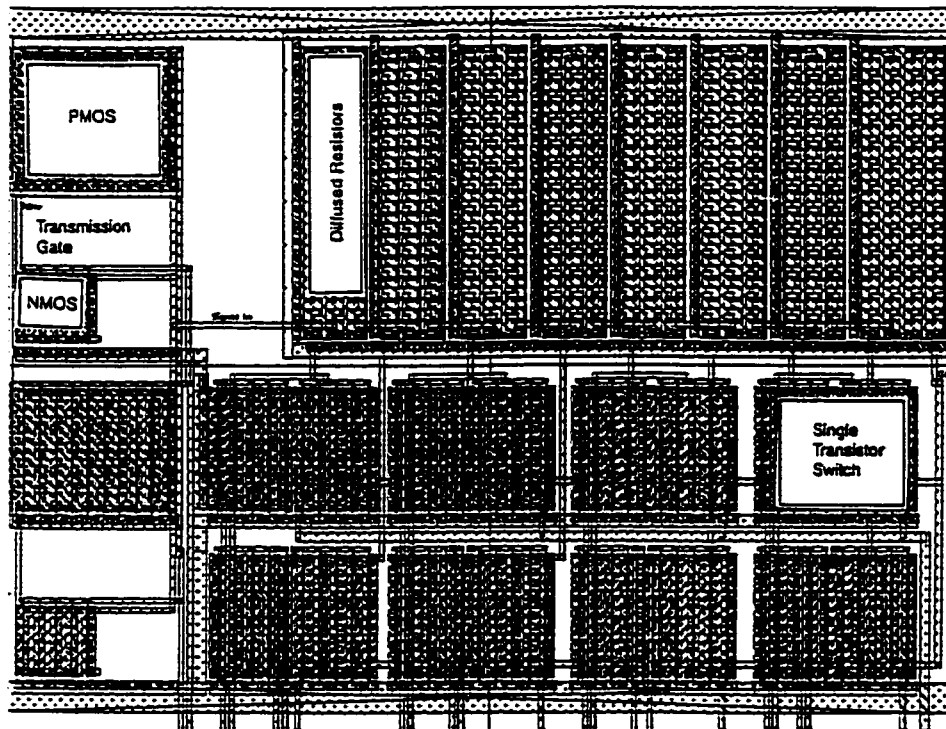


Figure 3.12: Multiplier cell, ICDCYSA1.

This concludes the discussion of the multiplier components. Figure 3.12 shows the layout that includes both the resistor network for the ladder and the analog switches used to control the signals. Simulating the finalized schematic version of the R-2R ladder the frequency response can be investigated. Figure 3.13 shows the response for the various node-voltages, as labelled in Figure 3.14. Due to the R-C network that is formed by the resistors and their subsequent parasitic capacitances, the node-voltages on the input to the 2R branches have a decreasing frequency range as the nodes approach the LSB. From this it can be understood that the bandwidth of the ladder will be dependent on the selection of bits.

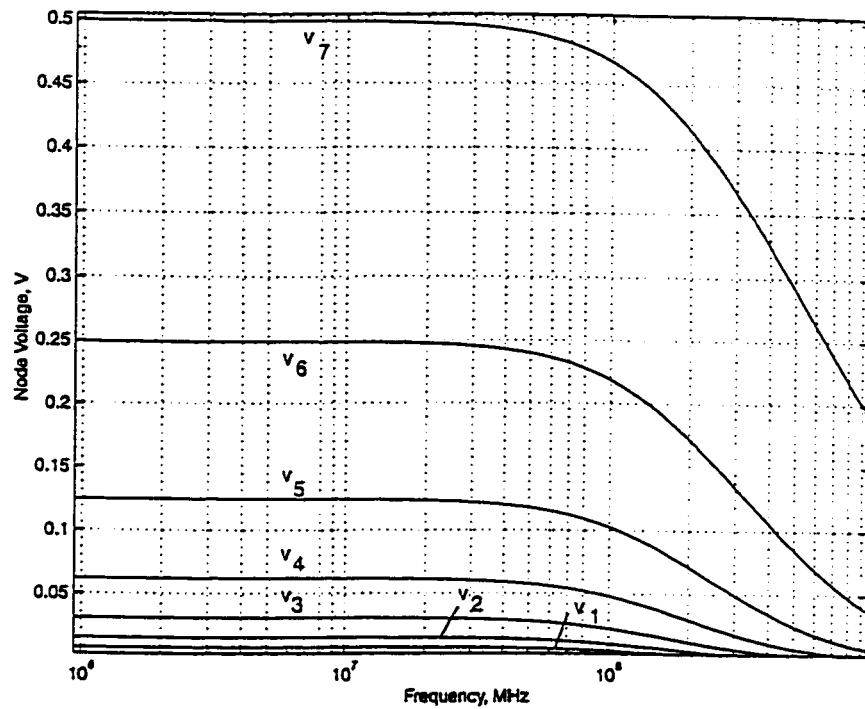


Figure 3.13: Frequency response of node voltages for completed R-2R Ladder, with chosen sizes of resistors and switches. An AC input of 1V was used to generate the results.

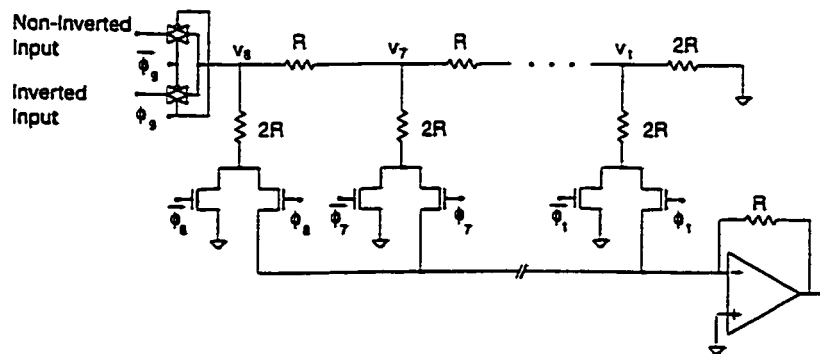


Figure 3.14: Labelling for node voltages.

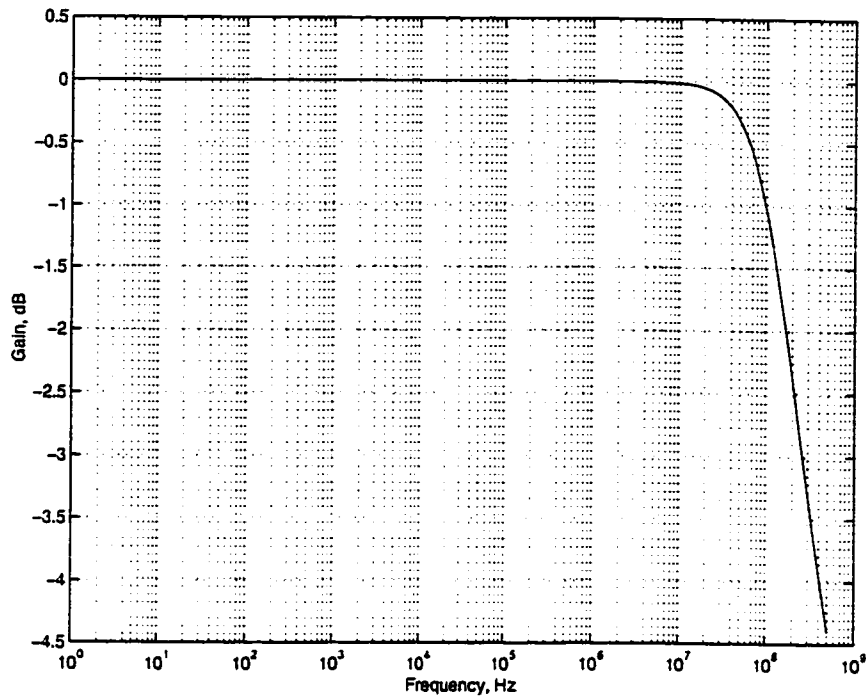


Figure 3.15: Frequency response of completed R-2R ladder, with chosen sizes of resistors and switches. Operating at AC input of 1V, with maximum gain.

Figure 3.15 shows the frequency response of the implemented ladder structure. The response includes the parasitic capacitances associated with both the drawn resistors and switches. For a gain where the only bit selected is the LSB, the 3dB frequency will only attain a value of approximately 90 MHz, which is comparable to the roll-off frequency for the node-voltage  $v_1$ . This selection of gain will be the lowest 3dB frequency for various gain settings. The frequency response indicates that the chosen sizes of components achieve the required 3dB bandwidth of 20 MHz.

The completed multiplier was also simulated to obtain the overall accuracy due to the selection of components. For simulation purposes, the feedback resistor on the amplifier was set to 2043 ohms. The increase of 43 ohms was to test the circuit's

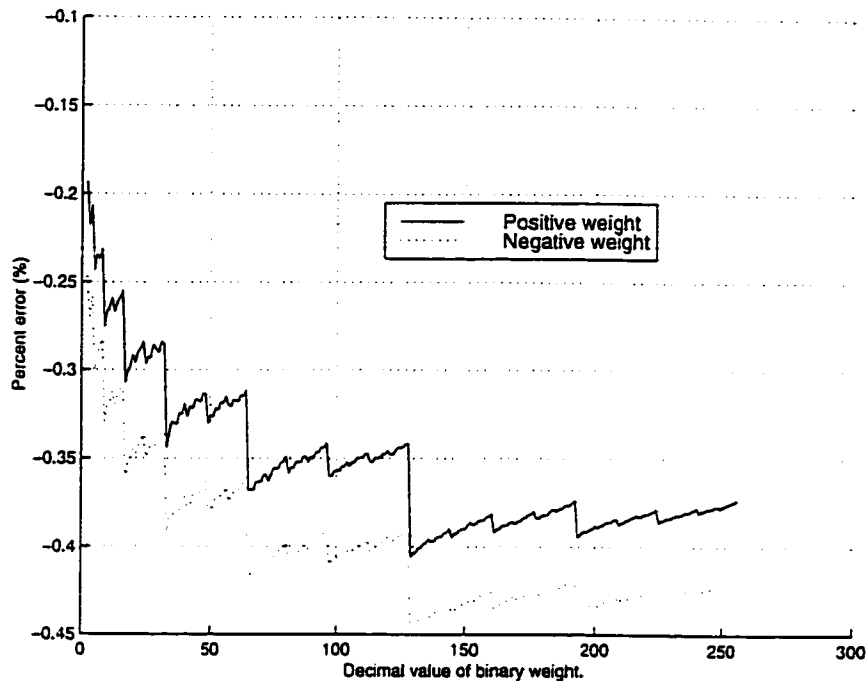


Figure 3.16: Percent error for a single multiplier with 1 V DC-input, for both positive and negative weights.

performance with the addition of transmission gates at the input to the ladder. The input to the circuit was set to a +1 V DC-input along with its complimentary -1 V supply for negative weights. The input voltages are at the extreme range of the required inputs, and will also test the full range for the transmission gates.

The output for varying multiplier weights will not be shown here, as the output matches closely with the ideal values. However, the overall accuracy is shown in Figure 3.16. The precision of the multiplier with all additional components is well within the range of the required 1 % accuracy. A point of interest on Figure 3.16 is the errors that have a sudden change. This sudden increase is due to the weights increasing to the point where the next significant bit is toggled on, while the lower bits are toggled

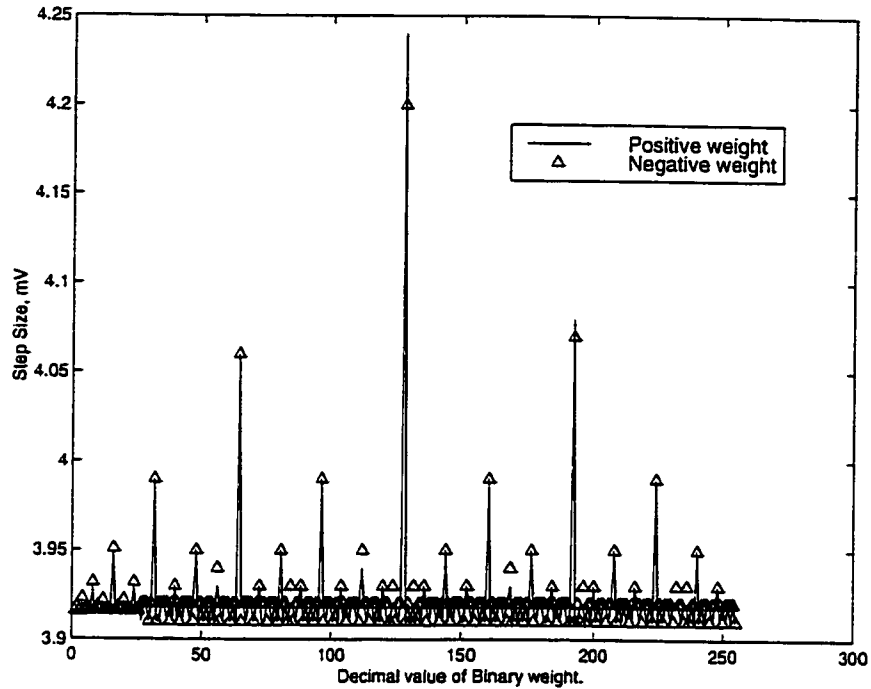


Figure 3.17: Step size between adjacent output voltage levels, for both positive and negative weights.

off. This indicates that the step size between adjacent weights is not equal and has the largest change in step as the next higher bit is toggled on. Figure 3.17 indicates this point, as the most severe level changes are at the points mentioned.

The reason for these large changes is due to the size of the transistor switches and the current levels in each branch. Since all switches are of the same size but current levels increase in each branch from LSB to MSB, the value of  $V_{DS}$  for each switch is increasing. From the previous chapter the on-resistance of the switch was shown to be:

$$(R_{on})_n = \frac{L}{\mu C_{ox} W (V_G - V_{Tn} - V_{DS})} \quad (3.6)$$

Therefore, as there is an increase in the value of  $V_{DS}$  the on-resistance of each switch

will also increase. This increasing resistance value causes the various voltage levels in the ladder to deviate from ideal conditions, and cause sudden jumps in error. However, for the switches chosen the error already falls within tolerated levels and will remain as chosen.

A final point for the performance of the multiplier is the linearity. From the previous curves concerning accuracy for various bit patterns, Figure 3.16, the worst change in error was seen due to the MSB. This is therefore also the largest deviation from the expected linear behaviour of the output, as seen from the same figure that the accuracy increases with the higher weights. By comparing the full range of inputs, -1 V to +1 V, a figure for the linearity can be measured from simulation due to the deviation of the MSB. Values of percent linearity were calculated using

$$\text{Linearity Error} = \frac{\text{Ideal} - \text{Simulated}}{\text{Full Scale Value}} \times 100\% . \quad (3.7)$$

Figure 3.18 shows the performance of the multiplier, and the general shape of the curve can be noticed to have large swings in linearity due to the transmission gates at the input. The linearity for an input of zero volts has been smoothed in the graph, since no output is expected at that point. As can be seen from the curve, the requirement of a 1% linearity can also be achieved with the selection of components made.

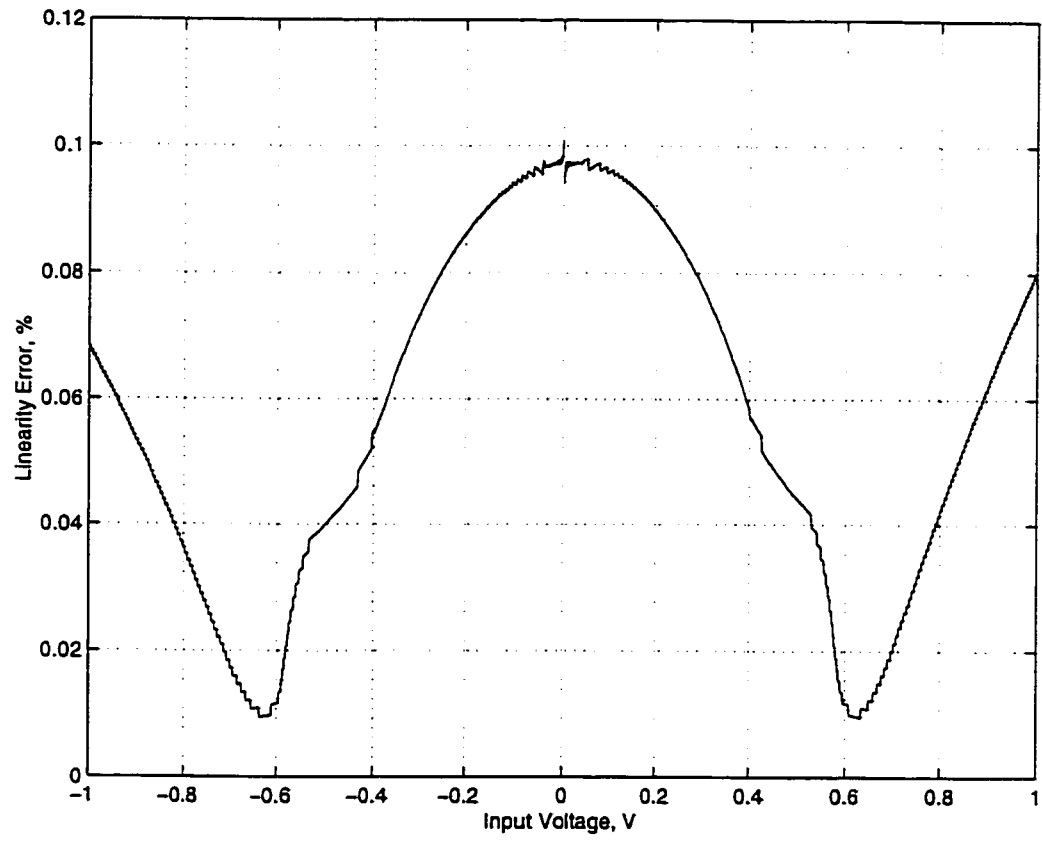


Figure 3.18: Linearity of R-2R ladder over the full range of input.

## 3.2 Digital Control Circuitry

In order to control the weights for the Ladder, additional circuitry had to be implemented. Since there are 96 multipliers requiring nine data-bits that have to be controlled, the chosen method employed nine shift-registers all using the same global clock signal. A single shift register can be seen in Figure 3.19, where the length of the unit is equal to the number of weights required. Each shift-register receives its signal from one data-bit of the DSP. In addition the global clock signal for the shift-registers is controlled by the DSP. For the specific application, the output of the last flip-flop in the shift-register (bit-out in the diagram) is taken to a digital output pad to allow access for another IC. This helps to ensure modularity of the design. The D-FF's are composed of a simple master-slave topology [24], as shown in Figure 3.20. The d-Latches, shown in Figure 3.21, used as the master-slave components are level-sensitive, which helps to reduce the concerns of timing problems in the circuit.

From the timing diagrams included in Figure 3.20, it can be seen that the addition of inverters is used to invert and delay ( $t_d$ ) the clock signal. This is to ensure that the slave d-latch is disconnected from the master before the new value of the D-input is clocked. The static slave cell is then used to update the next master d-latch in the shift register.

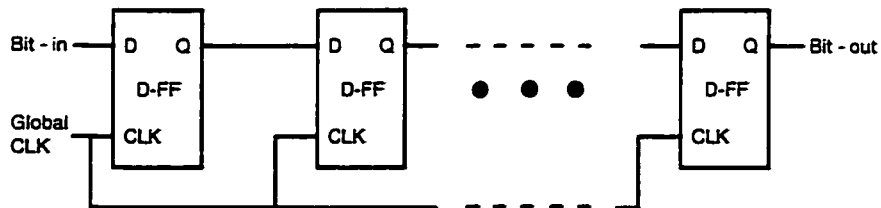


Figure 3.19: Shift Register using D-Flip Flops.



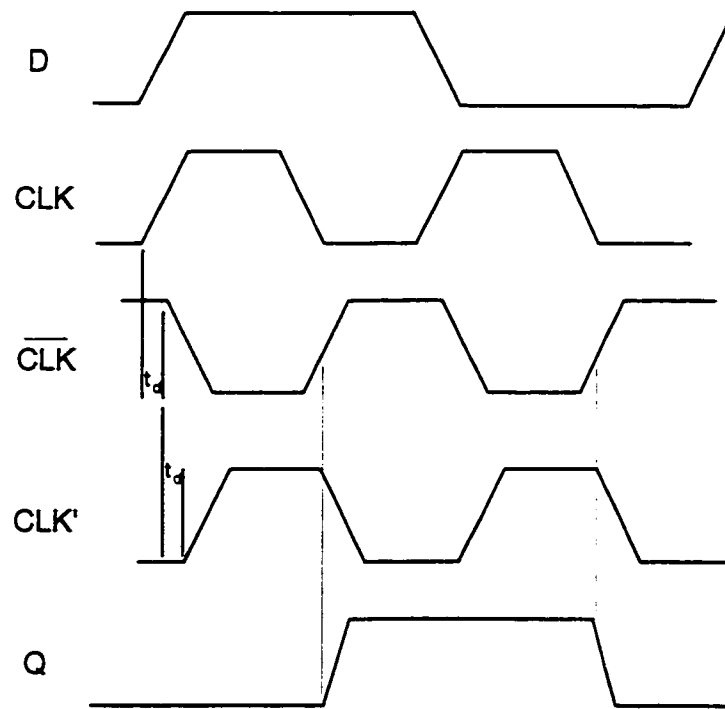
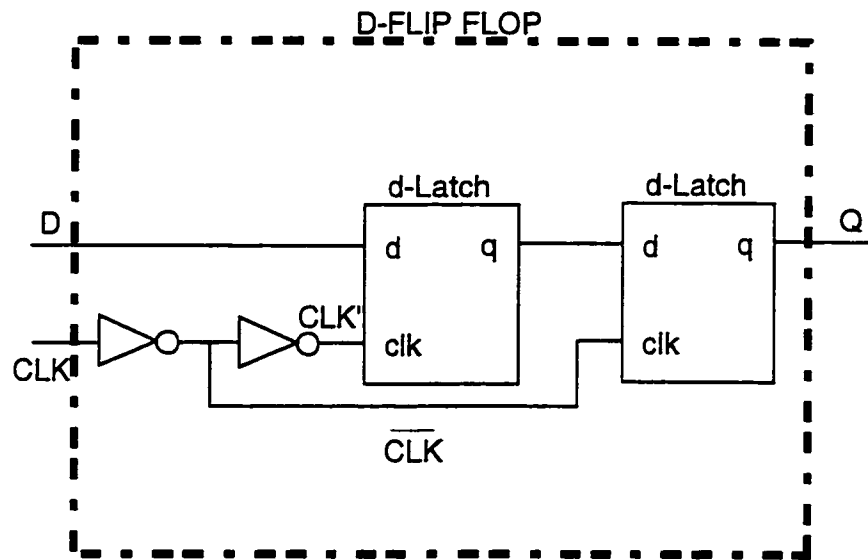


Figure 3.20: Master-Slave topology for the DFF.

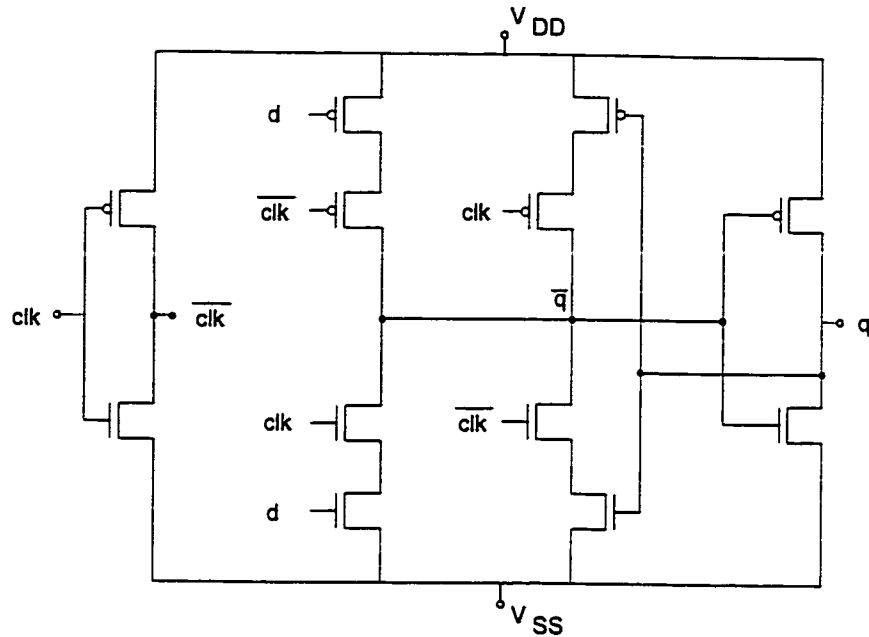


Figure 3.21: Circuit Diagram for D-Latch.

Since the weights of all 96 multipliers need to be updated simultaneously an additional latch is required for each bit of the shift register. The latches are subsequently controlled by a single global strobe signal. Figure 3.22 shows how the additional latches are included with the shift registers, and also elaborates on the timing for the circuitry. While the latches hold the current bit-setting for the multipliers, a new set of weights can be clocked into the shift-registers. Once the new weights have been completely loaded into the shift-registers, a strobe signal can be sent to update the weights to the new settings. This will allow for the minimum transient interference on the summer output signals while attaining the new output levels. As well, since the shift register utilizes a master-slave topology the strobe signal can follow the clock for the one pulse to load the new multiplier weights. The last setting on the slave-latches of the flip-flop will be sent to the additional latches.

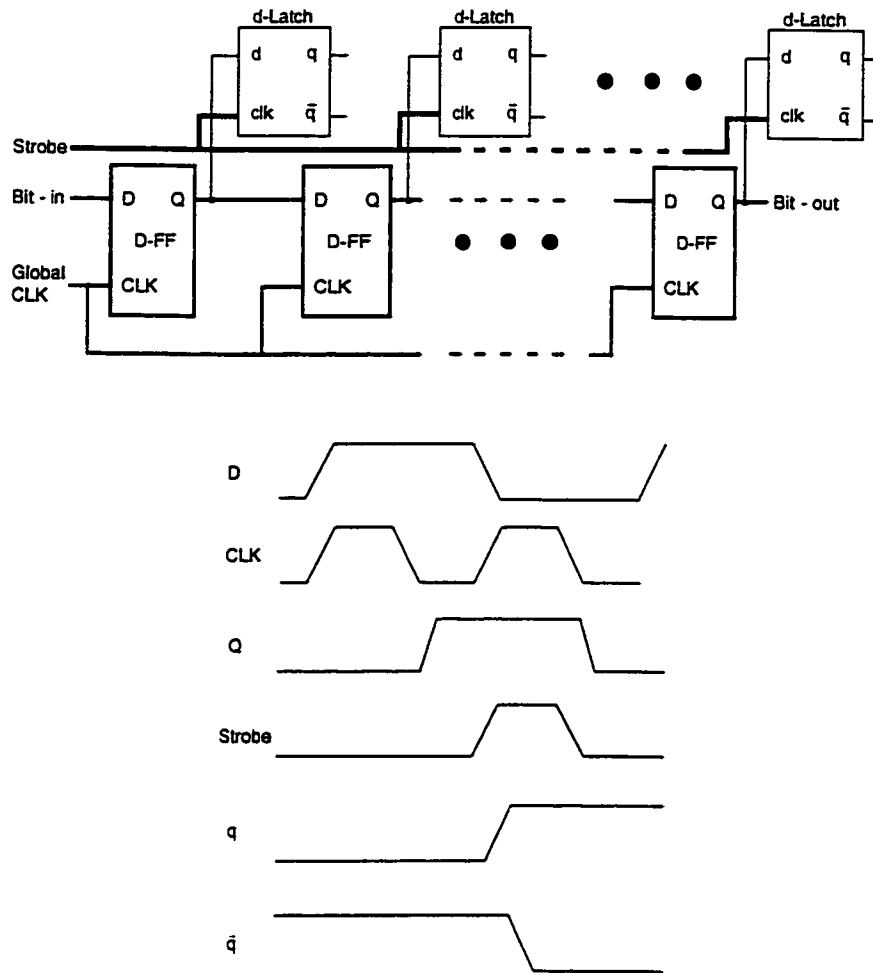


Figure 3.22: Shift Registers with Latches.

While this is being performed the next set of weights can also be loaded as it will not interfere with the slave-latch setting until the low cycle of the clock pulse. At that point the strobe signal will have already disconnected the additional latches.

The outputs from each additional latch,  $q$  and  $\bar{q}$ , are connected to the appropriate transistor switches in the ladder. For the weight of the multiplier, the  $q$  output is connected to the switch directing output to the summers, and the  $\bar{q}$  output is connected to the switch to analog ground. The sign bits of the multipliers also use

signals from the additional latches by connections to the transmission gates at the input of the multipliers. The levels from the latches are connected such that a low  $q$  output (-1.5 V) indicates a positive weight, and a high output (+1.5 V) indicates a negative weight.

Due to the symmetry of the weights, it should be noted that the shift-registers and corresponding latches need only to have a length of 48. One nine-bit weight, including sign, can be used to control two different multipliers. From the mathematics of the system, as shown in Chapter 1, some of the weights for two multipliers will be identical, while other pairs will only be different in sign. Since from the latches it is possible to access both the  $q$  and  $\bar{q}$  signals, the only requirement for the control signals is to have a more elaborate interconnect scheme. This is preferable on the basis of not only chip area, but also in that it will allow for a new full set of weights to be loaded at an increased rate, for a specific clock speed.

The components used such as the d-latches and inverters were taken from a standard parts library supplied by CMC. The layouts for each device were included in the kit, therefore no modifications were made to the structures of the components except to combine multiple items where required. Included for the digital components were the clock-drivers with the largest fan-out available in the kit. Each of these device characterizations that are of note here are listed in the Tables 3.2, 3.3 and 3.4 [25]. The rise ( $t_r$ ) and fall ( $t_f$ ) times are the time for the transition between 10% to 90% of the output signal change [26]. However the propagation delay is defined as the time difference between the input crossing the threshold voltage until the output signal crosses the threshold voltage [25]. The propagation delay takes on two different values,  $t_{pL-H}$  for a changing input to rising output and  $t_{pH-L}$  for a falling output.

<i>Characteristic</i>	<i>Input transition (ns)</i>	<i>Value (ns)</i>
$t_{dL-H}$	4.5	1.6 @ 5 pF
$t_{dH-L}$	4.5	1.2 @ 5 pF
$t_r$	4.5	1.0 @ 5 pF
$t_f$	4.5	1.1 @ 5 pF

Table 3.2: Transition times for clock driver for capacitive load.

<i>Characteristic</i>	<i>Input transition (ns)</i>	<i>Value (ns)</i>
$t_{dL-H}$	4.5(1.8)	0.66(0.58)
$t_{dH-L}$	4.5(1.8)	0.71(0.63)
$t_r$	4.5(1.8)	0.71(0.66)
$t_f$	4.5(1.8)	0.40(0.37)

Table 3.3: Transition times of d-latch for various input transition.

<i>Characteristic</i>	<i>Input transition (ns)</i>	<i>Value (ns)</i>
$t_{dL-H}$	1.8	0.41
$t_{dH-L}$	1.8	0.41
$t_r$	1.8	0.86
$t_f$	1.8	0.69

Table 3.4: Transition times for Inverters.

Each of the digital signals to the input of the multiplier chip are received from the DSP. Separate data lines are required for all signals including the global clock and strobe. Therefore the DSP must ensure that all outputs are synchronous, and that the data bits have twice the duration of the clock pulse, since the DSP is simulating the clock for the multiplier chip.

Although the required clock speed was to only attain 1MHz, Figure 3.23 shows performance of the shift register with the additional latches at a speed of 5MHz. In order to show the changing response due to the strobe on the additional latches, the simulation was set such that there would be a continuous change with each clock cycle. This was also done to indicate that there is not a requirement to delay the shifting of a new weight while the additional latches are being updated.

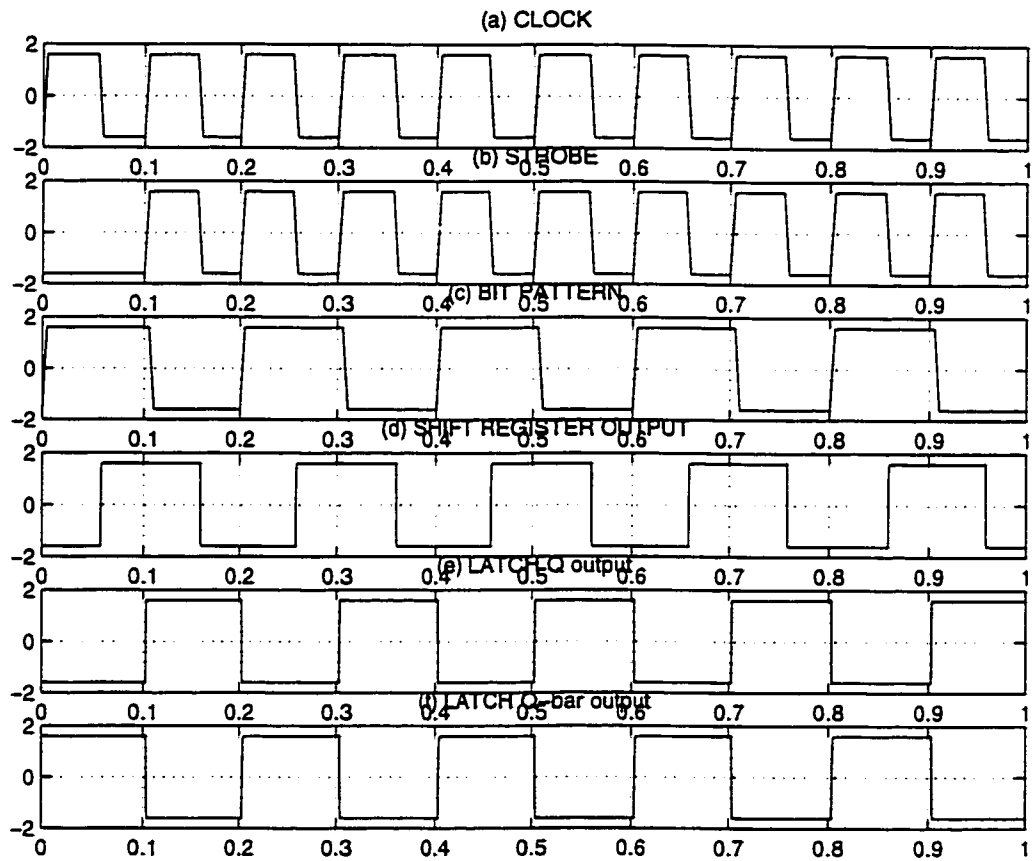


Figure 3.23: Timing sequence of digital components running at 5 MHz, all y-axis values measured in volts and x-axis values are in  $\mu\text{s}$ .

### 3.2.1 Transient Response caused by Latch switching

Due to the relatively fast switching speeds of the d-latches, effects will be seen on the analog switches of the R-2R ladders. Therefore, consideration must be given to the transient behaviour of the output signal at the point where the multiplier weights are being updated. The changing of states of the single transistor switches at the time when a strobe signal is sent will result in transient spiking at the output. The spiking for a change in the most significant bit can be seen in Figure 3.24. This is due to the charging and discharging of various parasitic capacitances.

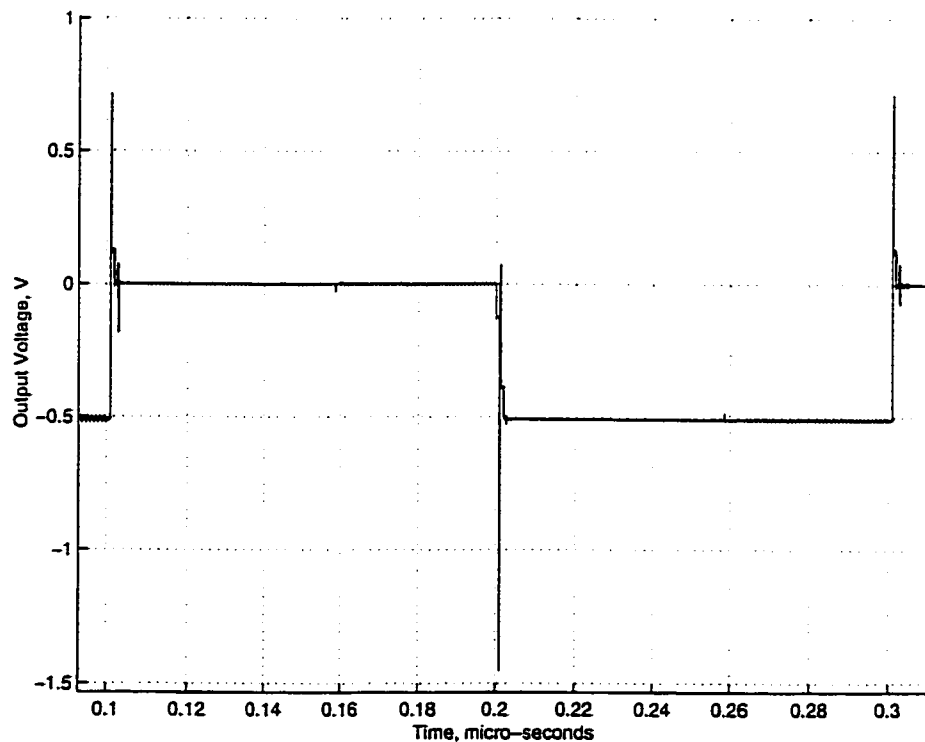


Figure 3.24: Transient spiking for a +1 V DC input, with the toggling of the MSB every 100 ns for a positive weight.



For any given switch two states are possible, off or on. Voltage dependent capacitances within the analog switches will have varying magnitudes between the two states. In the off-state capacitance  $C_{GB}$  will have comparatively larger magnitude than in the on-state. Components such as  $C_{GS}$  and  $C_{GD}$  will have larger magnitudes during the on-state than during the off-state [19, 22]. The varying values of capacitances are listed in table 3.5. In the table the parameter LD represents the lateral diffusion of the source and drain.

At any given state the various capacitances will be charged due to the different voltage levels of the switch and the surrounding nodes. The charge can be calculated by

$$Q_p = C_p V \quad (3.8)$$

where  $Q_p$  is the charge on the parasitic capacitance,  $C_p$  is the corresponding parasitic capacitance and  $V$  is the voltage across the parasitic [27]. Once the switch changes states, the resulting change in the magnitude of capacitances will result in excess charge being injected into the circuit, or charging of the increased capacitance from the circuit [27, 28, 29]. This charge will therefore correspond to a change in current seen at the output of the summer for the time period of the switching of states since,

$$i_c = \frac{dQ_p}{dt} = \frac{\Delta Q_p}{\Delta t} \quad (3.9)$$

<i>Parasitic Capacitance</i>	<i>Off-state</i>	<i>On-state (triode)</i>
$C_{GB}$	$C_{ox} W_{eff} L_{eff}$	0
$C_{GS}, C_{GD}$	$C_{ox} LD W_{eff}$	$\frac{1}{2} W_{eff} L_{eff}$

Table 3.5: Parasitic Capacitance approximations taken from [19, 22]

where  $i_c$  is the current caused by parasitic and  $t$  is the time for the change in state of the switch. From previous calculations  $C_{GS} = 87.5$  fF for a switch of  $100/0.35$   $\mu\text{m}$  while operating in the triode region. Therefore for the case when  $1.6$  V is across the parasitic, due to the switching levels, a charge of  $140$  fC will be on the capacitor. The resulting current spike when the switch is turned off can reach  $280$   $\mu\text{A}$  for a transition time of  $0.5$  ns. This current spike will then be seen across the feedback resistor of the summer, which results in a voltage spike of  $0.56$  V.

The spiking as seen at the output of the summer (op-amp) will however be limited by its corresponding slew rate. The switching of the transistors and the resulting voltage spikes will result over a time period of a few nanoseconds, due to the switching characteristics of the latches. Under ideal conditions the spiking will be seen, however inductance in the line connecting the summer and the multipliers will reduce high frequency components such as spiking. As well the spiking will only result on the strobing of the multipliers, or every 48 clock pulses.

## Chapter 4

# Testing and Results

Initial testing of the multiplier chip was completed by bread-boarding a circuit to test its performance. Although the most vital components of the chip are the multipliers themselves, the first stage of testing was to investigate that the shift registers were operating properly. The bread-board configuration for the original testing used simple toggle switches and tested the first multiplier attached to the shift-register. Once a weight had been shifted into the first multiplier, and the weights had been strobed, an output voltage occurred which appeared as expected. This initially indicated that the shift register was clocking in the data on the input lines, at least for low speed.

In order to test the response and accuracy of the multiplier the full range of multiplier weights were clocked in by hand. The setup was such that the input voltage was 1 V DC, and the multiplier sign was set for a positive weight. In order to achieve the appropriate gain, the feedback resistor on the amplifier had to be adjusted for each chip. The ideal value of the resistor was expected to be 2000 ohms, however due to the absolute tolerance of implemented resistors, the feedback resistor ranged in values from 2200 to 2400 ohms. This range of values was within the tolerance that

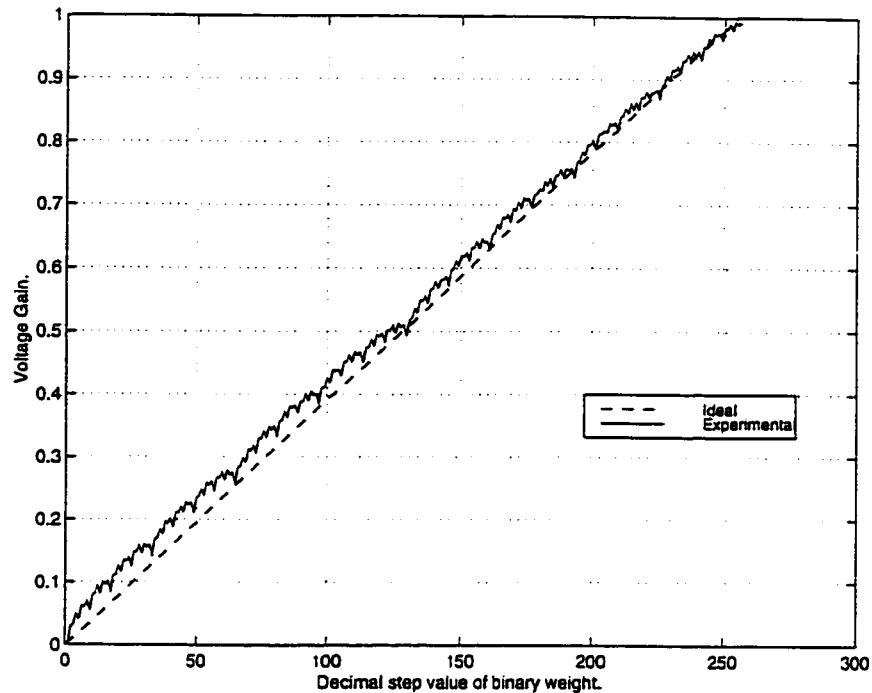


Figure 4.1: Positive weight DC behaviour of a single multiplier over the full range of 256 steps, performed on breadboard circuit.

was specified in the technology kit for the process.

Figure 4.1 shows the range of weights fed into the multiplier, and the resulting output voltage. As can be seen the output is non-monotonic, and after comparison with other chips the results were verified. A better visualization is given in Figure 4.2, which is an expanded view of the first 70 weights from Figure 4.1. This expanded view shows how the output can increase and decrease for increasing weights, however an ever-increasing output voltage is expected.

At first this might suggest that the transistor switches in the ladder may not be operating properly. In order to test this hypothesis, the ground current and feedback resistor current were measured as a single bit (switch) was toggled. As each bit is

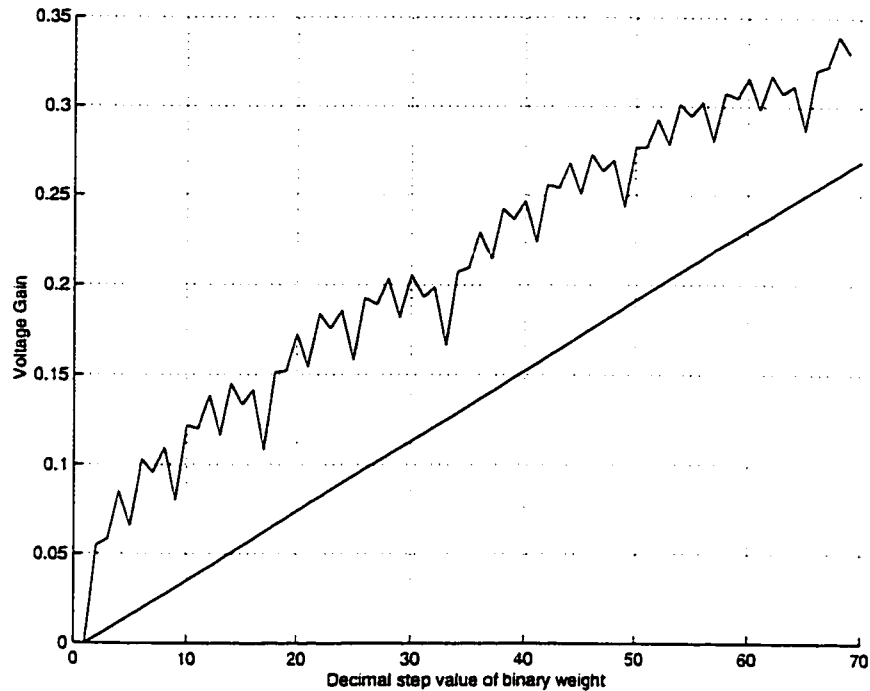


Figure 4.2: Expanded view of multiplier at lower weights.

toggled on and off for the multiplier there should be an equal change in each of these currents, thus indicating that the switches are routing the current properly. Figure 4.3 shows the currents as each bit is varied, where bit-1 is the LSB and bit-8 is the MSB. The expected change in current for the feedback resistor and the ground current were to be identical. Although the current for the feedback resistor does not match with the expected results, the curves do indicate that the appropriate switches are controlling the weight correctly.

Upon further inspection the error in the performance of the multipliers was identified to be caused by the line resistance of interconnects. When the layout for the chip was designed, since 12 multipliers were to be summed to a single pad, a common output signal line was used. This signal line was finally taken to the pad

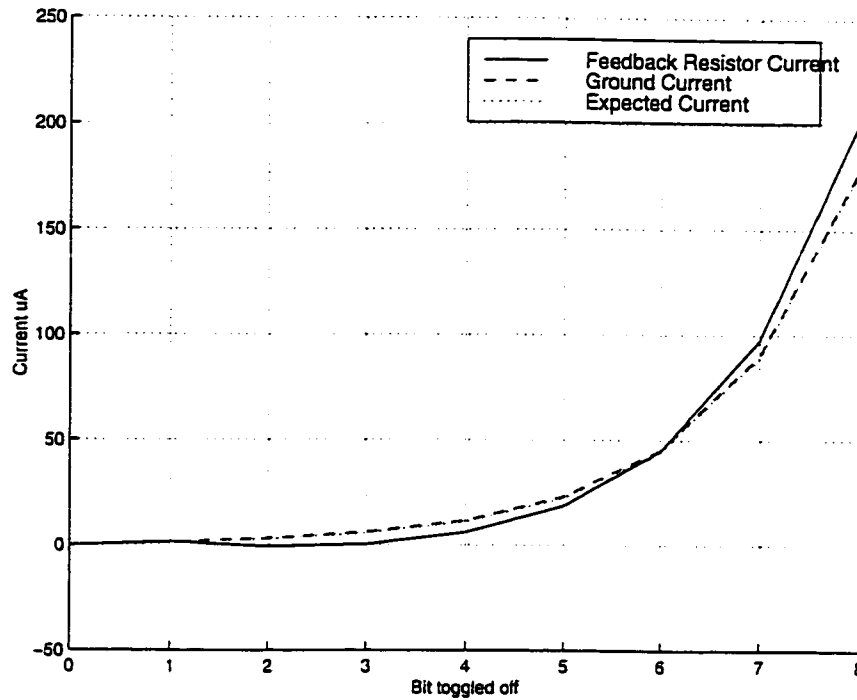


Figure 4.3: Change in current as each bit is separately toggled.

where it could be externally summed using an op-amp.

Each individual multiplier supplies a varying current, which for the designed specifications results in a maximum current of  $\pm 0.5$  mA ( $\pm 1$  V over  $2$  k $\Omega$ ). Therefore, current from all 12 multipliers will flow through the output signal line. Due to the reasonably high currents levels present, in the order of a few milliamperes, the line resistance will cause an increase in the potential along attached nodes. The attached nodes are consequently the single transistor switches in the ladder, and ideally these nodes should be attached to the virtual ground of the external op-amp.

By inspecting the layout, a calculation was made for the approximate values of line resistance. The line resistance between adjacent multipliers can attain values of approximately 3 or 4 ohms, which can cause a potential increase of a few millivolts

for each. Since the current passing through the line is also changing, due to changing multiplier weights, the non-monotonic behaviour in the output behaviour results. It should also be noted that there will be a similar problems resulting from the analog ground lines for the chip. The current passing through this line will raise the potential of nodes that are expecting the system ground.

The error in the layout could not be fixed properly without new fabrication of a multiplier chip. For testing purposes, certain elements of the chip could be examined. To minimize the error caused by line resistance effects, it was necessary to decrease the amount of current passing through both the output signal line and the analog ground line. In order to remove these currents it was required that only one multiplier for a given output summation be used. In addition, to minimize the effects of line resistance before the output pad, the multiplier closest to the output pad was utilized. However, due to the overall layout of the chip additional constraints are required.

Each of the multipliers closest to the output pad share the same analog ground line, and will therefore interfere with each other. As seen from the original diagram, Figure 1.3, input signals to the chip are used for a column of multipliers. Only one multiplier in a column can be used, and the interfering currents of the other multipliers must be directed to the output pad so that none of the currents interfere in the ground line. As well it should be noted that each given weight for the system controls two multipliers. Therefore this produces the realization that only one multiplier per chip can be used in order to minimize error.

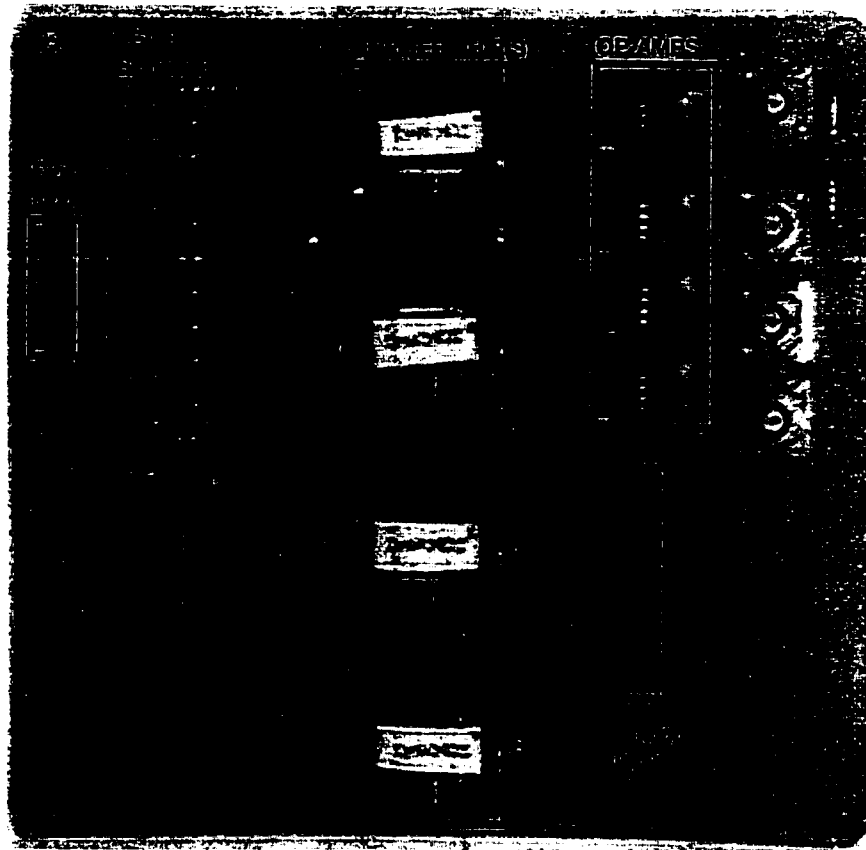


Figure 4.4: Test Board.

## 4.1 Test Board

In order to perform further testing on the multiplier chip, a printed circuit board (PCB) was constructed to allow for testing in an environment with less capacitive coupling, compared to the bread-board. The PCB shown in Figure 4.4 was developed such that multiple IC's could be used at one time. Also included on the board was space for 4 operational amplifiers, used as summers. The amplifier used to evaluate the circuit was the LM6171 High Speed Low Power Low Distortion Voltage Feedback Amplifier, produced by National Semiconductor. The selection of this device was



due to its ability to be unity-gain stable, with a Unity-Gain-Bandwidth Product of 100MHz and high slew rate of 3600 V/ $\mu$ s. Full details on the specific part can be found in the data sheets [30]. The feedback resistor value was controlled by the use of a 5 k $\Omega$  potentiometer.

The digital signals were controlled and output from the parallel port of a PC, level shifted to  $\pm 1.5V$ , and fed directly into the digital input of the multiplier chip. The software used to implement the digital interface was written in Lab Windows. For this testing, the speed was limited to a few kHz, which is due to the interface between the PC and the software designed in Lab Windows. For initial testing, this was sufficient to evaluate the accuracy of the single multipliers on the chip.

Originally multipliers from different individual IC's were to be used together to perform addition and subtraction to a single summing amplifier, if the proposed system was expanded to full capacity. However since each multiplier's resistive value ranges in absolute tolerance by approximately  $\pm 30\%$ , the feedback resistor will only be suitable for a single chip. Therefore the combination of multiple chips will produce significant error, and will not be an accurate measuring tool. For that reason, along with the errors understood from the general layout, the inclusion of the multiplier chips into the smart antenna system was not possible at this time. Therefore testing was done to mainly evaluate the design of the individual multipliers with respect to bandwidth and accuracy.

## 4.2 Multiplier Testing

In comparison to the original non-monotonic behaviour, Figure 4.5 shows the results of using a multiplier that is in close proximity to the output pad. As discussed

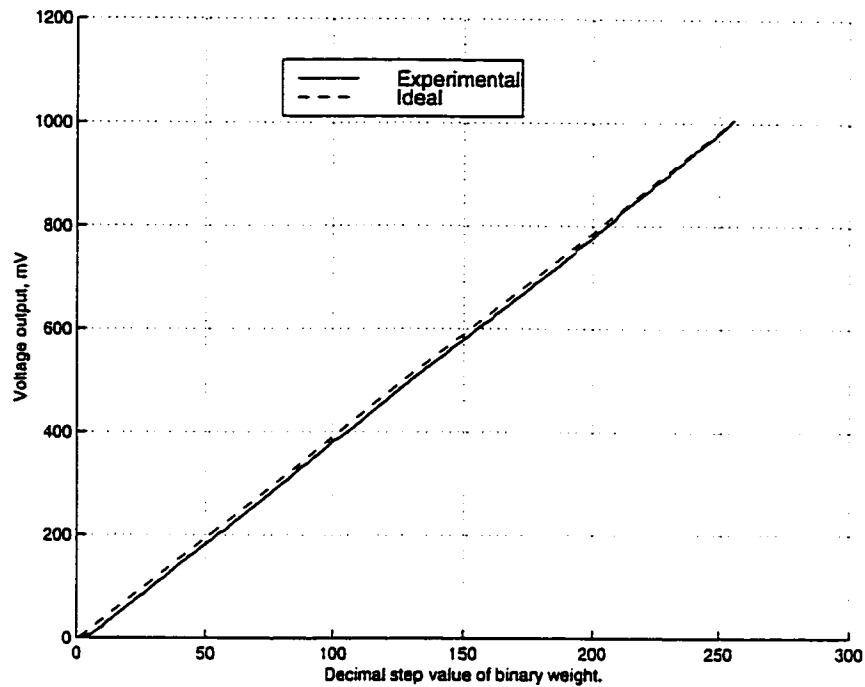


Figure 4.5: Positive weight DC behaviour of a single multiplier over the full range of 256 steps, performed on test board.

previously, measures were taken to minimize interfering current that would add to the error for the multiplier. As well, all other unused inputs were grounded. From the new characteristics of the multiplier it can be seen that the device does appear to be monotonic and linear.

In making a comparison with the expected values for the multiplier, Figure 4.6 shows the percent deviation from expected and Figure 4.7 shows the full-scale percent error which are calculated by

$$\text{Percent Deviation} = \frac{\text{Ideal} - \text{Measured}}{\text{Expected}} \times 100\% \quad (4.1)$$

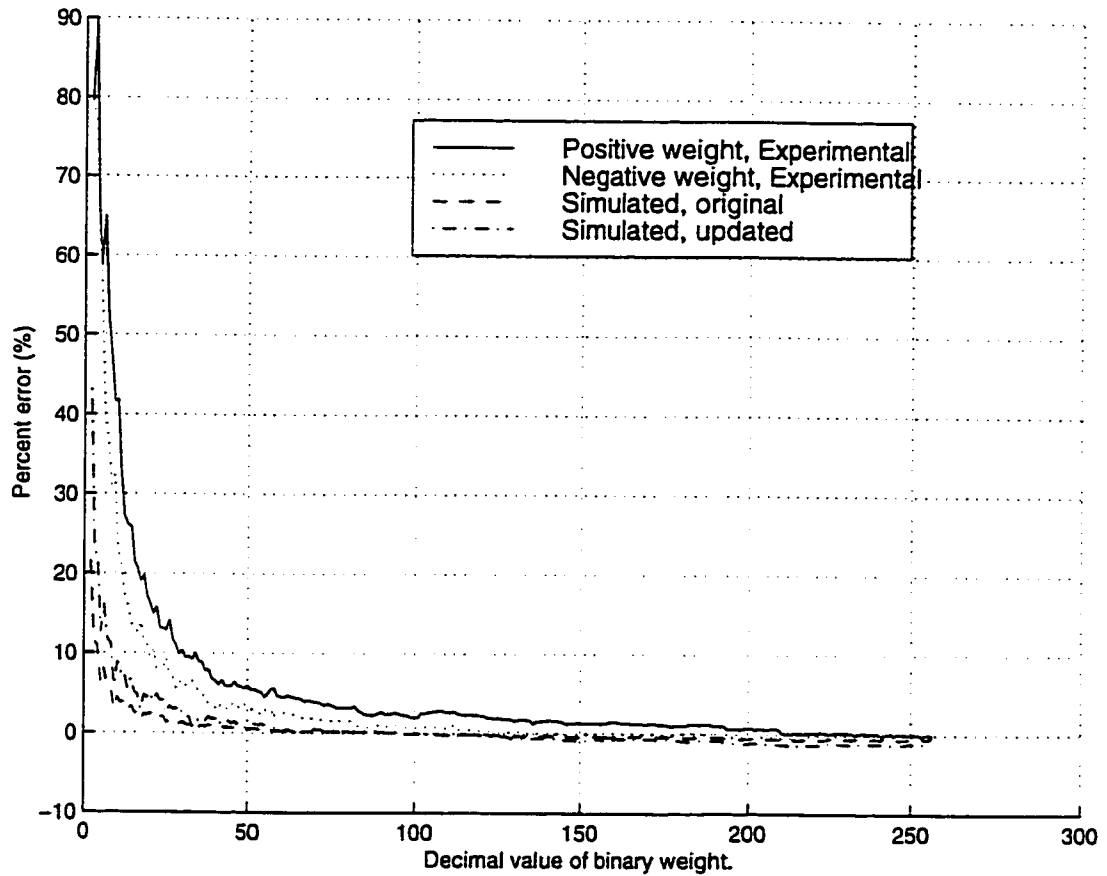


Figure 4.6: Percent deviation of multiplier measured on test board, compared with simulation HSPICE Level 28.

and

$$Full - Scale Error = \frac{Ideal - Measured}{Full Scale Value} \times 100\% \quad (4.2)$$

The large errors at the lower decimal values (binary weights) are not surprising as there will still remain a problem with the node potential being raised in the ground line due to the current being routed. As the more significant bits direct current to the op-amp the error should become less prominent, since a smaller potential change of a few millivolts is less apparent. The simulated results include line resistances in

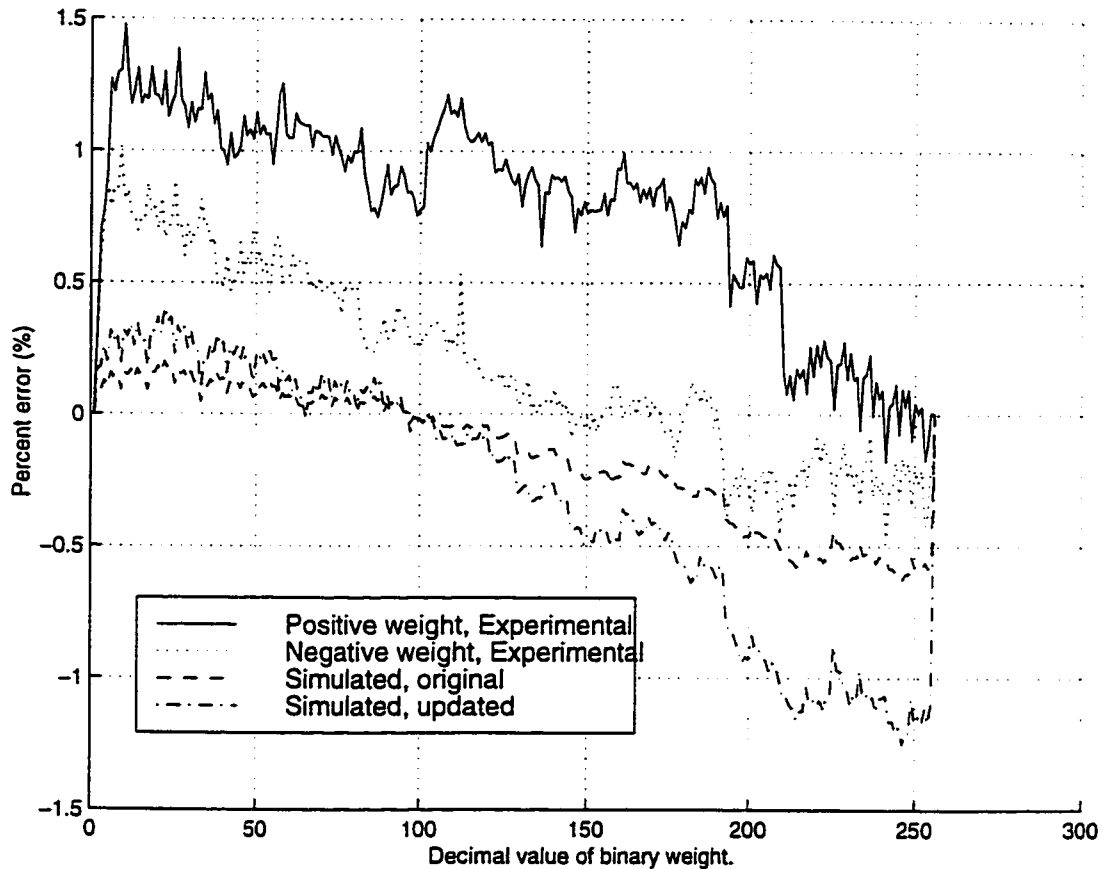


Figure 4.7: Full scale percent error of multiplier measured on test board, compared with simulation HSPICE Level 28.

the layout and indicate that the actual values in the fabricated chip are higher than expected. In a later released document for the fabrication technology, the range of sheet resistances for the various metal layers could approach two times the expected values. This would therefore increase the error, and if other contact and via resistances were included will produce a much greater error. In order to improve on the accuracy for the multipliers, the line resistance must be decreased but for testing purposes this was impossible.

Another area of interest is the bandwidth of the multipliers. Initially the mul-

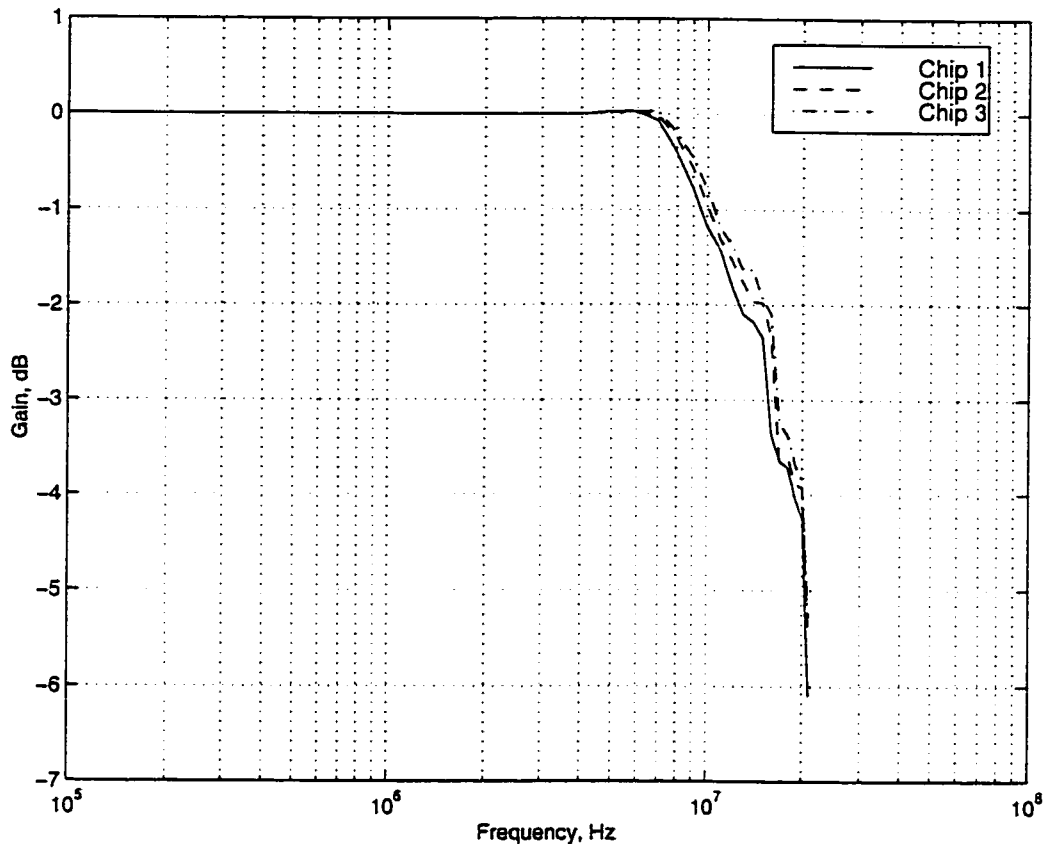


Figure 4.8: Frequency response of individual multipliers, with op-amp.

multipliers were tested with operational amplifiers included in the circuit. There was very noticeable peaking on the output, which is caused by the parasitic capacitance attached to the negative terminal of the summer, determined to be approximately 41 pF. In order to compensate for the peaking, the method as described in Appendix C was followed. By placing a small capacitance, 8 pF, in parallel with the feedback resistor the peaking was greatly reduced as shown in Figure 4.8. Initially the observed 3 dB frequency was disappointing, since a bandwidth in the hundreds of MHz was expected. By measuring the response of a square wave through a single multiplier Figure 4.9 shows the response of a 1 MHz signal without the feedback capacitor on the

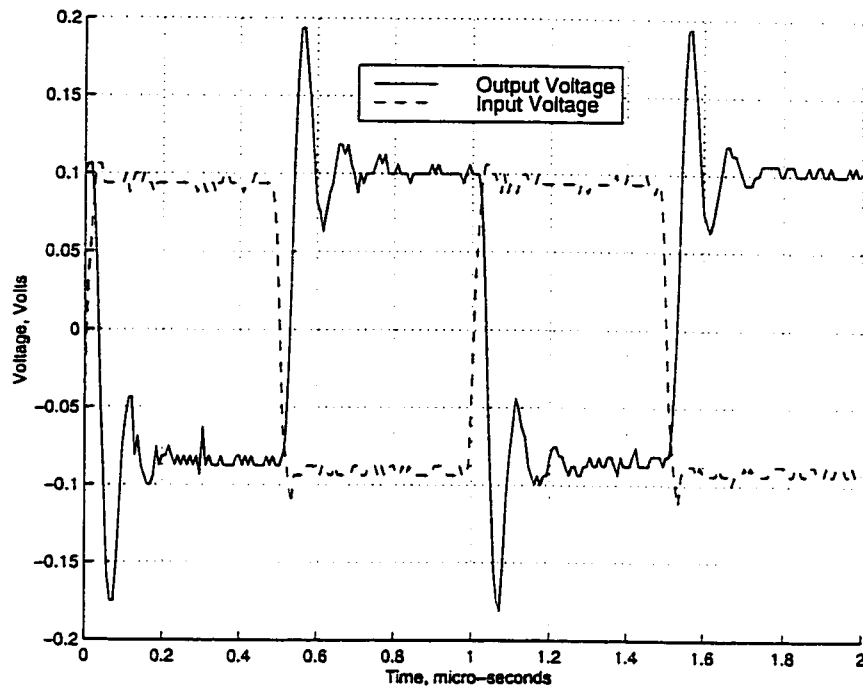


Figure 4.9: Square-wave response of multiplier with weight of -1, and 1 MHz input signal without feedback capacitor

amplifier. The noticeable ringing is removed with the addition of the 8 pF capacitor as seen in Figure 4.10. However, the system has become overdamped as is seen from the slow rising curve of the output. From the specifications of the amplifier, the performance of the amplifier is optimal with a 510 ohm feedback resistor. Therefore the 2 kohm feedback resistor required, coupled with the high input capacitance produces ringing. When the feedback resistor was reduced to approximately 500 ohms, the bandwidth of the circuit was seen to increase to 24 MHz. For that reason a simpler method to approximate the bandwidth was devised, to ensure that the bandwidth of the multipliers is not limiting the circuit.

The capacitance associated with the circuit needed to be minimized, therefore

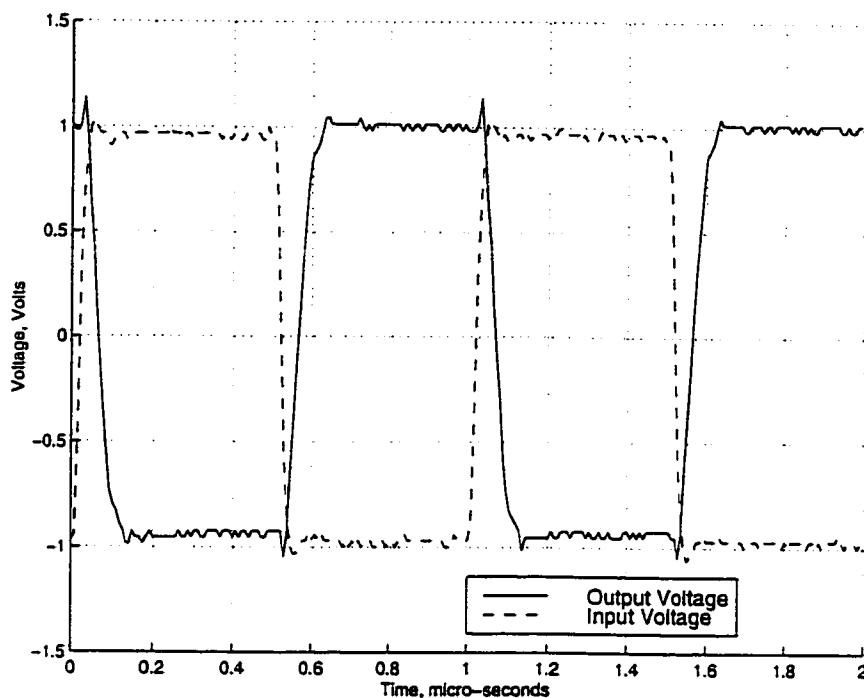


Figure 4.10: Square-wave response of multiplier with weight of -1, and 1 MHz input signal with 8 pF feedback capacitor

all sockets included in the circuit were removed. The output pin for the multiplier was probed directly without having contact with the PCB. As well, the scope probe used to measure the output was terminated with a 50 ohm resistor. This essentially created a voltage divider with the R-2R ladder and the 50 ohm load, in parallel with 15 pF from the scope probe. The measured results are shown in Figure 4.11, which shows a greatly improved frequency response. The gain of the amplifier was normalized to a gain of one, since the output at the scope probe is simply an attenuated value of the input. The test setup was also simulated in HSPICE which resulted in a 3dB frequency of 116 MHz. The simulation was set for the worst case parasitics on the diffusion resistors, which suggests that the estimate was an accurate representation. From this

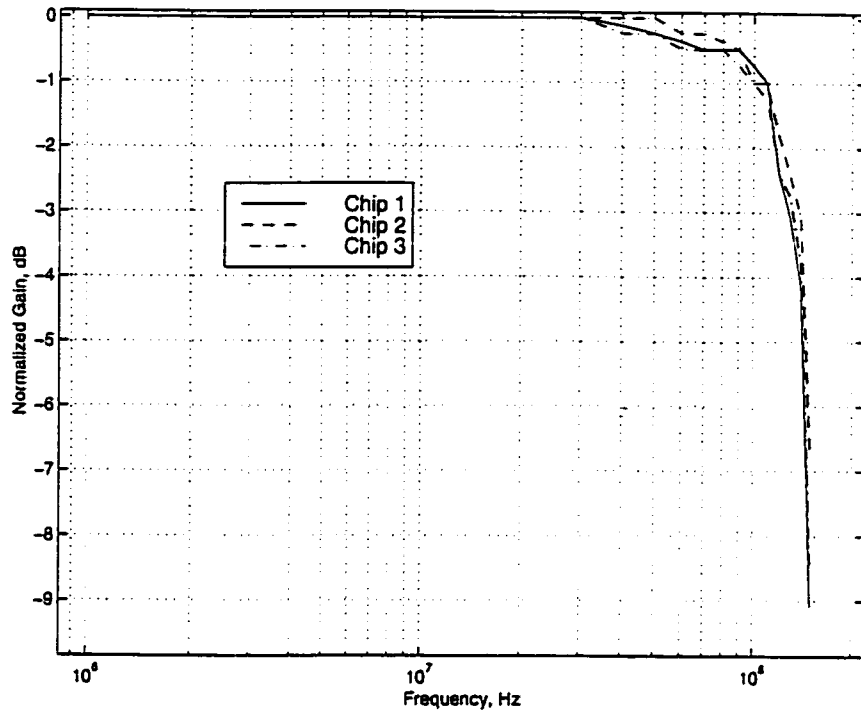


Figure 4.11: Frequency response of individual multipliers, with 50 ohm load.

frequency analysis of the multipliers it can be stated that the 3dB Bandwidth exceeds the required 20 MHz.



### 4.3 Additional testing for digital circuitry

In order to test the digital circuitry the PC and software used were not acceptable for speeds above a few kHz. At low bit-rates the weights could be varied for the full range, and at a low rates no timing issues were apparent.

To test the circuitry at higher speeds required a different method. A simple method, was to feed direct signals into the digital inputs of the chip. However, in doing so the weights of the multipliers were difficult to control and vary using a square-wave generator. For the purposes here it was sufficient to test a multiplier as the weight value varies from zero to the highest gain.

The input to the multiplier was set at a DC level of -1 V. The input clock signal and strobe signal were generated by a square-wave source and the levels were set to  $\pm 1.5V$ , with no DC offset. The digital data bits must maintain a high or low level for a single clock pulse, so it was required that the frequency of the clock signal be divided by two. This was done using a single 74HC74 D-FF [31] connected in a divide-by-two configuration. All data bits were tied to the same signal, which simply varied from a logic high or low level at half the frequency of the clock. This resulted in the shift registers receiving either a bit pattern of all zeros or all ones. When the strobe signal loaded the new weights to the multipliers, this generated a level of either ground or the highest gain for the multiplier.

The generated output signal should be of the form of a square-wave at a frequency of exactly one-half of the clock frequency. The levels of the square-wave varied from zero volts, for a multiplier weight of zero, to approximately -1 V, for the highest multiplier gain. This is due to the strobe signal being set to the same signal as the clock input, thus resulting in a continuous updating of weights.

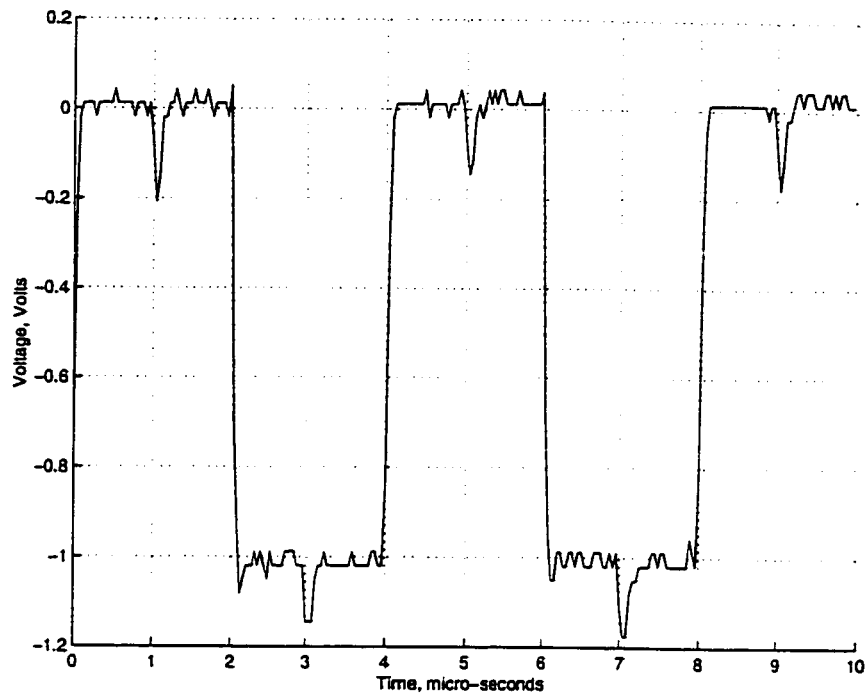


Figure 4.12: Testing of digital input at 500 kHz

Using the method described the clock was run at speeds of 500 kHz, 1 MHz and 2 MHz, and the generated output signals can be seen in Figures 4.12, 4.13 and 4.14, respectively. The generated output was tested with amplifiers in place on the test board with the feedback capacitor in place, so as to minimize ringing. The purpose of this test was to indicate the speed of the digital circuitry, so with the current setup the requirement was to notice the change at the output to the appropriate level.

Although the clock could be run at high speeds, there was noticeable clock noise in the output. As previously mentioned the fabricated chip was pad limited, and thus no separate analog and digital rails were available. In order to run the chip at the required 1MHz clock signals, separate supplies were required. In Figure 4.15 the effects of a 1 MHz clock on the chip cause spiking on the supply rails to the

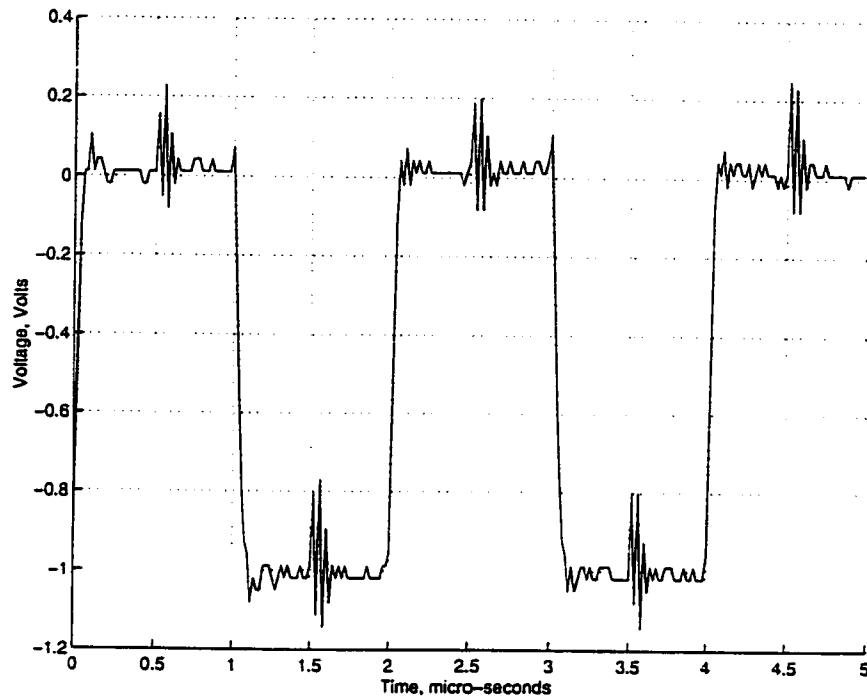


Figure 4.13: Testing of digital input at 1 MHz

chip, since there will be large transient current spikes from the switching of digital components. The speed of the digital circuitry exceeds the required limits, but with the inclusion of the apparent clock noise the error on the output was unacceptable as it began to swamp the output signal at higher frequencies.

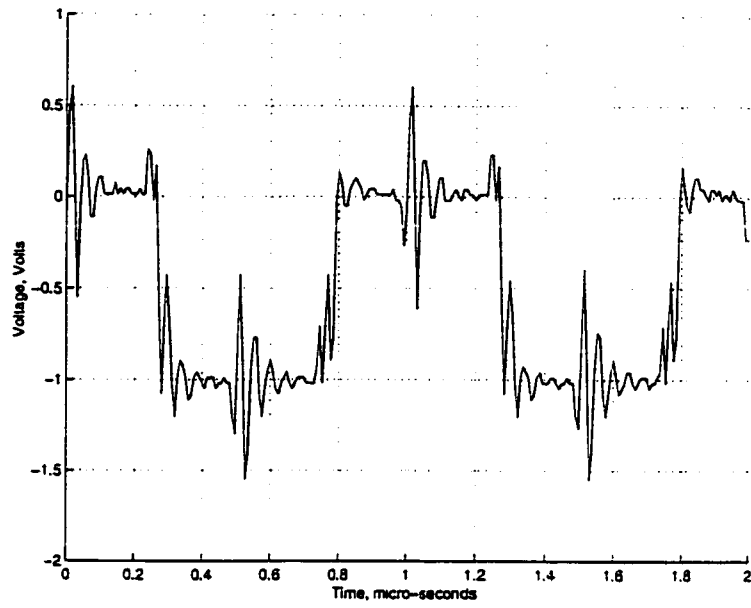


Figure 4.14: Testing of digital input at 2 MHz

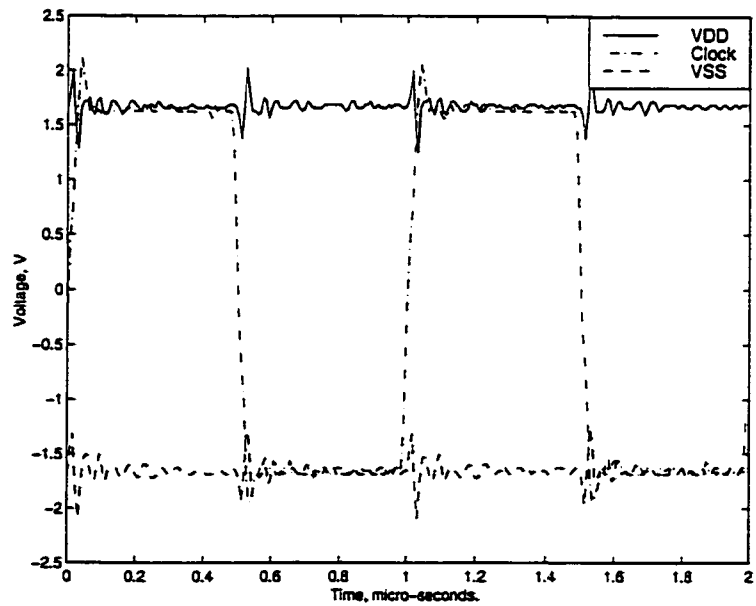


Figure 4.15: Noise on VDD and VSS due to a 1 MHz clock.

## Chapter 5

# Conclusions and Future Work

This research showed that the implementation of the analog multipliers in large quantities brings forward many issues to regarding the required levels of accuracy. All multipliers used to combine a single output signal, either I or Q, require good matching in order to provide a reasonable level of accuracy. In the R-2R ladder method of implementation, difficulties will arise due to the absolute tolerances of any type of resistor implemented. In order to maintain decent matching between multipliers to combine a single output signal, all resistors will be required to be in close proximity of each other. This grouping along with an elaborate cross-coupling scheme of resistor building blocks will allow for good matching. However for a system with 4 transmitters and 6 receiving elements, the number of multipliers required to combine a single I or Q output is 12. Using the R-2R ladder structure this requires good matching between 192 resistors of R and 2R sizes.

The individual multipliers selected were proven in simulation to meet the required specifications as outlined in Chapter 1. The bandwidth of the multiplier, with the selected size of resistors exceeds the 20 MHz bandwidth. Simulated results indi-

cate that the minimum bandwidth would be 90 MHz. The linearity and distortion levels are also within specified limits of 1%. With regards to input signals of -1V to +1V, the dual supply rails ( $\pm 1.6V$ ) selected allow for proper switching and removes concern with that regards.

## 5.1 Summary of the Multiplier Chip

Due to limitations of space in a fabrication run for the TSMC 0.35  $\mu\text{m}$  CMOS process, the initial chip layout did not allow for the best matching of resistors. The initial implementation was designed to allow for all signal processing for the above stated transmitter/receivers. This required a total of 96 multipliers on the chip, which would require a larger chip area in order to have the needed cross-coupling of devices.

With the additional difficulties rising from the line-resistances of the signal and ground lines testing was not possible to determine the accuracy of a combination of multipliers. Instead, in order to get a monotonic behaviour of the cells only a single multiplier could be tested on each separate chip. The combination of multipliers from various chips to form a single output signal was not possible, due to absolute tolerances of resistors from chip-to-chip.

Testing with the temporary fix for the single multipliers allowed the results to be measured to show the frequency response of the cells. The 3dB bandwidth measured was comparable to the expected simulated values. However, the overall accuracy with the additional line resistances was not at acceptable levels.

In order to correct the problems with the line resistances a new connection scheme will have to be performed on the overall layout. Although the resistances of the lines can be decreased by widening the paths, further steps should be taken to

minimize resistive effects. The suggested method would be that of a star configuration for the individual signal paths from each branch of the ladder structure. This will reduce the total line current in each path. In the fabricated chip this was not possible due to the amount of space that was allocated, and the required core area for the design.

Allowing for layout corrections will therefore require a larger chip area. The benefits of the added area will be two-fold, as the number of pads that can be included will also increase. This will allow for separate analog and digital supplies.

## 5.2 Further Research

From simulation the individual multipliers do meet the required specifications. However errors in the layout unfortunately limited the accuracy and the complete testing to compare matching between cells. In order to perform further testing, another test chip will be required to be fabricated with corrections to the layout. Also, it would be more feasible to reduce the number of multipliers on the chip and perform tests on a single signal output. This will greatly reduce the area required and a proper interconnect scheme can be implemented.

The initial testing of a single multiplier at higher frequencies was difficult due to the parasitic capacitances on the PCB. In order to better test the multiplier two possibilities present themselves. Firstly, a high speed test board can be made that would reduce the trace capacitances between the multiplier chip and the operational amplifiers. However, due to the errors on the multiplier chip such a board will not prove to be useful. Ideally, the summer required should be implemented on the fabricated chip.

Finally it may also be necessary to investigate further approaches for the specific multiplier cells. Due to matching concerns with the various types of resistors in the R-2R ladder, a scheme that eliminates these resistors would be preferred. In [32] a new implementation of the ladder structure is introduced, so that it is a MOSFET-only R-2R ladder. However, concern will always be present for the matching between individual components and between common multiplier cells for an output signal. Therefore in any new fabrication, additional area requirements will be mandatory to achieve excellent matching.



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## Appendix A

# Small Signal Analysis of Adjustable Current Mirror

From the original circuit for the adjustable current mirror, Figure A.1, a small-signal equivalent circuit can be drawn as shown in Figure A.2. Using this circuit it is possible to derive an expression for the small-signal current gain. It should be noted that while performing the analysis that all parasitic capacitances were retained. Once a general equation has been achieved it will be possible to make further simplifications depending on the region of operation of individual transistors. The validity of the general equation should also be noted. If the requirements dictate that the wiper of the potentiometer be taken to its extreme limits (ie.  $a = 0$  or  $1$ ) care must be taken when expressing the overall current gain. These extreme limits may cause a more general equation to become unsolvable, as will be seen.

For the small signal circuit shown in Figure A.2 each of the capacitances in

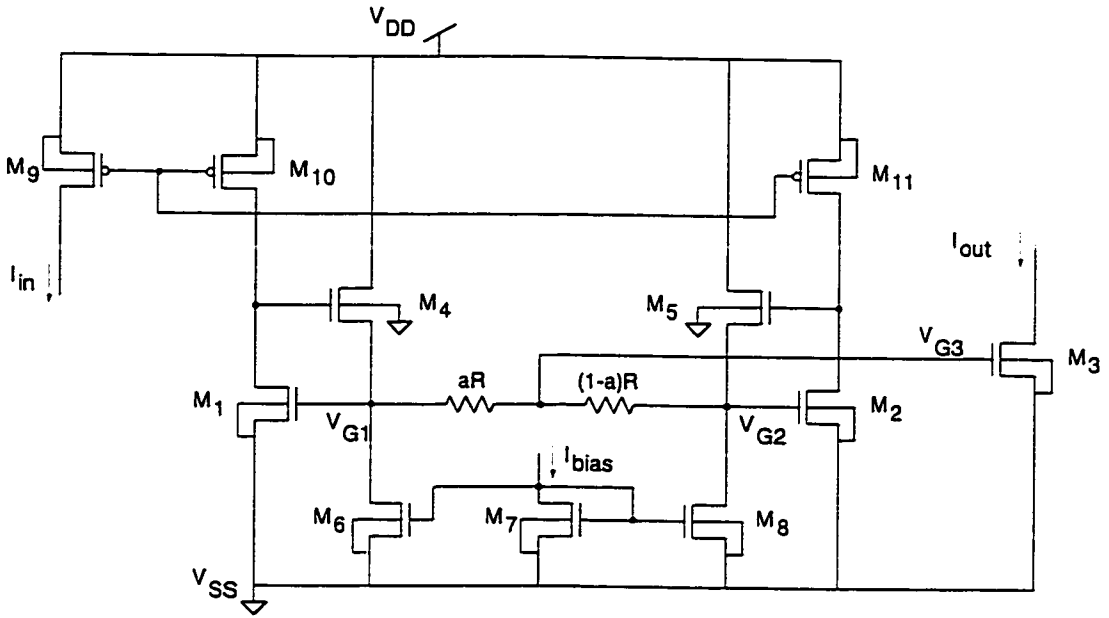


Figure A.1: Adjustable Current Mirror.

the diagram represents multiple parasitics, defined as follows:

$$C_1 = C_{gs4} + C_{gd1}$$

$$C_2 = C_{gd4} + C_{gb4} + C_{db1}$$

$$C_3 = C_{gs1} + C_{gb1} + C_{sb4}$$

$$C_4 = C_{gs3} + C_{gb3}$$

$$C_5 = C_{gs2} + C_{gb1} + C_{sb5}$$

$$C_6 = C_{gd5} + C_{gb5} + C_{db2}$$

$$C_7 = C_{gs5} + C_{gd2}$$

where subscripts g, s, d and b represent the gate, source, drain and bulk, respectively.

The analysis will be performed assuming a short-circuited output as node 6, so

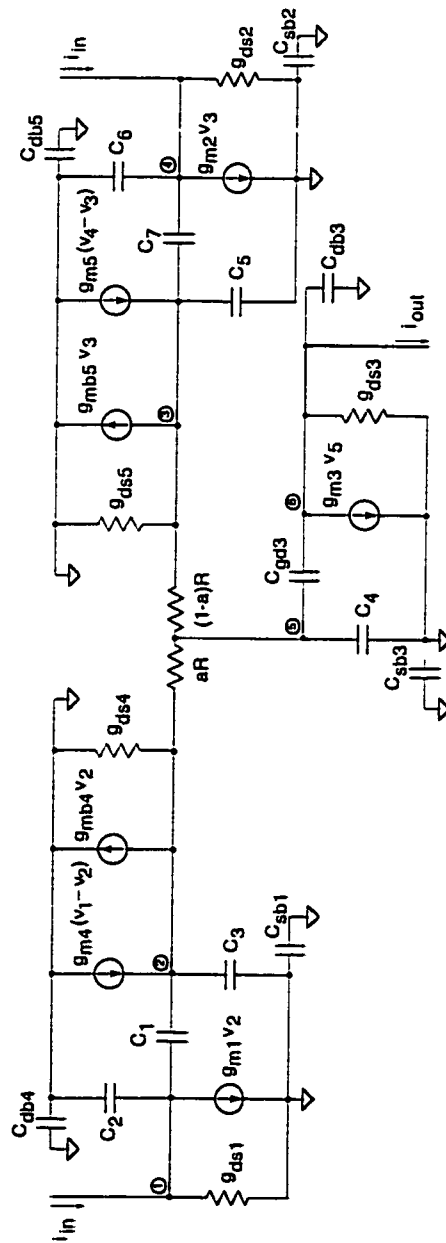


Figure A.2: Small signal equivalent circuit of adjustable current mirror.

that at node 6,

$$i_{out} = v_5 s C_{gd3} - v_5 g_{m3}$$

$$\therefore v_5 = \frac{i_{out}}{s C_{gd3} - g_{m3}} \quad (\text{A.1})$$

At node 1,

$$\begin{aligned} i_{in} &= v_1 g_{ds1} + v_2 g_{m1} + (v_1 - v_2) s C_1 + v_1 s C_2 \\ &= v_1 (g_{ds1} + s (C_1 + C_2)) + v_2 (g_{m1} - s C_1) \end{aligned}$$

$$\therefore v_1 = \frac{i_{in} + v_2 (s C_1 - g_{m1})}{g_{ds1} + s (C_1 + C_2)} \quad (\text{A.2})$$

At node2,

$$(v_2 - v_1) s C_1 + v_2 s C_3 + v_2 g_{mb4} + (v_2 - v_1) g_{m4} + v_2 g_{ds4} + \frac{v_2 - v_5}{aR} = 0$$

$$\therefore v_2 = \frac{v_1 (s C_1 + g_{m4}) + \frac{i_{out}}{aR (s C_{gd3} - g_{m3})}}{s (C_1 + C_3) + g_{mb4} + g_{m4} + g_{ds4} + \frac{1}{aR}} \quad (\text{A.3})$$

Due to symmetry, equations for  $v_3$  and  $v_4$  can likewise be found.

$$\therefore v_4 = \frac{i_{in} + v_3 (s C_7 - g_{m2})}{g_{ds2} + s (C_6 + C_7)} \quad (\text{A.4})$$

$$\therefore v_3 = \frac{v_4 (s C_7 + g_{m5}) + \frac{i_{out}}{(1-a)R (s C_{gd3} - g_{m3})}}{s (C_5 + C_7) + g_{mb5} + g_{m5} + g_{ds5} + \frac{1}{(1-a)R}} \quad (\text{A.5})$$

At node 5,

$$\frac{v_2 - v_5}{aR} + \frac{v_3 - v_5}{(1-a)R} - v_5 s (C_4 + C_{gd3}) = 0$$



$$\frac{v_2}{aR} + \frac{v_3}{(1-a)R} = i_{out} \cdot \frac{\frac{1}{aR} + \frac{1}{(1-a)R} + s(C_4 + C_{gd3})}{sC_{dg3} - g_{m3}} \quad (\text{A.6})$$

Using the above equations it is possible to show that

$$v_2 = \frac{\frac{i_{in}(sC_1 + g_{m4})}{g_{ds1} + s(C_1 + C_2)} + \frac{i_{out}}{aR(sC_{gd3} - g_{m3})}}{s(C_1 + C_3) + g_{mb4} + g_{m4} + g_{ds4} + \frac{1}{aR} + \frac{(g_{m1} - sC_1)(g_{m4} + sC_1)}{g_{ds1} + s(C_1 + C_2)}} \quad (\text{A.7})$$

$$v_3 = \frac{\frac{i_{in}(sC_7 + g_{m5})}{g_{ds2} + s(C_6 + C_7)} + \frac{i_{out}}{(1-a)R(sC_{gd3} - g_{m3})}}{s(C_5 + C_7) + g_{mb5} + g_{m5} + g_{ds5} + \frac{1}{(1-a)R} + \frac{(g_{m2} - sC_7)(g_{m5} + sC_7)}{g_{ds2} + s(C_6 + C_7)}} \quad (\text{A.8})$$

A solution for the current gain can now be found using equation A.6. However, the solution will be in a form that can not be easily simplified. For that reason only a version in polynomial form will be given here. The equation was simplified using the mathematical package MAPLE.

$$\frac{i_{out}}{i_{in}} = (C_{gd3} \cdot s - g_{m3}) \cdot \frac{N_3 \cdot s^3 + N_2 \cdot s^2 + N_1 \cdot s + N_0}{D_5 s^5 + D_4 \cdot s^4 + D_3 \cdot s^3 + D_2 \cdot s^2 + D_1 \cdot s + D_0} \quad (\text{A.9})$$

$$N_3 = aC_7(C_1(C_2 + C_3) + C_2C_3) - C_1(C_7(C_5 + C_6) + C_6C_7)(a - 1)$$

$$N_2 = (g_{m4}(C_7(C_5 + C_6) + C_5C_6)(1 - a) + C_1b_3(a - 1) - a(-g_{m5}(C_1(C_2 + C_3) + C_2C_3) + C_7a_3))$$

$$N_1 = (C_1g_{m2}g_{m5}(1 - a) + g_{m4}b_3(a - 1) + a(g_{m5}a_3 + C_7g_{m1}g_{m4}))$$

$$N_0 = (ag_{m1}g_{m4}g_{m5} + g_{m2}g_{m4}g_{m5}(1 - a))$$

$$\begin{aligned}
D_5 &= (a(1-a)(C_4 + C_{gd3})Ra_2b_2) \\
D_4 &= ((C_4 + C_{gd3})a(1-a)Ra_3b_2 + (C_4 + C_{gd3})a(1-a)Ra_2b_3 + a_2b_2) \\
D_3 &= ((C_1 + C_2)(1-a)\frac{b_2}{aR} + (C_4 + C_{gd3})a(1-a)Ra_3b_3 \\
&\quad + (C_4 + C_{gd3})a(1-a)Ra_4b_2 + a_3b_2 + (C_4 + C_{gd3})a(1-a)Ra_2b_4 + a_2b_3 \\
&\quad + a(C_6 + C_7)\frac{a_2}{(1-a)R}) \\
D_2 &= ((C_4 + C_{gd3})a(1-a)Ra_4b_3 + a_4b_2 + a_2b_4 + a_3b_3 \\
&\quad + (C_1 + C_2)(1-a)\frac{b_3}{aR} + (C_4 + C_{gd3})a(1-a)Ra_3b_4 + a(C_6 + C_7)\frac{a_3}{(1-a)R}) \\
D_1 &= (a_4b_3 + (C_4 + C_{gd3})a(1-a)Ra_4b_4 + a_3b_4 + (C_1 + C_2)(1-a)\frac{b_4}{aR} \\
&\quad + a(C_6 + C_7)\frac{a_4}{(1-a)R}) \\
D_0 &= g_{m1}g_{m2}g_{m4}g_{m5}
\end{aligned}$$

$$\begin{aligned}
a_1 &= g_{mb4} + g_{m4} + \frac{1}{aR} \\
a_2 &= -(C_1(C_2 + C_3) + C_2C_3) \\
a_3 &= -(g_{mb4} + g_{m4} + \frac{1}{aR}) \cdot (C_1 + C_2) + C_1(g_{m4} - g_{m1}) \\
a_4 &= (-g_{m1}g_{m4}) \\
b_1 &= g_{mb5} + g_{m5} + \frac{1}{(1-a)R} \\
b_2 &= -(C_7(C_5 + C_6) + C_5C_6) \\
b_3 &= (-b_1(C_6 + C_7) + C_7(g_{m5} - g_{m2})) \\
b_4 &= (-g_{m2}g_{m5})
\end{aligned}$$

Using this elaborate equation the frequency response of the adjustable current mirror was investigated. Since all parasitics were maintained in the equations the frequency response for both subthreshold and heavy inversion could be plotted. For

the purposes in this work, the equations were used to identify key aspects relating to the bandwidth of the overall circuit, and are elaborated in Chapter 2.

## Appendix B

### Harmonic Distortion

When deciding on the specific sizes for the single transistor switches it is clear from an earlier discussion that the larger the W/L ratio, the smaller the on-resistance. In order to ensure that no distortion effects will appear in the output voltage ( $V_{out}$ ) caused by a large W/L ratio, an analysis can be performed to identify such effects. In order to simplify the analysis each specific branch of the R-2R Ladder with its corresponding switch is isolated as shown in Figure B.1. Although there are a pair of switches for each branch in the ladder, only one of the two switches will be conducting at any given time. Here concern will be given to the switch which when conducting directs current to the amplifier. Using equation 2.21 the current in the isolated branch of the ladder can be expressed as:

$$I_D = \frac{-V_{out}}{R} = \frac{V_x - V_{DS}}{2R} = \beta_n \left( (V_{GS} - V_{Tn}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

where  $\beta_n = \mu_n C_{ox} \frac{W}{L}$ . From here it is possible to derive an expression for  $V_{out}$  in terms of  $V_{in}$ . Firstly an intermediate expression for  $V_{DS}$  must be found to eliminate it from

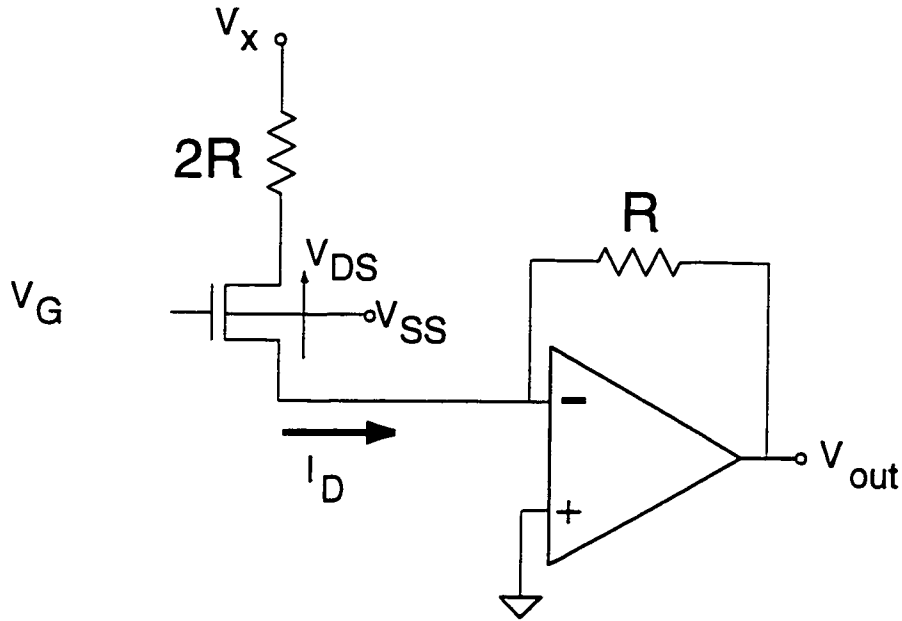


Figure B.1: Single Transistor Effect on Output.

the equation.

$$V_{DS} = \left( \frac{1}{2Rk_n} + V_{GS} - V_{Tn} \right) - \sqrt{\left( \frac{1}{2R\beta_n} + V_{GS} - V_{Tn} \right)^2 - \frac{V_x}{R\beta_n}}$$

$$\therefore V_{out} = \frac{-V_x}{2} + \frac{1}{4R\beta_n} + \frac{V_{GS} - V_T}{2} - \frac{1}{2} \sqrt{\left( \frac{1}{2R\beta_n} + V_{GS} - V_{Tn} \right)^2 - \frac{V_x}{R\beta_n}} \quad (\text{B.1})$$

In order to obtain an expression where the higher order harmonics are apparent,  $V_{out}$  must be transformed into an easily usable form. In order to obtain such an expression a Maclaurin series expansion is used, i.e.

$$V_{out} = a - \frac{1}{2}b - V_x \left( \frac{1}{2} - \frac{1}{4R\beta_n b} \right) + \frac{V_x^2}{16b^3 R^2 \beta_n^2} + \frac{3V_x^3}{96b^5 R^3 \beta_n^3} + \frac{15V_x^4}{768b^7 R^4 \beta_n^4} + \dots \quad (\text{B.2})$$

where  $a = \frac{1}{4R\beta_n} + \frac{V_{GS} - V_{Tn}}{2}$  and  $b = \frac{1}{2R\beta_n} + V_{GS} - V_{Tn}$ . Due to complexity only the

first five terms were expanded, which appears appropriate due to the powers of the factors in the denominator of the last term.

Finally  $V_{out}$  can be expressed in the following form, such that  $V_x$  is a single-tone sine wave input. This shows how higher frequency components which are integer multiples of the input frequency, enter into the equation.

$$\begin{aligned}
 V_{out} = & \frac{1}{32b^3 R^2 \beta_n^2} + \frac{45}{6144b^7 R^4 \beta_n^4} \\
 & - \left( \frac{1}{2} - \frac{1}{4R\beta_n b} - \frac{9}{384b^5 R^3 \beta_n^3} \right) \cdot \sin \theta \\
 & - \frac{1}{2} \left( \frac{1}{16b^3 R^2 \beta_n^2} + \frac{15}{768b^7 R^4 \beta_n^4} \right) \cdot \cos 2\theta \\
 & - \frac{3}{384b^5 R^3 \beta_n^3} \cdot \sin 3\theta + \frac{15}{6144b^7 R^4 \beta_n^4} \cdot \cos 4\theta + \dots \quad (B.3)
 \end{aligned}$$

Since in the above equation the term  $\beta_n$  is directly proportional to the W/L ratio, the size of the transistor can be used to decrease the distortion on the output. Therefore the benefits of having a large W/L are two-fold, producing lower on-resistance and lower distortion.

## Appendix C

# Minimizing Peaking of Amplifier Output

Since an observable peaking problem was noticed at the output when investigating a single multiplier, it was necessary to investigate the cause. In order to do so, an approximate model of the problem area is shown in Figure C.1. A general analysis will be made using resistor values of  $R_1$  and  $R_2$ . However, the value of  $R_1$  is the resistance  $R$  of the R-2R ladder, which is approximately equal to  $2k\Omega$ . In order to achieve the appropriate gain for the amplifier  $R_2$  is selected such that it has a value equal to  $R_1$ . The value of  $C_1$  is a combination of the parallel capacitance of the input to the amplifier and of the output value of the multiplier chip itself. The second capacitor,  $C_2$ , is added to the circuit in an attempt to help reduce the peaking of the output. If  $C_2$  accomplishes this goal, a suitable selection can be made by making an accurate measurement of  $R_1$ ,  $R_2$  and  $C_2$ .

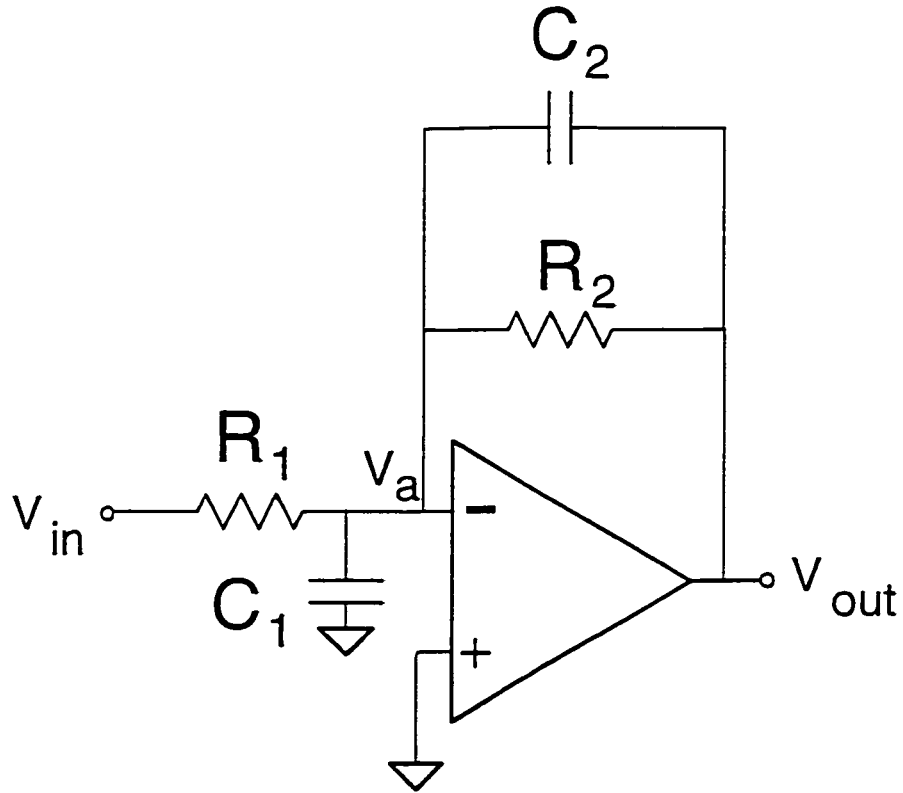


Figure C.1: Model for Peaking Analysis of Multipliers.

Summing the currents at the negative terminal of the amplifier gives,

$$\frac{v_{in} - v_a}{R} - v_a s C_1 + \frac{v_o - v_a}{R} + (v_o - v_a) s C_2 = 0$$

which when combined with

$$A \gg 1, v_o = -A v_a$$

can be simplified to the following form:

$$\frac{v_o}{v_{in}} = \frac{-1}{1 + (C_1 + A C_2) \frac{sR}{A}} \quad (C.1)$$



If the gain of the amplifier is modeled as a dominant pole transfer function, ie.

$$A = \frac{A_o}{1 + \frac{s}{\omega_\lambda}}$$

equation C.1 can be written in the form of

$$\frac{v_o}{v_{in}} = \frac{-\omega_o^2}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2}$$

where  $\omega_o$  is the pole frequency of the system, and  $Q$  is the pole quality factor [12].

The general expression equates to the following:

$$\frac{v_o}{v_{in}} = \frac{-\frac{\omega_A A_o}{C_1 R}}{s^2 + sR \left( \frac{C_1}{A_o} + C_2 \right) \frac{\omega_A A_o}{C_1 R} + \frac{\omega_A A_o}{C_1 R}} \quad (C.2)$$

$$\omega_o^2 = \frac{\omega_A A_o}{C_1 R} \quad (C.3)$$

$$\frac{\omega_o}{Q} = R \left( \frac{C_1}{A_o} + C_2 \right) \frac{\omega_A A_o}{C_1 R} \quad (C.4)$$

$$\therefore Q = \frac{1}{R \left( \frac{C_1}{A_o} + C_2 \right) \sqrt{\frac{\omega_A A_o}{C_1 R}}} \quad (C.5)$$

In order to reduce the peaking on the output the  $Q$  factor must be decreased, without modifying the value of  $\omega_o$ . From the equation for  $Q$  a simple method of eliminating the peaking is to increase the value of  $C_2$  since it is a dominant term in the denominator. Also, the value of  $C_2$  does not have any effect to the value of  $\omega_o$ . So by using a capacitor value of only a few pico-farads the peaking can be reduced. However, if too large a value is chosen the bandwidth of the amplifier will also be greatly reduced.