DESIGN METHODOLOGY AND INVESTIGATION OF GHZ RANGE CMOS RF MIXERS

by

Arif A. Siddiqi, B.Sc. E.E. (UET, Taxila, Pakistan)

A thesis submitted to the Faculty of Graduate Studies and Research

in partial fulfillment of the requirements for the degree of

Master of Engineering

Department of Electronics

Carleton University

Ottawa, Ontario, Canada

September, 2000

The information used in this thesis comes in part from the research program of Dr. T.A. Kwasniewski and his associates in the VLSI in Communications group. The research results appearing in this thesis represent an integral part of the ongoing research program. All research results in this thesis including tables, graphs and figures but excluding the narrative portions of the thesis are effectively incorporated into the research program and can be used by Dr. Kwasniewski and his associates for education and research purposes, including publication in open literature with appropriate credits. Matters of intellectual property may be pursued cooperatively with Carleton University and Dr. Kwasniewski where and when appropriate.

Abstract

This thesis presents the design methodology and implementation of CMOS RF down-conversion mixers for GHz range wireless and mobile applications. The design methodology provides an efficient and practical approach by using a simulator-based design strategy with appropriate reference to the theory. This has been done by illustrating a complete design process for a single-balanced current-switching mixer to achieve desired conversion gain, noise figure and linearity performance. Several other differential and single-ended CMOS mixer structures, based on the same design methodology have been designed and their performance has been compared with the reference single-balanced current-switching mixer. The designs have been fabricated in 0.25 μm standard CMOS technology. The comparison of designed mixers with the recent literature shows significant improvement in some of the major performance parameters. The final differential double-balanced current-switching mixer shows a conversion gain of 6.1 dB, simulated noise figure of 8.3 dB and input 1-dB compression point of -8.3 dBm, consuming 5.6 mW at 2.4 GHz input RF and 250 MHz output IF frequency.

Acknowledgements

I would like to thank my graduate supervisor Professor Tad Kwasniewski for his assistance, encouragement and patience during my thesis work. His guidance and supervision style allowed me to exercise my full potential and creativity in the thesis research.

I would also like to thank Department of Electronics, Carleton University for financial support and Canadian Microelectronics Corporation (CMC) for its technical support and fabrication facilities.

I would like to thank my fellow research group members Bill Toole, Kashif M. Sheikh and Mashkoor A. Baig for their continuous help and participation in private discussions.

Last but not least, I am deeply grateful to my parents whose kindness and understanding helped me in achieving my goals in life.

Table of Contents

List of Figures

List of Abbreviations

ASITIC . . . . . Analysis of Si Inductors and Transformers for ICs

BJT . . . . . Bipolar Junction Transistor

CMC . . . . . Canadian Microelectronics Corporation

CMOS . . . . . Complementary Metal Oxide Semiconductor

CS . . . . . Current-Switching

DB . . . . . Double-Balanced

DSP . . . . . Digital Signal Processing

FET . . . . . Field Effect Transistor

IC . . . . . Integrated Circuit

IF . . . . . Intermediate Frequency

IM . . . . . Intermodulation

IM_3 . . . . . Third-order Intermodulation

IP_3 . . . . . Third-order Intercept Point

ISM . . . . . Industrial, Scientific and Medical

LAN . . . . . Local Area Network

LNA . . . . . Low Noise Amplifier

LO . . . . . Local Oscillator

LVS . . . . . Layout vs. Schematic

NF . . . . . Noise Figure

NF_{min} . . . . . Minimum Noise Figure

P_{1dB} ..... 1-dB Compression Point

PCS ..... Personal Communication Services

PCB ..... Printed Circuit Board

RF ..... Radio Frequency

SB ..... Single-Balanced

TSMC ..... Taiwan Semiconductor Manufacturing Company

TTM ..... Time-to-Market

$\frac{W}{L}$ ..... $\frac{Width}{Length}$ of Transistor Gate

CHAPTER 1

Introduction

1.1 Introduction

With the ever increasing demand of wireless communications services, the growth of portable communication products is rising exponentially. This has resulted in severe competition among various service providers and manufacturers whose main concern is to offer low power, low cost, high mobility products and services to attract large number of consumers. These consumer based requirements have, in turn, increased pressure on RF circuit designers to explore new technologies and evolve means to satisfy both consumers and manufacturers. Different solutions have been proposed to achieve above mentioned objectives. The viable solution is to utilize such technologies that offer high degree of integration between different building blocks of a transceiver, resulting eventually in a single-chip solution. This solution will not only help in reducing power and cost of the product but also opens new ways of advancement and research interests towards efficient and innovative use of technologies. Modern cellular radio systems usually consist of two to four Integrated Circuits (IC)s with some additional passive components [3]. The back-end section, carrying Digital Signal Processing (DSP) blocks, is implemented in latest CMOS

technology, while analog front-end is realized in high performance state-of-the-art technologies like Si bipolar or GaAs MESFET to achieve high operating frequencies and speed [1]. The latest advancements in sub-micron CMOS technology has resulted in reduction of minimum channel length of the MOS device consequently increasing the unity current gain cut-off frequency to such an extent that now it is comparable to that of BJT and GaAs devices. Quite a few fully integrated CMOS transceivers for various applications have been reported in the literature targeting operating frequencies from 900 MHz to 2.4 GHz [3-7], [31]. However, with continuous scaling down of CMOS devices, the frequencies well into the upper microwave range (>10GHz) would soon be achievable [8].

1.2 Thesis Motivation and Objectives

The explosive growth of wireless services and consumption of wireless products has resulted in severe congestion in the usual 900 MHz frequency band for cellular applications. The commercially available 1900 PCS band will also soon be facing the same situation. The advent of Wireless LAN and Wireless Internet has further pushed the operating radio frequency towards 2.4 GHz, 3.5 GHz and now announced 5 - 6 GHz unlicensed frequency spectrum. These system level demands have directly been translated to RF circuit designers to evolve novel high frequency chip architectures and designs. RF down-conversion mixer, whose job is to convert high frequency signals to lower frequency spectrum where high performance digital and analog blocks (especially high Q filters) can be implemented quite efficiently, is one of the most important part of the system because its performance directly affects the overall performance of the whole front-end receiver.

The motivation behind this thesis deals with the same future trends in wireless industry by thoroughly discussing several RF CMOS down-conversion mixer architectures at 2.4 GHz Industrial, Scientific and Medical (ISM) band. The objectives are to investigate these structures on the basis of their advantages and disadvantages at GHz range frequencies and coming up with a conclusion of using specific type of configuration depending on the application and environment. The design methodology illustrated in the thesis, presents a simulator-based design cycle to characterize and optimize important performance parameters, with appropriate reference to the theory, which can be implemented successfully in newer CMOS technologies. It addresses most of the major design issues and requirements during earlier phases of design, which helps in achieving design specifications in less turn-around time, resulting in better Time-to-Market (TTM) strategy.

1.3 Thesis Organization and Outline

This thesis is organized to facilitate readers with step-by-step information involving design of CMOS mixers. Chapter 2 reviews basic transceiver architecture and RF mixers with particular emphasis on CMOS down-conversion mixers giving advantages and limitations of different configurations. Chapter 3 further elaborates CMOS mixer structures with respect to their major performance parameters. It also discusses some of the design issues that should be considered at the early stages of design to evaluate the full potential of circuits. Chapter 4 provides the simulation and measurement results of the mixers implemented in 0.25 μm CMOS technology. It also gives the performance evaluation of the designs and shows the comparison of this work with some reported CMOS mixer designs from the recent literature. It has also been shown how this design methodology

can be implemented directly in the latest available 0.18 μm CMOS technology. Chapter 5 then outlines the conclusions drawn from this thesis, while indicating the contributions of this research and explores some related future research areas.

CHAPTER 2

General Design Considerations and Issues

2.1 Introduction

In this chapter, a general introduction of front-end transceiver is presented, which explains the importance of RF down-conversion mixer in a RF system. A brief description of major performance parameters is also given to explain their effects in successfully implementing a particular circuit design as a down-conversion mixer. In the later sections, a substantial discussion has been provided for several CMOS circuit configurations which are currently used to realize a frequency mixing operation with more emphasis on their working and operation as a mixer, while elaborating their advantages, drawbacks and limitations.

2.2 *Transceiver System Architectures*

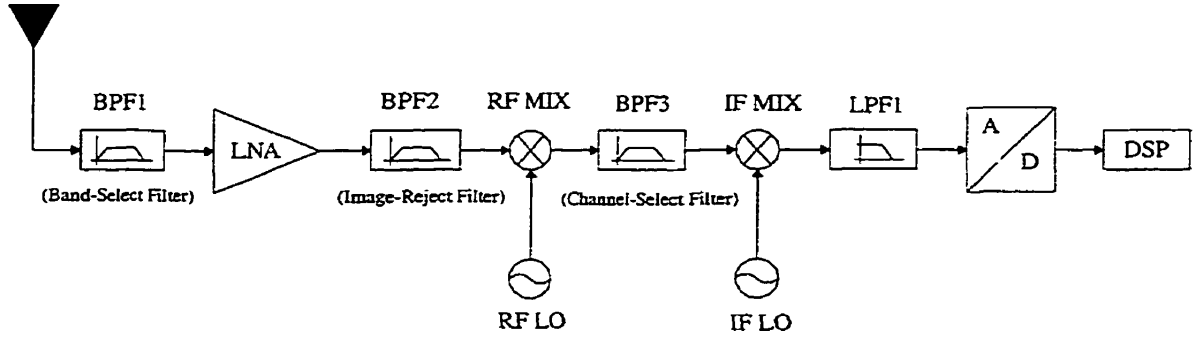

Figure 2.1: A Conventional Superheterodyne Receiver Architecture

Figure 2.1 shows a general superheterodyne receiver. The incoming signal, received by the antenna, first encounters a band-select filter where the desired band is selected and then is amplified by a low noise amplifier, followed by an image-reject filter, to filter out the image frequency. The frequency spectrum of the signal is shifted to a lower frequency, called the Intermediate Frequency (IF) by first down-conversion mixer, again filtered to obtain the desired channel and further down-converted to the baseband where it can be processed by DSP stages.

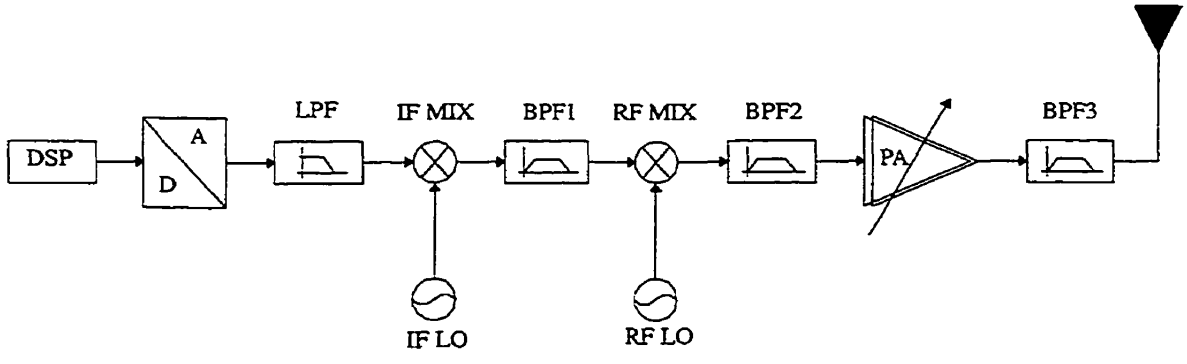

Figure 2.2: A General Transmitter Architecture

The transmitter follows the same architecture but now the signal direction is opposite to that of the received signal (Figure 2.2). Here the baseband signal is shifted to higher frequency spectrum by a couple of up-conversion mixer stages and then amplified by a power amplifier, before radiating it through Radio Frequency (RF) antenna.

2.3 *Mixer Fundamentals*

A mixer is an important building block of a radio transceiver whose function is to translate signal frequency to a higher or lower spectrum generally by the multiplication of two signals. Depending on the type of application, the input to a mixer is either Radio Frequency (RF) signal or Intermediate Frequency (IF) signal multiplied by a reference Local Oscillator (LO) signal.

Consider a general multiplication of two sinusoidal signals

$$A\cos(\omega_1 t) \times B\cos(\omega_2 t) = \frac{AB}{2}[\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t] \qquad (2.1)$$

From Equation 2.1, the multiplication of two signals together creates frequency components at the sum and difference frequencies, out of which only one is usually desired. Taking f_2 as the LO frequency, f_1 would be either RF or IF signal. If the sum frequency is desired with IF input then the mixer is termed as an up-conversion mixer, which is employed at the transmitter chain of the radio system (Figure 2.2). However, when the input RF signal with difference output signal is desired, the mixer is called a down-conversion mixer, used at the receiver section of a transceiver (Figure 2.1). Ideally, this mixer would contribute no noise, no limit to maximum amplitude, no dependence on the LO sig-

nal amplitude and would develop no intermodulation products between various RF signals. In addition, the waveform at the IF output would not contain any LO or RF components. However a real mixer will deviate from the ideal behavior on the basis of above mentioned performance parameters and the IF output can be quite complex even for a small number of signals at the input spectrum.

2.4 Typical Issues Relating RF Down-Conversion Mixers

The desired characteristics of a RF down-conversion mixer can be summarized as follows:

- low noise figure
- a moderate conversion gain for the reduction of noise contributions due to the IF and baseband amplifiers
- linearity and dynamic range
- low coupling from the LO to RF port
- suppression of LO feedthrough (leakage) to the IF port
- good matching at the RF, LO and IF ports

To get a better understanding of the issues involved while designing a down-conversion mixer, these performance parameters are elaborated below.

2.4.1 Conversion Gain and Noise Figure

The conversion gain is defined as the ratio of the amplitude of desired IF output to the amplitude of the RF input. It could be either voltage or power conversion gain. However, if the input impedance and the load impedance of the mixer are both equal to the source

impedance i.e. 50 Ω, then the voltage and the power conversion gains of the mixer are equal when expressed in dBs. Referring to Equation 2.1, the conversion gain of a simple multiplier is IF output amplitude $\frac{AB}{2}$ divided by the RF input amplitude 'A'. Hence the conversion gain is $\frac{B}{2}$ or half the LO amplitude. Assuming LO amplitude to be constant and B = 1 then the output of even a simple multiplier suffers from a conversion loss of 6 dB. Positive conversion gain is often desirable since the mixer then provides amplification along with the frequency translation. In Chapter 3, voltage conversion gain relations for different types of CMOS mixers have been derived.

Noise figure is defined as the available output noise power divided by the available input noise power due to the source expressed in dBs. It is the measure of the degradation of a signal when it passes through the circuit. Noise figure can be expressed by the following relation [9].

$$NF = 10\log\left[\frac{\frac{S_i}{N_i}}{\frac{S_iG}{N_{o(total)}}}\right]$$

Where

N_o = Output Noise

N_i = Input noise due to the Source

G = Power Gain

S_i = Input Signal Power

S_o = Output Signal Power = S_iG

$N_{o(total)} = N_{o(source)}+N_{o(added)}$

For passive devices, the noise figure is equal to the attenuation of the signal e.g. 6 dB insertion loss ideally results in 6 dB of noise figure ($N_o = N_i$ but $S_o < S_i$). For active devices, additional noise is added to this insertion loss. Noise figure for mixer tends to be considerably higher than that of amplifiers, due to fact that the noise emanating from the frequencies other than the desired RF signal can also mix down at the IF port. Also, referring to Equation 2.1, it can be observed that the output of even the simplest mixer contains two sidebands. In the usual case, where the desired signal exist only at a single sideband, the noise figure is called the Single Sideband Noise Figure (SSB-NF) and if both the sidebands contain useful information, then the noise figure is called the Double Sideband Noise Figure (DSB-NF). The SSB-NF is more specific to the receivers employing heterodyne architecture while the DSB-NF is applicable to the homodyne (direct-conversion) receivers [15].

2.4.2 Dynamic Range and Linearity

In the context of mixers, the desirable linearity would be the proportional increase in the IF output power with the increase in the RF input power. The dynamic range of the receiver largely depends on the linearity of the first down-conversion mixer [10].

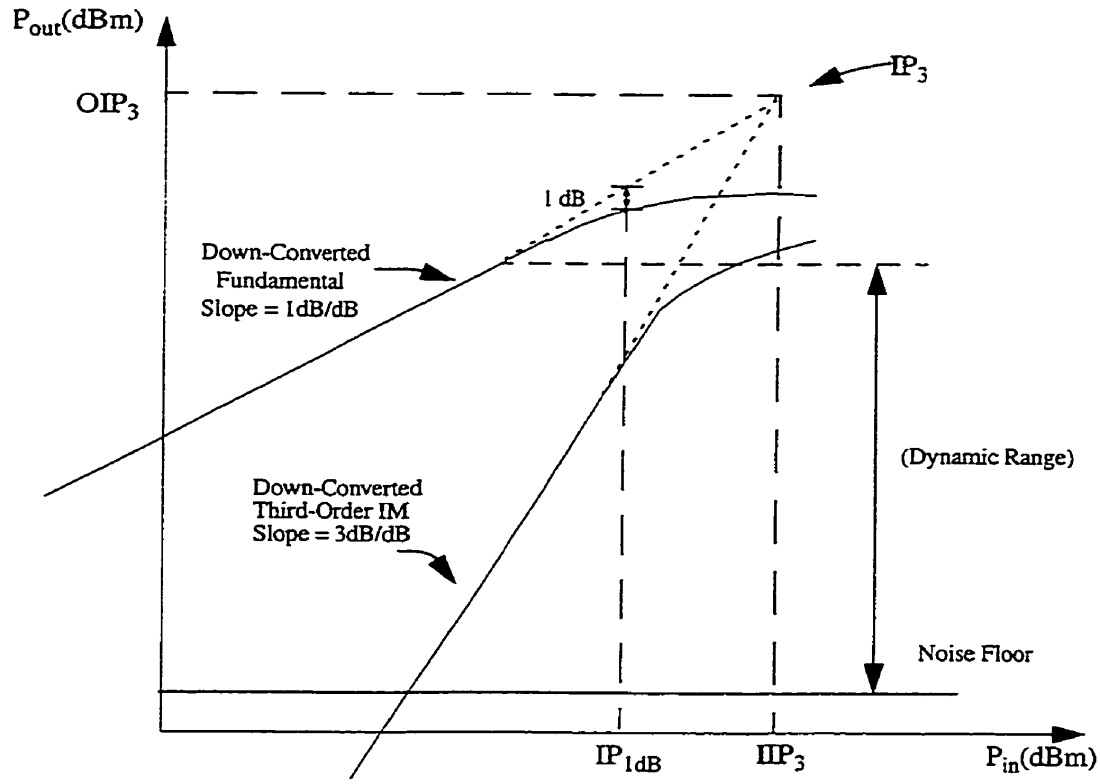

Figure 2.3: Mixer Linearity Parameters

The two-tone third-order Intercept Point (IP_3) is a measure of mixer linearity characterization. Intermodulation (IM) products occur due to the multiplication of desired input signal with a potential interferer resulting in higher order product terms in addition to the desired fundamental. Third-order Intermodulation (IM_3) products are, usually, of great concern, as they cannot be filtered out due to their close proximity with the desired IF output frequency. As a measure of the degree of departure from the linear mixer behavior, the desired output and the IM_3 output can be plotted as a function of RF input power level. The IP_3 is an extrapolated intersection of these curves as shown in Figure 2.3. In general,

the higher the IP_3, the more linear is the mixer. A high IP_3 provides a measure of protection against large adjacent interferer signals causing large signal distortion in the receiver. Referring to Figure 2.3, the non-linearity in the circuit causes the power gain to deviate from its idealized curve. The point at which the power gain is 1 dB down from the ideal linear curve is referred to as 1 dB Compression Point (P_{1dB}) and is a measure of dynamic range of a mixer. The receiver must operate several dBs below this level to avoid non-linear behavior and distortion in the output signal. Chapter 3 discusses IP_3 and P_{1dB} in detail along with the derivation of relations to determine IP_3 analytically.

2.4.3 Port-to-Port Isolation

The isolation between every two ports of a mixer is of great practical importance. Port isolation is a measure of frequency component suppression among different ports. It is generally desirable to minimize interaction among RF, IF and LO ports. Port isolation is also important in determining the amount of filtering required before and after the mixer. Since LO signal is quite large as compared to the RF signal, any LO-RF feedthrough or leakage, if not filtered out, may cause problems in the subsequent stages of the signal processing chain. In addition, large RF and LO feedthrough signals at the IF output may saturate the IF port and decrease the P_{1dB} of the mixer.

2.5 Classes of Mixers

Mixers are, generally, classified as active and passive mixers. The major difference between both classes is the amount of conversion gain they provide. Active mixers can achieve conversion gain and may require lower LO power than their passive counterparts

[10] and essentially, are transistor circuits. By virtue of their gain, active mixers reduce noise contributed by the subsequent stages of the receiver and are widely used in RF applications. Passive mixers, on the other hand, typically show conversion loss but exhibit excellent IM performance, high linearity and speed at the expense of high LO power requirements and find their applications in microwave and base station circuits [11]. Active CMOS mixers are well suited to integrated circuit design because large LO drives, besides reducing LO-RF and LO-IF isolation, are difficult to realize in low voltage and low power environments. However, passive CMOS mixers followed by gain stages, have also been reported for fully integrated CMOS transceivers [3], [7]. Being the topic of interest, the remaining discussion will be based on different topologies and configurations of active CMOS down-conversion mixers.

2.6 CMOS Mixer Design Topologies

Mixer design requires many compromises among different figures of merit such as conversion gain, LO power, linearity, noise figure, port-to-port isolation and total power dissipation. The two main techniques employed for the mixer operation are the multiplication of the input signal with a reference signal and the exploitation of mixer non-linearities. The following discussion will be based on the mixer implementation using one of these techniques.

2.6.1 Single Transistor Mixers

There are three standard modes of operation for simple single device mixers: transconductance, drain and resistive mixers [12]. The CMOS transconductance mixer operates by

applying the LO to the gate, which varies the gate-source voltage and swings the transistor between saturation and cutoff regions of operation. Maximizing the LO frequency component of the transconductance waveform optimizes the conversion gain, noise figure and linearity. There are a couple of conditions that guarantee successful mixing operation and ensure maximum transconductance. First, the transistor should be biased at the threshold voltage and operated with a transconductance waveform $g_m(t)$ having 50% duty cycle, with peak value equal to the maximum transconductance. This condition results in maximum conversion gain for the transconductance mixer [14]. In addition, drain-source voltage should ideally be kept constant and large enough to ensure that the transistor never enters the linear range of operation.

In the drain mixer , the RF signal is applied to the gate of the transistor and the mixer operates via a drain fed LO, which modulates the drain-source voltage of the device. This voltage swings the transistor between linear and saturation regions of operation. The frequency mixing occurs due to the variation in the transconductance g_m and drain-source conductance g_{ds} of the transistor.

The FET resistive mixer operates by modulating the channel resistance (resistance between drain and source) with a large LO signal while keeping the transistor in linear region of operation. The transistor channel is switched between fully depleted and fully inverted regions, thus the channel resistance is close to either infinity or a low value determined by the device dimensions [12]. No drain-source voltage or gate-source bias voltage is required to keep the FET in the linear region so the FET resistive mixer is essentially a passive mixer.

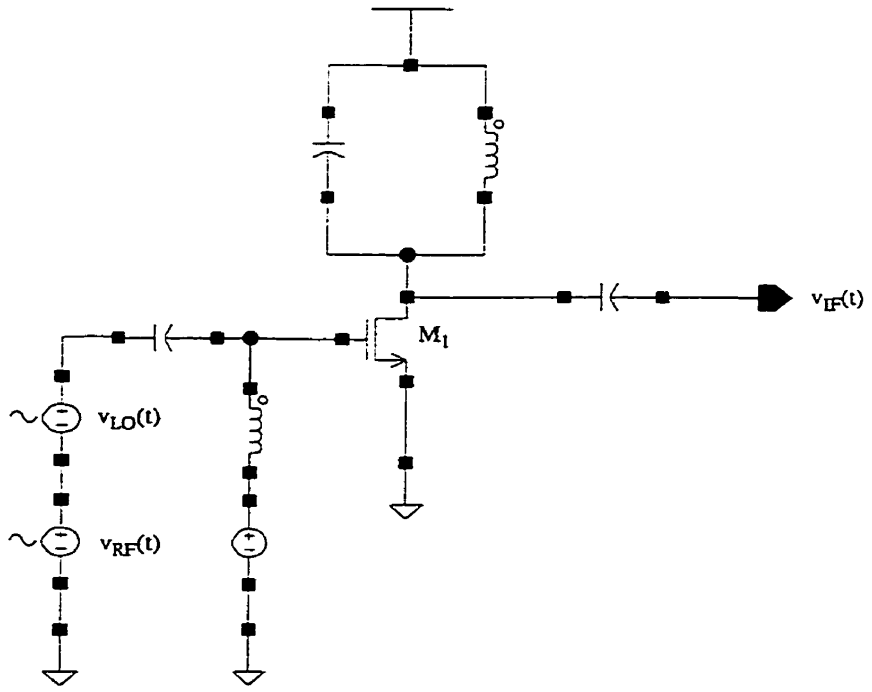

Figure 2.4: A Simple Square-Law Mixer

The most common single transistor mixer is the one that exhibits square-law behavior i.e. it makes use of only the lowest order non-linearity (squared term) and higher order non-linearities are usually undesirable. [13]. Square-law mixer can be realized with a long channel MOSFET or with any other type of non-linearity in which the quadratic term dominates. In Figure 2.4, a series combination of RF and LO signal, along with the DC bias, drive the gate of an FET. A tuned IF load is used at the drain of the device to provide an approximate short circuit for the LO component that also helps in keeping drain-source voltage constant over the entire LO cycle. The advantage of the square-law mixer is that the undesired spectral components are usually at the frequencies, quite different from the

IF frequency and can easily be removed [13]. Also, due to the single device configuration, it has a simple structure and provides good noise figure and conversion gain. The disadvantage of this structure is the poor RF-LO and LO-RF isolation, as both RF and LO signals are applied at the same port. In addition, the LO signal is amplified by the FET, which reduces LO-IF isolation. The other main disadvantage is the difficulty in matching the input at both RF and LO frequencies. In such cases, the matching is done only for the RF signal at the expense of increased LO requirements that further reduces isolation.

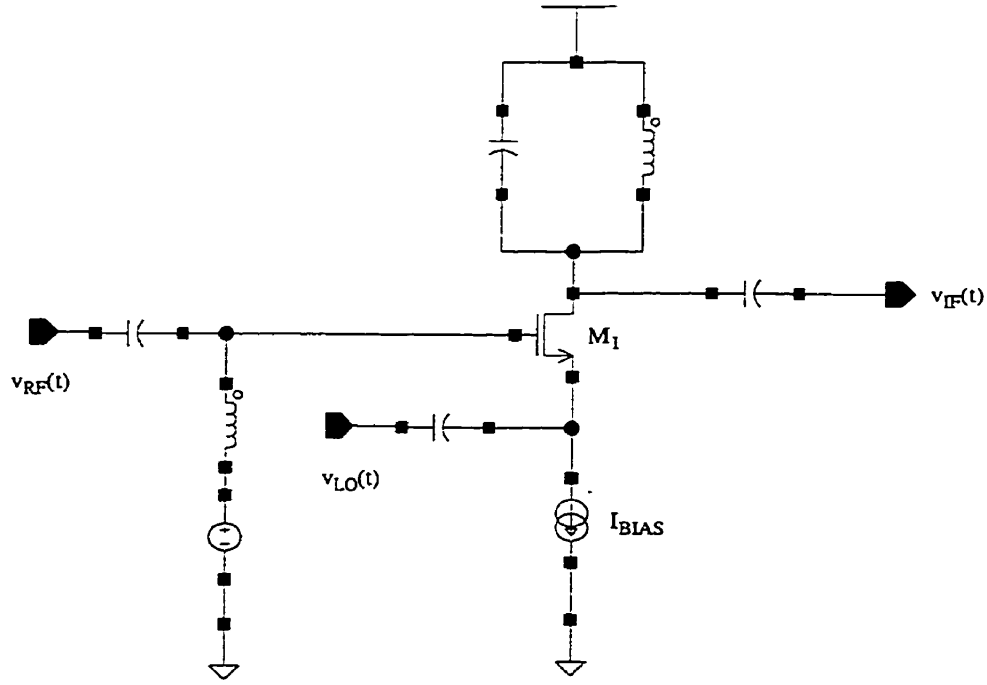

Figure 2.5: High Isolation Square-Law Mixer

An alternate structure using the same functionality is depicted in Figure 2.5. In this topology, the LO signal is applied at the source of the FET resulting in better LO-RF isolation

and lower LO power requirements due to the possibility of matching LO port at the LO frequency [13].

2.6.2 *Dual Gate Mixers*

Dual gate mixers have one major advantage over single gate mixers that the RF and LO signals can be applied to the separate gates. The dual gate device is simply a cascode connection of two single gate FETs as shown in Figure 2.6.

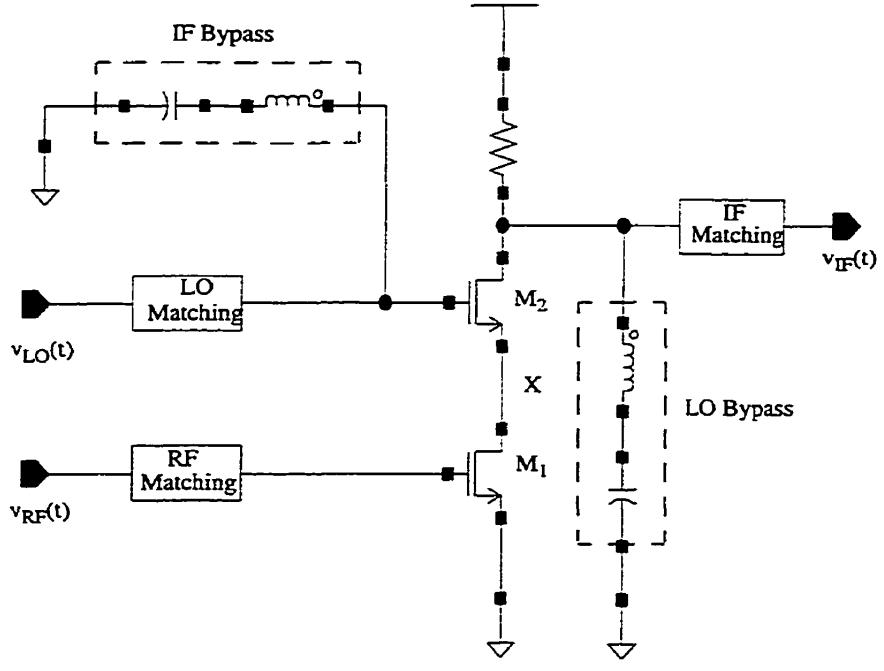

Figure 2.6: Dual-Gate Mixer with LO and IF Bypass Resonant Circuits

The second gate has several effects on the transistor operation. Its primary use is to control the small signal transconductance of the first gate device and therefore, the RF gain of the

device, making it useful as a mixer [14]. In addition, this configuration is well suited to CMOS technology since the drain and source of the two cascoded devices can be shared reducing capacitance at the common junction. The dual gate structure also has an added advantage of isolating LO and RF ports, allowing separate matching networks and providing inherent LO-RF isolation. It has been proved that the usual mode of operation is the one in which LO signal is applied to the top gate (M_2 in the Figure 2.6) and the RF signal is fed to the lower gate [12], [14], [29-30]. This not only improves the RF-IF isolation but also enhances the linearity by allowing the use of standard port matching techniques for the RF signal. The applied LO signal modulates the common node voltage (node X in Figure 2.6). The modulated node is the drain of M_1 resulting in the mixing of LO and RF signal. This type of mixing operation is similar to the operation of a single device drain mixer. The gate-source voltage of the lower transistor M_1 is approximately constant because the RF signal is usually very small and the modulated drain-source voltage swings M_1 in and out of linear and saturated regions of operation over the LO cycle. Frequency mixing occurs due to the modulated transconductance g_m and drain-source conductance g_{ds} of M_1. The upper transistor M_2 remains in current saturation over most of the LO cycle, thus, it operates, simultaneously, as a source-follower amplifier for the LO and a common-gate amplifier for the IF. This gate should be grounded at the IF harmonic, which can be done by placing a series resonant structure, tuned to IF, as shown in Figure 2.6. The drain of M_2 should also be shorted to ground at the LO frequency. This short circuit keeps the drain voltage constant and guarantees that M_2 remains in saturation over most of the time.

The disadvantages of dual gate mixer are the inevitable use of passive components for LO and IF rejection making it less useful in low frequency RFIC implementation, and reduction in conversion gain due to the possible addition of a series resistance at the source of lower transistor, to avoid instability that could occur due to the common-gate operation of LO transistor [14]. The dual gate mixer can be implemented as a double-balanced structure that increases port-to-port isolation and achieves LO short at the IF port without using passive resonant components as shown in Figure 2.7

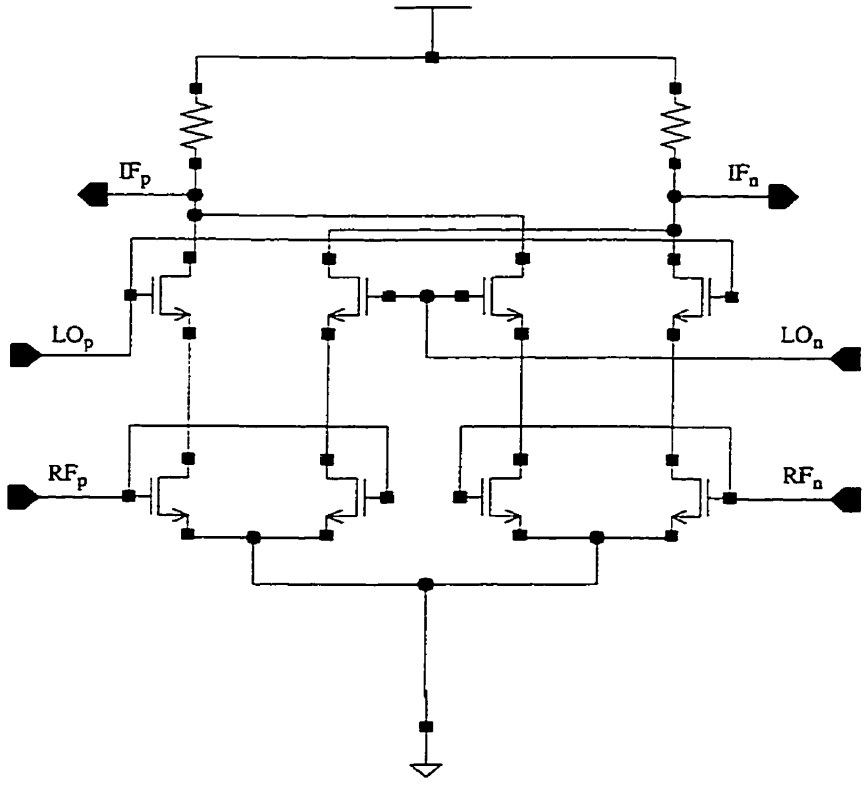

Figure 2.7: Double-Balanced Dual-Gate Mixer

2.6.3 Single-Balanced Mixers

Mixers based on the multiplication of two signals exhibit superior performance as they ideally generate only the desired mixing products. Both the RF and LO signals are applied at different ports resulting in high degree of inherent isolation among all the three ports. Down-conversion mixers usually employ LO short at the IF port, as discussed earlier, to achieve optimum IM performance. The LO short is practically important for the active mixers because LO signal is typically larger than the RF signal and it is further amplified by the active devices. The mixer that accommodates a differential LO signal and a single-ended RF signal is termed as single-balanced mixer (Figure 2.8)

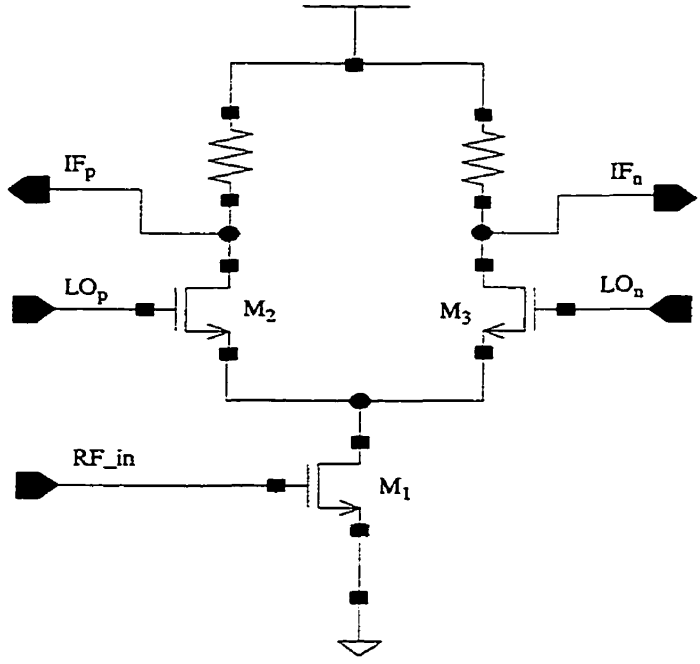

Figure 2.8: Single-Balanced Mixer

In Figure 2.8, the incoming RF voltage signal is first converted into a current signal and then multiplied in current domain. The FETs M_2 and M_3 are biased slightly above their threshold level. This results in the LO alternatively switching M_2 and M_3 on and off. Consequently, one LO transistor is always on, while other LO transistor is ideally off, keeping the RF transistor in saturation. Hence, the LO signal can be considered as a square wave consisting of odd harmonics of the LO frequency. The magnitude of this signal should be large enough to ensure complete switching of the differential LO transistors. The RF input current signal is multiplied by the odd-order harmonics of LO signal, resulting in mixing products to appear at the output IF port. The analytical description to derive a first order relation of the voltage conversion gain is given in Chapter 3.

The major disadvantage of the single-balanced mixer is the presence of LO components at the output port and will be discussed in detail in Section 3.2.1. The amplification of the LO signal by the active devices further aggravates the situation. Since the mixer is usually followed by an amplifier, filtering may be required to prevent saturation of the amplifier by suppressing LO portion of the output signal.

2.6.4 Double-Balanced Mixer

Two single-balanced mixers can be combined to form a double-balanced mixer. Both RF and LO inputs of the mixer are now differential. The active double-balanced current-switching mixer is also termed as Gilbert cell mixer as shown in Figure 2.9.

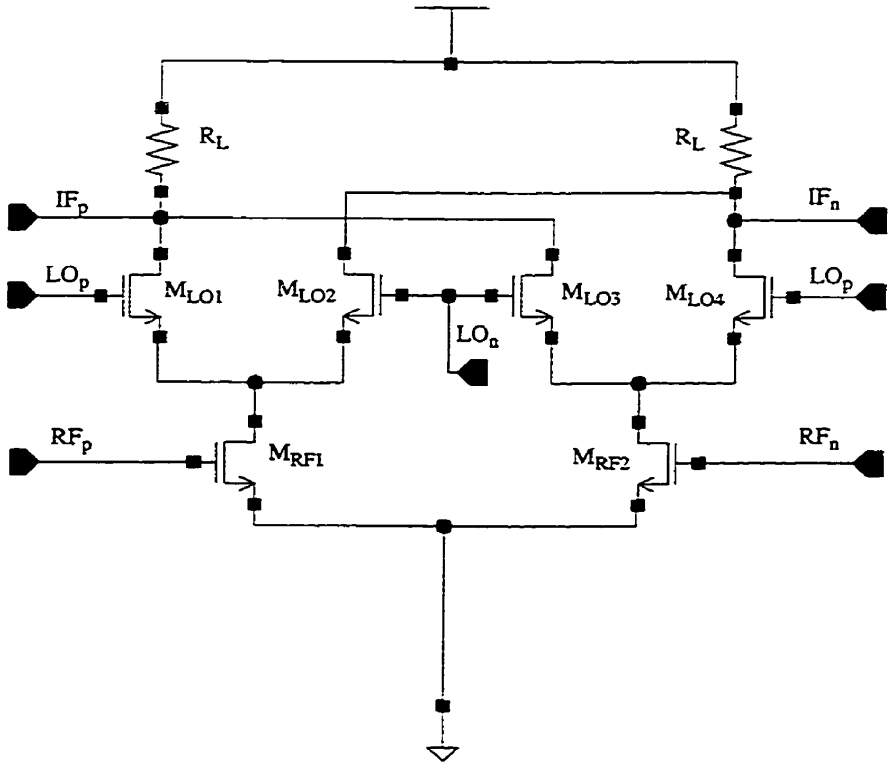

Figure 2.9: CMOS Double-Balanced Gilbert Cell Mixer

The LO drive should be large enough to make the differential pair act like current-steering switches. The two single-balanced mixers are connected in anti-parallel as far as LO signal is concerned but in parallel for RF signal, therefore, the LO terms are cancelled at the output port. In addition, the interconnection of the outputs causes the drain of the LO quad transistors to act as a virtual ground not only for LO and RF frequencies but also for the even-order spurious frequencies [14]. Hence, no special circuitry is required to provide RF and LO short at the drain of LO quad. Consequently, this mixer provides a high degree of LO-IF isolation easing filtering requirements at the proceeding receiver stages. The major

drawback of double-balanced mixer is the higher power consumption, because of twice the number of devices as compared to a single-balanced mixer and also due to the fact that all the active devices should remain in saturation region of operation and a current source is often necessary for proper biasing. Moreover, mismatches between different devices and signal path lengths limit port-to-port isolation and cancellation of the harmonics at the output IF port.

2.7 Summary

A fully integrated single-chip transceiver offers several advantages in terms of reducing size and power consumption of the portable radios. For many semiconductor manufacturers, this single-chip transceiver is particularly important if it is designed and fabricated in the same standard CMOS technology that they use for their other IC products. A single-chip CMOS transceiver requires the exploration of new systems and circuit design topologies to facilitate the highest level of receiver and transmitter integration. The continuing scaling-down of the CMOS transistor gate length is improving CMOS technology's RF performance. Using CMOS technology, RF designers can utilize the large infrastructure already in place that supports and develops low cost, mass production and high yield ICs. Being an important building block of the monolithic CMOS transceiver, a CMOS RF mixer allows a considerable increase in transceiver integration and a reduction in its cost. Several types of CMOS mixers were discussed, each having some advantages and disadvantages. Although, single device and dual gate mixers exhibit better conversion gain and noise figure performance, they are not well suited in highly integrated design due to their low isolation and high filtering requirements. Single-balanced CMOS mixers also need

some type of filtering due to the presence of LO harmonics at their output. Double-balanced CMOS mixers possess inherent port-to-port isolation and have better linearity making them a serious contender for integrated circuit design. Using proper biasing conditions, they can operate at lower LO power requirements, thus relieving pressure from some of the other building blocks of the transceiver. In addition, the operation and design methodology of double-balanced mixers (especially Gilbert mixer) is well understood that allows the possibilities of implementing innovations during design process to make them more efficient at higher frequencies. However, as RF applications are moving towards higher frequencies e.g. the recently opened 5 - 6 GHz frequency spectrum for unlicensed high-speed Internet access and data transmission, the implementation of small sized passive components will become a reality which could be used for LO rejection in CMOS dual gate mixers.

CHAPTER 3

Design Techniques and Performance Parameters

3.1 Introduction

In the previous chapter, a general overview of a front-end transceiver architecture was given, which explained the importance of RF down-conversion mixer, in evaluating the overall performance parameters of whole front-end receiver section of the transceiver.

The RF down-conversion mixer, which is the focus of this thesis, is an important building block in a receiver because its performance affects the overall performance of the receiver and performance requirements of the adjacent building blocks. For instance, a mixer needing low LO power will help in reducing total power consumption of the receiver and result in relaxed filtering requirements after the mixer stage due to greater LO-IF isolation. Also, low noise figure and high conversion gain mixer will help in reducing gain requirements from the preceding LNA stage and overcome the noise contributions due to the subsequent IF stages. In this chapter, some of the performance parameters in context of CMOS RF mixers, will be discussed, addressing certain design issues for different topologies and configurations.

3.2 Voltage Conversion Gain of CMOS Mixers

As discussed in Chapter 2, active mixers can provide conversion gain and offer a high degree of isolation depending on the configuration. In this section, voltage conversion gain of certain CMOS mixer topologies and structures will be discussed in detail, with emphasis on deriving a first-order conversion gain relation. This relation. although neglects parasitics, still gives a good foundation to analyze the effects of device transconductance and output load on the conversion gain of a mixer. This information will be used in Chapter 4 to optimize the mixer designs.

3.2.1 Single-Balanced Current-Switching Mixer

Consider a single-balanced CMOS mixer, with resistive load R_L as shown in Figure 3.1.

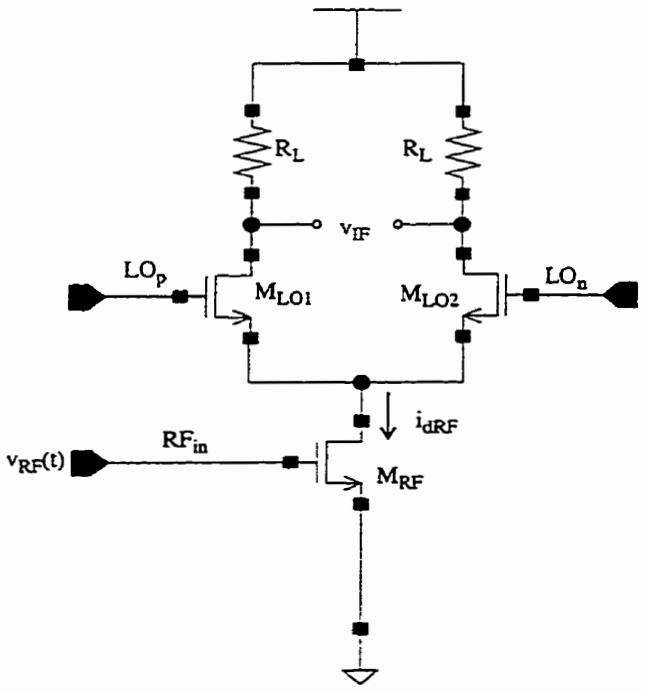

Figure 3.1: Single-Balanced Current-Switching Mixer

If the switching LO signal is given by an ideal square wave LO(t) with an amplitude of ±1, to achieve an instantaneous switching action, then it can be represented by its Fourier series equivalent as shown in the Equation 3.1

$$LO(t) = \frac{4}{\pi}\sum_{k=1}^{\infty}\left[\frac{\sin\left(\frac{k\pi}{2}\right)}{k}\cos(k\omega_{LO}t)\right] \tag{3.1}$$

Note that, although this equation represents the LO voltage, still is a dimensionless quantity because it only shows the switching of the LO transistors. This switching action turns LO transistors on and off with the application of positive and negative peaks of the perfect square wave (i.e. for the positive peak, M_{LO1} is on and M_{LO2} is off and for the negative peak, M_{LO2} is on and M_{LO1} is off). Therefore, the RF transistor remains in the saturation region of operation and the output current flows through the load resistors at all times

Equation 3.1 can be expanded as

$$LO(t) = \frac{4}{\pi}\left[\cos(\omega_{LO}t) - \frac{1}{3}\cos(3\omega_{LO}t) + \frac{1}{5}\cos(5\omega_{LO}t).....\right] \tag{3.2}$$

Figure 3.2 shows the switching action of single-balanced current-switching mixer.

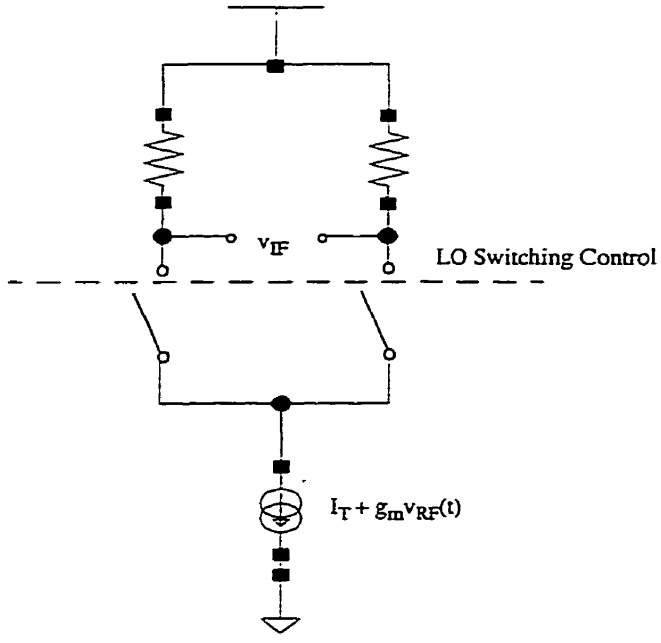

Figure 3.2: The LO Switching Action in Single-Balanced CS Mixer

The RF transistor is modeled by:

$$i_{dRF}(t) = I_T + g_m v_{RF}(t) \tag{3.3}$$

where I_T is the DC tail current.

Taking $v_{RF}(t)$ as a sinusoidal signal

$$v_{RF}(t) = V_{RF}\cos(\omega_{RF}t)$$

The mixer current-switching action can now be expressed by combining Equations 3.2 and 3.3

$$i_o(t) = (I_T + g_m V_{RF}\cos(\omega_{RF}t))\left[\frac{4}{\pi}\left(\cos(\omega_{LO}t) - \frac{1}{3}\cos(3\omega_{LO}t) + \frac{1}{5}\cos(5\omega_{LO}t) - \ldots\ldots\right)\right] \quad (3.4)$$

Rearranging

$$i_o(t) = \frac{4}{\pi}\left(I_T\cos(\omega_{LO}t) - \frac{1}{3}I_T\cos(3\omega_{LO}t) + \ldots\ldots\right)$$

$$+\left(\frac{4}{\pi}g_m V_{RF}\cos(\omega_{RF}t)\cos(\omega_{LO}t)\right.$$

$$\left.-\frac{4}{3\pi}g_m V_{RF}\cos(\omega_{RF}t)\cos(3\omega_{LO}t) + \ldots\ldots\right) \quad (3.5)$$

Equation 3.5, after neglecting higher order harmonics, can further be simplified as

$$i_o(t) = \frac{4}{\pi}\left(I_T\cos(\omega_{LO}t) - \frac{1}{3}I_T\cos(3\omega_{LO}t) + \ldots\ldots\right)$$

$$+\frac{2}{\pi}g_m V_{RF}[\cos(\omega_{RF} - \omega_{LO})t + \cos(\omega_{RF} + \omega_{LO})t] \quad (3.6)$$

In Equation 3.6, the second term in square brackets is the actual mixing term, where we have both the down-converted and up-converted side-bands present simultaneously. By filtering out the up-converted frequency, we remain with the following useful expression

$$i_o(t) = \frac{4}{\pi}\left(I_T\cos(\omega_{LO}t) - \frac{1}{3}I_T\cos(3\omega_{LO}t) + \ldots\ldots\right)$$

$$+\frac{2}{\pi}g_m V_{RF}[\cos(\omega_{RF} - \omega_{LO})t] \quad (3.7)$$

The output load, as shown in Figure 3.1, is R_L, therefore output IF voltage is given by

$$v_{IF}(t) = \frac{4}{\pi}R_L\left(I_T\cos(\omega_{LO}t) - \frac{1}{3}I_T\cos(3\omega_{LO}t) + ...\right)$$

$$+\frac{2}{\pi}g_m R_L V_{RF}[\cos(\omega_{IF})t] \qquad (3.8)$$

where $\omega_{IF} = \omega_{RF} - \omega_{LO}$ is the fundamental down-converted frequency. Equation 3.8 is specific to single-balanced mixer where the first term gives the LO leakage or feedthrough at the IF output.

We can calculate the voltage conversion gain of the single-balanced mixer as output IF amplitude divided by the input RF amplitude i.e.

$$G_v = \frac{V_{IF}}{V_{RF}} = \frac{2}{\pi}g_m R_L \qquad (3.9)$$

Equation 3.8 is true only for a single-balanced structure when output is taken differentially.

If the output is single-ended then the DC component in the LO signal is not cancelled at the output and gets multiplied with the input RF signal resulting in RF feedthrough at the output, in addition to the inherent LO feedthrough [15]. The LO signal, in this case, only switches between 0 and +1, instead of -1 and +1 as shown in Figure 3.3 [11].

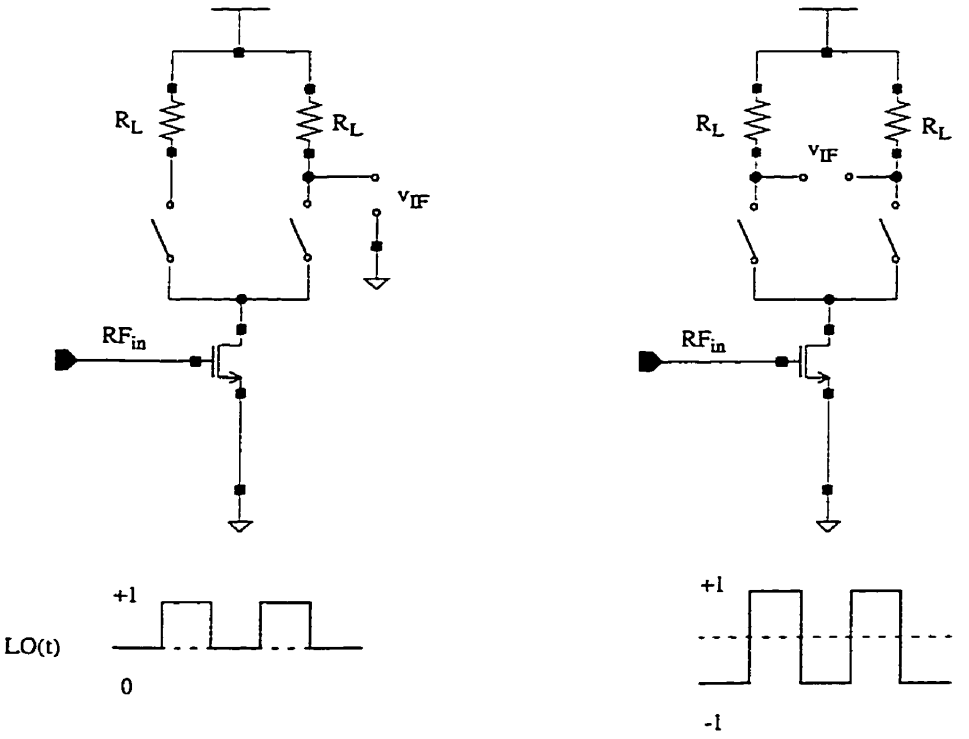

Figure 3.3: The LO Switching for Single-Ended and Differential Output

Therefore, LO(t) is given by

$$LO(t) = \frac{1}{2} + \frac{4}{\pi}\left[\cos(\omega_{LO}t) - \frac{1}{3}\cos(3\omega_{LO}t) + \frac{1}{5}\cos(5\omega_{LO}t).....\right] \qquad (3.10)$$

Output current, in this case, is

$$i_o(t) = (I_T + g_m V_{RF}\cos(\omega_{RF}t))\left[\frac{1}{2} + \frac{4}{\pi}\left(\cos(\omega_{LO}t) - \frac{1}{3}\cos(3\omega_{LO}t)...\right)\right] \qquad (3.11)$$

Now as output is single-ended, the output voltage swing is from +1 to 0, instead of +1 to -1, therefore, the output voltage magnitude will be half of the differential output voltage, and output IF voltage will effectively be divided by 2. In terms of dB, the output voltage will be 6 dB less than the differential output IF voltage

$$v_{IF}(t) = \frac{1}{4}(g_m R_L V_{RF}\cos(\omega_{RF}t)) + \frac{2}{\pi}R_L\left(I_T\cos(\omega_{LO}t) - \frac{1}{3}I_T\cos(3\omega_{LO}t) + ...\right)$$

$$+\frac{1}{\pi}g_m R_L V_{RF}[\cos(\omega_{IF})t] \qquad (3.12)$$

As expected, we see a strong RF feedthrough term in addition to the LO feedthrough and required down-converted term. Therefore, if single-ended output is taken in a single-balanced mixer, the LO and RF feedthrough would not be suppressed at the IF output port. However, only LO feedthrough is present at the output of a single-balanced mixer if output is taken differentially due to the cancellation of DC term present in the LO signal at the IF port.

3.2.2 Double-Balanced Current-Switching Mixer

The analysis discussed in Section 3.2.1 for single-balanced CMOS mixer can directly be applied to a double-balanced mixer as the double-balanced structure is just a combination of two single-balanced structures connected in parallel i.e. 180° out of phase for the LO signal while in-phase for the RF signal. Hence, LO signal feedthrough at the IF output is ideally suppressed completely as output port acts as a virtual AC ground for LO signal. In addition, all even-order harmonics of the mixed output are cancelled out, resulting in bet-

ter 1-dB compression and third-order intermodulation intercept point, consequently better dynamic range and linearity response. The only drawback is that being a combination of two single-balanced mixers, double-balanced mixer takes twice as much the current, however, conversion gain remains the same as will be made clear in the following pages.

Consider a double-balanced current-switching CMOS mixer with resistive load R_L as shown in Figure 3.4.

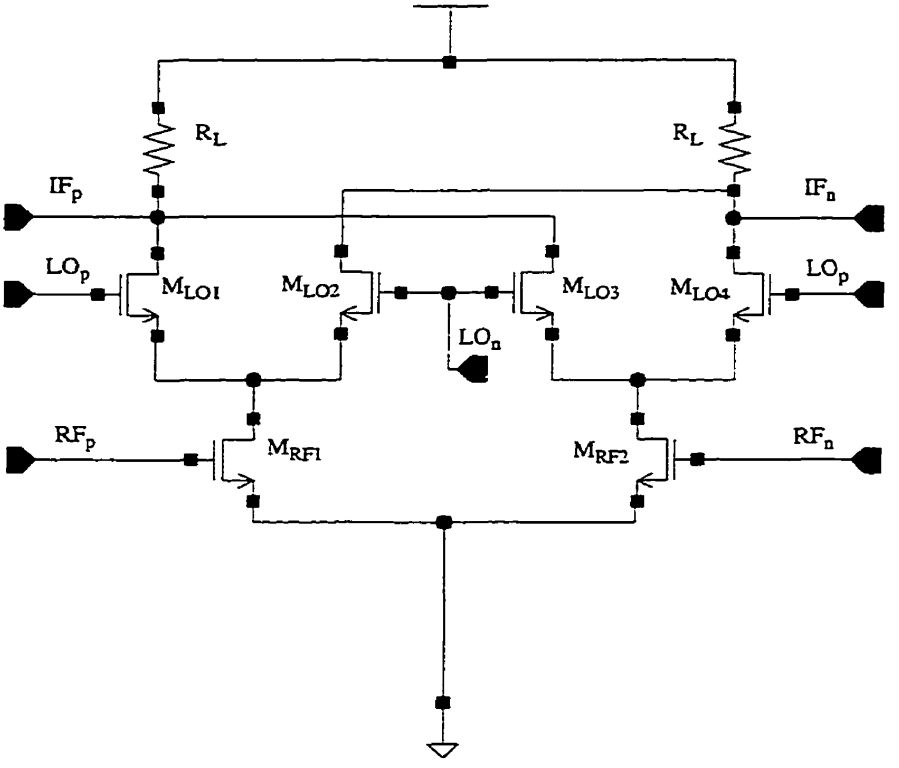

Figure 3.4: Double-Balanced Current-Switching Mixer

The square wave LO signal is again represented by its Fourier series equivalent.

$$LO(t) = \frac{4}{\pi}\left[\cos(\omega_{LO}t) - \frac{1}{3}\cos(3\omega_{LO}t) + \frac{1}{5}\cos(5\omega_{LO}t).....\right]$$

The RF driver drain current in each branch is again the transconductance of the input RF transistor multiplied by the input voltage $v_{RF}(t)$ plus the DC current as shown in the Figure 3.5.

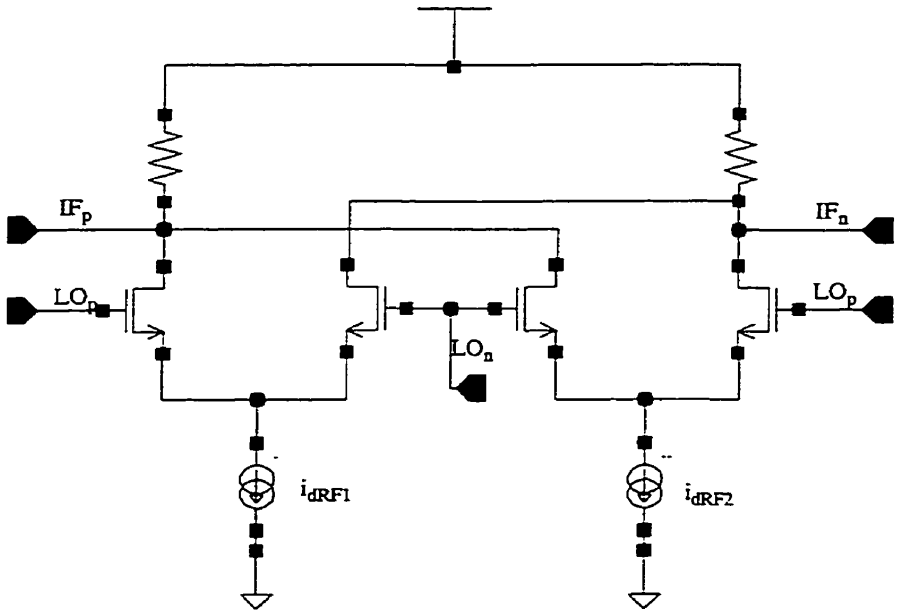

Figure 3.5: RF Driver Current for Double-Balanced Current-Switching Mixer

Here it must be noted that effective transconductance of each input transistor is half the total input transconductance g_m because $v_{RF}(t)$ is now divided equally into two voltages

$\frac{v_{RF}(t)}{2}$ and $\frac{v_{RF}(t)}{2}$ to accommodate differential input, therefore, the drain current through each RF transistor is given by

$$i_{dRF1}(t) = I_T + \frac{g_m}{2} v_{RF}(t) \tag{3.13}$$

and

$$i_{dRF2}(t) = I_T + \frac{g_m}{2} v_{RF}(t) \tag{3.14}$$

The total RF current is given by

$$i_{dRF}(t) = i_{dRF1}(t) - i_{dRF2}(t)$$

$$\Rightarrow \quad i_{dRF}(t) = \left[I_T + \frac{g_m}{2} v_{RF}(t)\right] - \left[I_T + \frac{g_m}{2} v_{RF}(t)\right]$$

$$\therefore \quad i_{RF}(t) = g_m v_{RF}(t) \tag{3.15}$$

Equation 3.15 shows two very important results. First, the DC current I_T through each branch is cancelled out and second, the RF AC current in Equation 3.15 for the double-balanced mixer is same as the RF AC current of the single-balanced mixer (Equation 3.3), therefore, both have the same conversion gain [15], [16].

The output current for double-balanced CMOS switching mixer is given by

$$i_o(t) = \frac{2}{\pi} g_m V_{RF} [\cos(\omega_{RF} - \omega_{LO})t + \cos(\omega_{RF} + \omega_{LO})t]$$

The output IF current is given by

$$i_{IF}(t) = \frac{2}{\pi} g_m V_{RF} \cos(\omega_{IF} t) \tag{3.16}$$

The output IF voltage is Equation 3.16 multiplied by the output load R_L

$$v_{IF}(t) = \frac{2}{\pi} g_m R_L V_{RF} \cos(\omega_{IF} t) \tag{3.17}$$

From Equation 3.16, it is clear that a double-balanced mixer effectively suppresses both the LO and RF feedthrough at the output IF port. Also, the voltage conversion gain is same for both single-balanced and double-balanced mixer structures. i.e.

$$G_v = \frac{V_{IF}}{V_{RF}} = \frac{2}{\pi} g_m R_L \tag{3.18}$$

It should be noted that Equation 3.17 is true only for the double-balanced CMOS mixer when output is taken differentially and this equation assumes instantaneous switching by the commutating LO quad transistors.

If the output is single-ended then, as discussed earlier in the case of single-balanced mixers, there will be a DC term present in the LO signal which gets multiplied with the RF voltage signal resulting in some additional components at the output. Output current in this case is given by the following equation.

$$i_o(t) = \left(I_T + \frac{g_m}{2}V_{RF}\cos(\omega_{RF}t)\right)\left[\frac{1}{2} + \frac{4}{\pi}\left(\cos(\omega_{LO}t) - \frac{1}{3}\cos(3\omega_{LO}t)\ldots\right)\right]$$

$$+\left(I_T - \frac{g_m}{2}V_{RF}\cos(\omega_{RF}t)\right)\left[\frac{1}{2} + \frac{4}{\pi}\left(\cos(\omega_{LO}t) - \frac{1}{3}\cos(3\omega_{LO}t)\ldots\right)\right]$$

which can be reduced to

$$i_o(t) = I_T + \frac{2}{\pi}g_m V_{RF}[\cos(\omega_{RF}t - \omega_{LO}t) + \cos(\omega_{RF}t + \omega_{LO}t)] \qquad (3.19)$$

and the output IF voltage is given by

$$v_{IF}(t) = \frac{I_T R_L}{2} + \frac{1}{\pi}g_m R_L V_{RF}\cos(\omega_{IF}t) \qquad (3.20)$$

Equation 3.20 shows the presence of DC offset in the output IF port, however, RF and LO leakage terms are ideally suppressed. This DC component can be removed by using a DC blocking capacitor at the output port. It should be noted that IF output voltage for single-ended output is again half of the differential output voltage.

3.2.3 Voltage Conversion Gain of CMOS Cascode Mixer

In contrast to current-switching mixers where we have two types of configurations, namely single-balanced and double-balanced mixers, there are three types of CMOS dual gate or cascode mixer structures. The first and the simplest is a single cascode mixer. The other two types i.e. single-balanced and double-balanced cascode mixers are just the combination of two and four cascoded structures respectively, which progressively helps in achieving a LO short at the output IF port without using passive LO rejection circuitry.

The analysis of CMOS cascode mixer is quite complex as compared to the current-switching mixers because the input RF driver transistor is operating in linear region of operation, where drain-source resistance is also significant. The schematic of CMOS cascode mixer is shown in Figure 3.6.

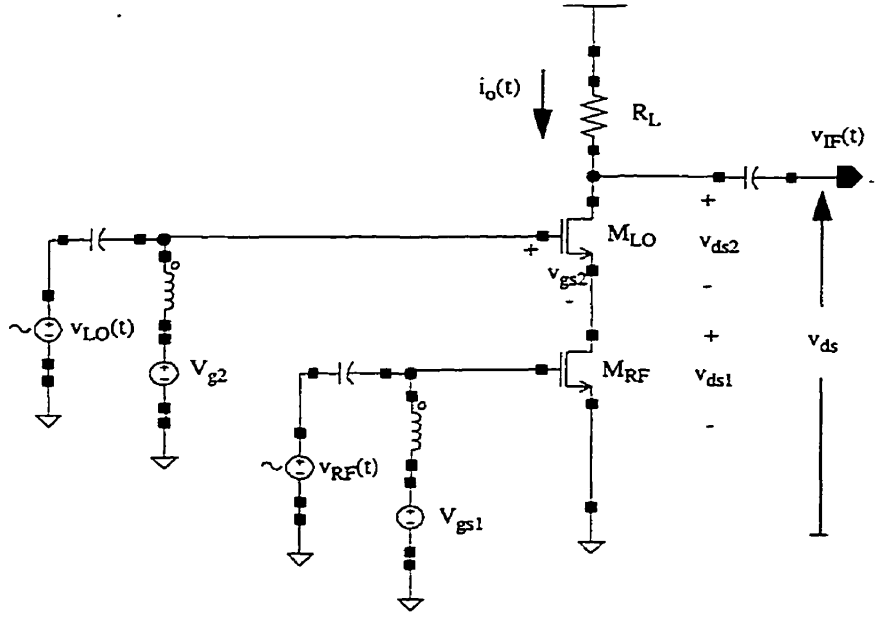

Figure 3.6: CMOS Single Cascode Mixer

The operation of this mixer was discussed briefly in Chapter 2, where it was established that the best mode of operation for this kind of drain mixer is when the lower transistor M_{RF}, which is also the input RF transistor, operates in linear region while the upper transistor M_{LO}, which is fed with a large LO signal, operates in the saturation region and acts as a common-gate amplifier for the mixing stage. The sinusoidal LO signal modulates the transconductance g_{m1} of M_{RF} which swings between linear and saturation regions of operation due to the application of positive and negative excursions of the large LO signal.

A good analysis for a MESFET cascode mixer, which can also be applied to a CMOS cascode mixer, is given in [30]. The output IF voltage, in this case, is given by

$$v_{IF}(t) = \left[\frac{R_L AB}{V_T^2} - \frac{3R_L ABC}{2V_T^2} \times \overline{V_{LO}^2} - \frac{R_L 2B^3 CA}{V_T^2}\right] \times (\overline{V_{LO} V_{RF}}) \cos(\omega_{IF} t) \qquad (3.21)$$

where

$$A = \frac{-2I_{dss}(1 + \lambda v_{ds2})}{V_T - V_{g1}}$$

$$B = V_T - V_{g2} + V_{dd} - v_{ds2}$$

$$C = \frac{R_L I_{dss}}{V_T^2}\left[\frac{\lambda}{1 + \lambda(V_{dd} - v_{ds2})} + \frac{\alpha\left(1 - \frac{\alpha(V_{dd} - v_{ds2})}{3}\right)^2}{1 - \left(1 - \frac{\alpha(V_{dd} - v_{ds2})}{3}\right)^3}\right]$$

and

I_{dss} = Drain current with gate shorted to source

λ = Empirical channel-length modulation factor

R_L = Load resistance

$\overline{v_{LO}}$ = Time-averaged value of $v_{LO}(t)$

$\overline{v_{RF}}$ = Time-averaged value of $v_{RF}(t)$

V_T = Threshold voltage of the FET

3.2.4 Transconductance g_m and Conversion Gain

In the previous sub-sections, the voltage conversion gain of both the current-switching and CMOS cascode mixers has been discussed. The conversion gain shows a strong dependence on the transconductance of the input RF transistors.

The DC transconductance g_m for FET is given by the relation

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{3.22}$$

where I_D is the drain-source current and V_{GS} is the gate-source voltage.

In active region, I_D for a N-MOSFET is given by the following first order equation

$$I_D = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{tn})^2 \tag{3.23}$$

where

μ_n = Mobility of Electrons (technology dependent)

C_{ox} = Gate Capacitance per Unit Area

V_{tn} = Threshold Voltage of NMOS (technology dependent)

W = Width of Transistor Gate

L = Length of Transistor Gate

From Equation 3.23

$$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{tn}) \tag{3.24}$$

Similarly, for transistor operating in linear region, transconductance is given by

$$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)V_{DS} \tag{3.25}$$

Equations 3.24 and 3.25 show that transconductance is directly proportional to the aspect ratio $\frac{W}{L}$ of a MOSFET. Hence, by using large width and minimum length gate, the g_m and therefore, the conversion gain of a CMOS mixer can be increased significantly. However, it should be noted that increasing gate area also increases gate-source and gate-drain parasitic capacitances which limit the capability of a transistor to operate at higher frequencies by decreasing the unity current-gain transition frequency f_t of a transistor, in addition to the increased noise figure and higher power consumption, as discussed in Sec-

tion 3.5. Therefore, a trade-off is usually necessary depending on the applications and the requirements.

3.3 Linearity and Intermodulation Intercept Point

Double-balanced current-switching mixers show better linearity as compared to the single-balanced mixers because of the cancellation of both LO and RF leakage terms and the even-order harmonics at the output port. Linearity, in general, depends strongly on the LO power and input RF transistor overdrive voltage (V_{GS}-V_T). CMOS current-switching mixers usually require higher LO drive than their BJT counterparts because larger LO voltage swing is needed to turn-off one side of the switching pair or quad [15].

Single-balanced and double-balanced CMOS cascode mixers have better linearity and lower conversion gain as compared to the respective current-switching CMOS mixers, more or less due to the same reason i.e. in cascode mixers, input RF transistor operates in linear region of operation which inherently is more linear but has lower conversion transconductance as compared to the transistor operating in saturation region.

1-dB Compression Point (P_{1dB}) and Third-Order Intermodulation Intercept Point (IP_3) are the measures of mixer linearity. Non-linearity can be expressed by a Taylor series expansion.

$$v_o = a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + a_4 v_i^4 + ... + a_n v_i^n \qquad (3.26)$$

where v_o and v_i are the input and output signals respectively and a_1, a_2, a_3, ... a_n are constant coefficients.

If v_i is represented by a single-tone then only the first term ($a_i v_i$) in Equation 3.26 gives the required fundamental output for a perfectly linear circuit. However, due to the presence of non-linearities in the devices, higher order terms are also present in a real system.

First, considering a second order harmonic of the input signal $v_i = A\cos(\omega t)$, then

$$v_i^2 = (A\cos\omega t)^2 = \frac{A^2}{2}(1 + \cos 2\omega t)$$

Hence, for n = 2, the square of the input voltage generates a second-order harmonic $\frac{A^2}{2}\cos 2\omega t$ plus a DC term $\frac{A^2}{2}$. It can be seen, that if 'n' is an even number then 'nth' power of v_i generates all the even-order harmonics equal to and less than 'n' plus the DC term.

If n = 3, then cube of v_i is given by

$$v_i^3 = (A\cos\omega t)^3 = \frac{3}{4}A^3\cos\omega t + \frac{1}{4}A^3\cos 3\omega t \qquad (3.27)$$

Generalizing, if 'n' is an odd number, the 'nth' power of v_i generates fundamental term plus all the odd order harmonics equal to and less than 'n'. It can be seen from Equation 3.27 that odd-order harmonics produce a fundamental term which is directly

added to the desired fundamental term. For example, for n = 5, the total desired output signal would be:

$$v_{o(desired)} = A\cos\omega t + \frac{3}{4}A^3\cos\omega t + \frac{5}{8}A^5\cos\omega t \qquad (3.28)$$

The cubed and higher order terms are usually insignificant for a small input signal. However, their amplitude increase with the power of 'n' of the amplitude of the input signal and their effect on the total output signal keeps on getting more significant in proportion to the increase in the input signal amplitude. If the polarity of a_3, which represents the dominant third-order harmonic distortion, is negative (which is generally the case), then it will cause gain compression for a large input signal. When the conversion gain is 1 dB lower than its projected small-signal gain, the level is called the 1-dB compression point (P_{1dB}) and is a measure of dynamic range of a RF building block.

If the input voltage is sum of two or more signals having different frequencies then the non-linear terms in Equation 3.26 would also generate frequency-mixing products in addition to the higher order harmonics. These product terms are called Intermodulation (IM) products. For example if v_i is given by

$$v_i = A_1\cos\omega_1 t + A_2\cos\omega_2 t$$

then square of v_i after trigonometric manipulations would be

$$v_i = \frac{A_1^2}{2}(1 + \cos 2\omega_1 t) + \frac{A_2^2}{2}(1 + \cos 2\omega_2 t)$$

$$+ A_1 A_2[\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t] \qquad (3.29)$$

In Equation 3.29, first two terms are second-order harmonics plus DC components of respective input signals, while third term gives the second-order intermodulation products as sum and difference frequencies. If both the signals have frequencies quite close to each other e.g. one channel apart, then their difference and sum IM products do not fall in the in-band spectrum and can easily be filtered out. However, if the receiver employs a direct conversion scheme, then the second-order IM products are of great consequence because their frequencies fall in the baseband spectrum in addition to adding a problematic DC offset.

Now consider cube of the input signal v_i

$$v_i^3 = (A_1 \cos\omega_1 t + A_2 \cos\omega_2 t)^3$$

$$= (A_1 \cos\omega_1 t)^3 + (A_2 \cos\omega_2 t)^3$$

$$+ 3(A_1 A_2^2 \cos\omega_1 t(\cos\omega_2 t)^2) + 3(A_1^2 A_2(\cos\omega_1 t)^2 \cos\omega_2 t)$$

After using a few trigonometric relations and rearranging, v_i^3 can be written as

$$v_i^3 = \frac{3}{4}(A_1^3\cos\omega_1 t + A_2^3\cos\omega_2 t) + \frac{1}{4}(A_1^3\cos 3\omega_1 t + A_2^3\cos 3\omega_2 t)$$

$$+ A_1A_2\left[\frac{3}{2}(A_2\cos\omega_1 t + A_1\cos\omega_2 t) + \frac{3A_2}{4}(\cos(\omega_1 - 2\omega_2)t + \cos(\omega_1 + 2\omega_2)t)\right.$$

$$\left. + \frac{3A_1}{4}(\cos(2\omega_1 - \omega_2)t + \cos(2\omega_1 + \omega_2)t)\right] \qquad (3.30)$$

At the output, $v_i^3(t)$ is multiplied by a_3 which is usually negative, therefore, the first two terms in Equation 3.30 will introduce third-order harmonic distortion for a large input signal resulting in gain compression.

The third-order IM products (IM_3) require a special attention. The sum and difference frequencies, in this case, fall directly at the required spectrum which could not be filtered out. For example, suppose v_i is given by a sum of two tones of equal amplitude having frequencies $f_1 = 2.4$ GHz and $f_2 = 2.41$ GHz. This input is mixed down with a 2.15 GHz LO signal so that the IF output is at 250 MHz and 260 MHz. The down-converted IM_3 products are given as

$$IM_3 = (2f_1 - f_2) - f_{LO} = 240 \text{ MHz}$$

$$IM_3 = (2f_2 - f_1) - f_{LO} = 270 \text{ MHz}$$

The down-converted IM_3 products fall within the required band of spectrum and cannot be filtered out. These IM_3 products, again, are of less consequence for small input signal but

increase 3 times the input signal amplitude and at some large input signal they will be equal to the desired output fundamental. This level is called Third-Order Intermodulation Intercept Point (IP_3), that can be referred to input or output power. It should be noted that IP_3 is a hypothetical level which can never be achieved in reality, in contrast to P_{1dB} which can physically be measured. Therefore, IP_3 is measured basically at a small-signal input level while P_{1dB} is a large signal measurement.

The most common method of measuring IP_3 is by applying two equal amplitude, small-signal tones at the input and measuring output fundamental power and output IP_3 and using slope equations to calculate IP_3 as shown in Figure 3.7 [9].

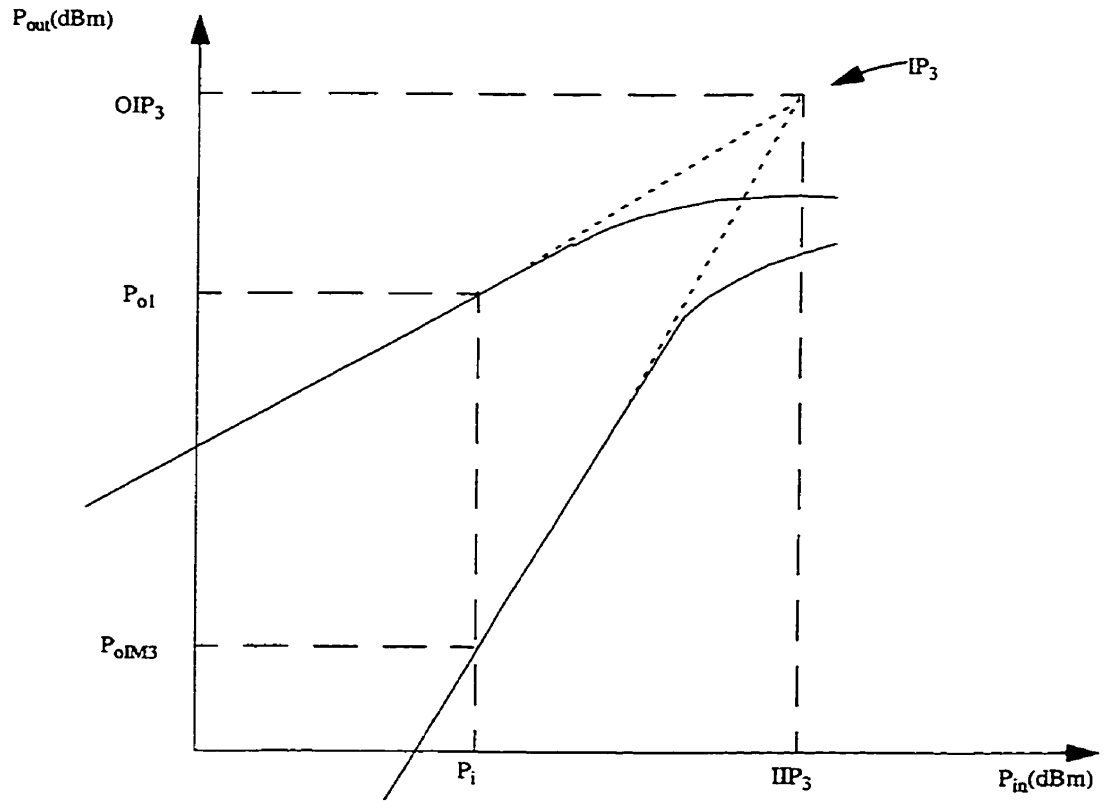

Figure 3.7: Graphical IP_3 Determination

where

P_i = Small-signal Input Power

P_{o1} = Fundamental Output Power

P_{oIM3} = IM_3 Output Power

IIP_3 = Input IP_3

OIP_3 = Output IP_3

From simple concepts of analytical geometry, slope is defined as

$$\text{Slope} = \frac{y_2 - y_1}{x_2 - x_1}$$

Therefore, $$\frac{OIP_3 - P_{o1}}{IIP_3 - P_i} = 1 \quad \Rightarrow \quad IIP_3 - P_i = OIP_3 - P_{o1} \tag{3.31}$$

and $$\frac{OIP_3 - P_{oIM3}}{IIP_3 - P_i} = 3 \quad \Rightarrow \quad IIP_3 - P_i = \frac{OIP_3 - P_{oIM3}}{3} \tag{3.32}$$

From Equations 3.31 and 3.32

$$OIP_3 - P_{o1} = \frac{OIP_3 - P_{oIM3}}{3}$$

$$\Rightarrow \quad OIP_3 = \frac{1}{2}(3P_{o1} - P_{oIM3}) \tag{3.33}$$

Also from Equation 3.31

$$IIP_3 = P_i - P_{o1} + OIP_3$$

$$\Rightarrow \quad IIP_3 = P_i + \frac{1}{2}(P_{o1} - P_{oIM3}) \tag{3.34}$$

To calculate IP_3 analytically, consider the coefficients of output fundamental signal and IM_3 products in Equation 3.30 and assuming A_1=A_2 =A under small-signal conditions

Therefore, fundamental output at ω_1 $= a_1 A + \frac{3}{4}a_3 A^3 + \frac{3}{2}a_3 A^3$

$$= a_1 A + \frac{9}{4}a_3 A^3$$

IM_3 at $(2\omega_1-\omega_2)$ and $(2\omega_2-\omega_1)$ $= \frac{3}{4}a_3 A^3$

At IP_3 both are equal, therefore, magnitude of IP_3 is given by

$$IP_3 = A = \sqrt{\frac{2a_1}{3a_3}} \tag{3.35}$$

It should be noted that Equation 3.35 is valid for two tone input signal only.

3.4 Noise Figure in CMOS Mixers

One of the performance parameter considered, while designing mixers is the noise figure. Fortunately, conversion gain and noise figure in active mixers are related in such a way that a design optimized for better noise figure performance usually shows good conversion gain, however, converse is not always true [14], [17].

Consider the high-frequency, small-signal FET model shown in Figure 3.8.

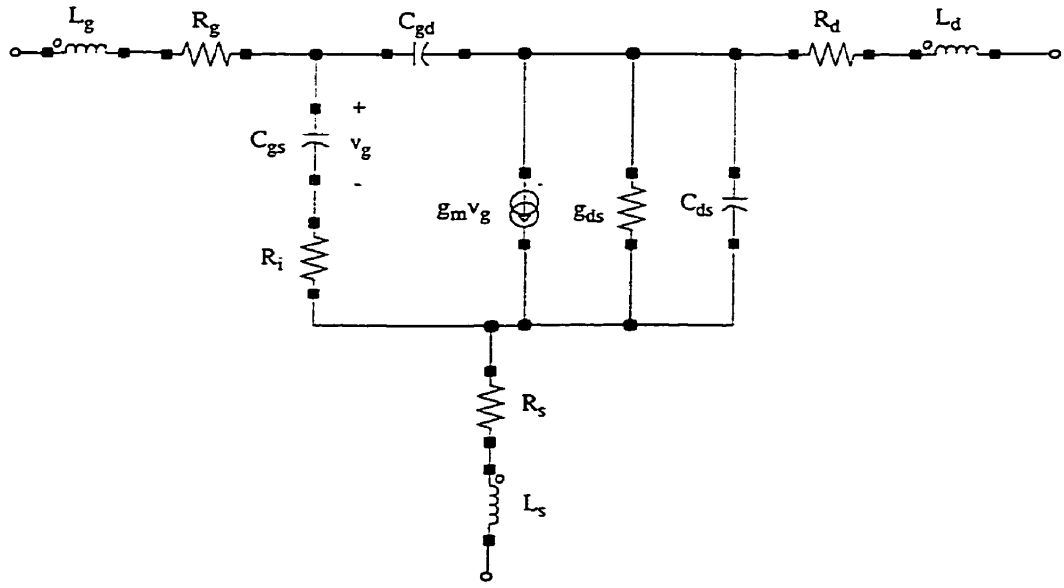

Figure 3.8: High Frequency Small-Signal Model for FET

L_g, R_g and L_s, R_s and L_d, R_d represent the respective inductance and resistance at gate, source and drain of a FET. R_i is the channel charging resistance which represents the non-instantaneous response of the channel charge due to the instantaneous variation in gate-source voltage [18]. Since gate-source voltage is proportional to the transconductance g_m of the device, R_i is also proportional to g_m and related as

$$R_i = \frac{1}{5g_m} \propto \frac{1}{g_m} \tag{3.36}$$

where factor of 5 is due to the distributed nature of channel resistance between source and drain.

The minimum noise figure NF_{min} for the high-frequency small-signal FET model shown in Figure 3.8 is given by the equation [19].

$$NF_{min} = 1 + 2\omega\frac{C_{gs}}{g_m}\sqrt{\frac{R_s + R_g}{R_i}} \tag{3.36}$$

Few important observations are apparent from Equation 3.36.

- NF_{min} is proportional to the frequency of operation
- NF_{min} is proportional to the gate resistance R_g. If contact to the gate of transistor is single-ended i.e. only one end of the gate is connected to the signal, then gate resistance is given by the relation

$$R_g = \frac{R_{sh}W}{3\ L} \tag{3.37}$$

where R_{sh} is the sheet resistance of gate material, W is the width and L is the length of a transistor gate. The factor of 3 in Equation 3.37 is again due to the distributed nature of gate resistance. However, by contacting gate from both ends, this factor can be increased to $3\times(2)^2 = 12$ times i.e.

$$R_g = \frac{R_{sh}W}{12\ L}$$

Therefore, by connecting gate at both ends, gate resistance R_g can be reduced 4 times, resulting in better NF_{min}. In addition, by using multi-fingered gate, R_g of the transistor

can further be reduced because width of gate, and hence its resistance, is now equally divided among all the gate fingers.

In current-switching mixers, the switching pair or quad injects further noise due to the imperfect switching of LO transistors. This noise results from the fact that both the LO transistors in case of single-balanced mixer, remain on for some period of time. Therefore, thermal noise introduced by both transistors is added to the total output noise power. Similarly, in case of double-balanced current-switching mixers, all the transistors of switching quad remain on for some period of time introducing considerable thermal noise at the output. This thermal noise ideally has twice the magnitude as compared to that of the single-balanced mixers [16], [20]. In CMOS cascode mixers, the RF transistors operate in linear region of operation which inherently is more noisy as compared to current-switching RF transistors that operate in saturation region. This is due to the fact that, in the linear region, drain-source resistance r_{ds} affects the transistor performance whereas, in saturation region r_{ds} is very large.

3.5 Unity Current Gain Cut-off Frequency

Figure 3.8 shows a high frequency, small-signal model of a FET. To calculate the unity current gain cut-off frequency of FET, Figure 3.8 can be simplified to an equivalent circuit shown in Figure 3.9 [19].

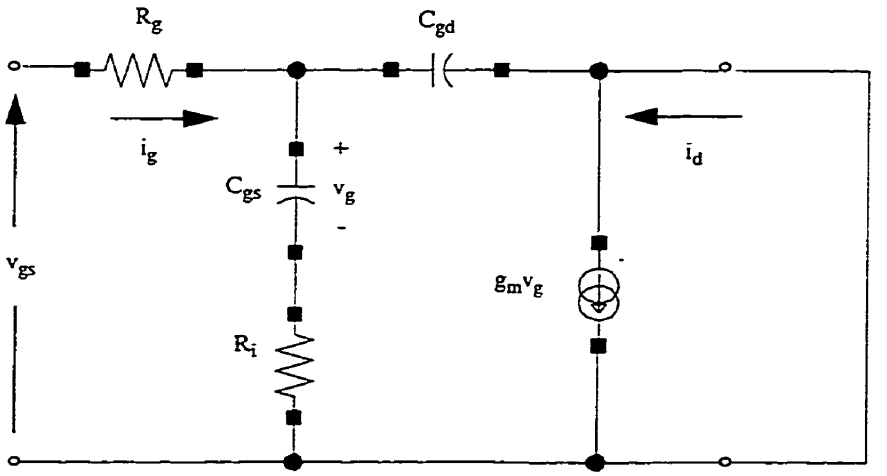

Figure 3.9: Simplified Small-Signal Model of High Frequency FET

Current gain is given by

$$G_i = \left|\frac{i_d}{i_g}\right|$$

$$= \frac{g_m v_g}{v_g \omega (C_{gs} + C_{gd})} = \frac{g_m}{\omega (C_{gs} + C_{gd})}$$

By definition, unity current gain cut-off frequency f_t is the frequency at which G_i becomes unity under short-circuit conditions, i.e.

$$f_t = \frac{g_m}{2\pi (C_{gs} + C_{gd})} \tag{3.38}$$

Therefore, f_t is directly proportional to the transconductance g_m and inversely proportional to the gate-source capacitance C_{gs} and drain-source capacitance C_{gd} of the transistor. However, under saturation conditions, C_{gd} is much lower than C_{gs}. From Equation 3.24,

g_m depends on the $\frac{W}{L}$ ratio of the transistor while C_{gs} and C_{gd} depend on the total gate area i.e. $W \times L$. Considering L to be fixed and transistor in saturation, any increase in W will increase both the g_m and C_{gs}. However, this increase in the g_m and C_{gs} is not proportional and C_{gs} increases more as compared to the g_m. Therefore, there is a limit on increasing the gate width W of a transistor as shown in Equation 3.38. Similarly, same trade-off also holds for the minimum noise figure of the transistor (Equation 3.36).

3.6 Summary

Comparison of different types of active CMOS mixer topologies and configurations on the basis of their major performance parameters suggests that the choice of configuration largely depends on the application requirements. Generally, there exists a trade-off between conversion gain and linearity of active mixers. Single-balanced mixers consume less power but their linearity performance is worse than double-balanced structures, which obviously consume twice as much the power. However, major advantage of using double-balanced mixer is the suppression of LO and RF feedthrough and even-order harmonics which might fall in the frequency spectrum that may be allocated to some other user. Also, if the mixer is surrounded by other RF building blocks in an integrated system, the absence of unwanted harmonics will improve the overall performance of the system. All the mixer structures discussed previously are implemented in 0.25 μm standard CMOS process and their simulation and measurement results are reported in Chapter 4 for comparison.

CHAPTER 4

Circuit Design and Performance Evaluation

4.1 Introduction

In this chapter, simulation, measurement and layout issues of the CMOS mixer structures, discussed in Chapter 3, are described. The mixer structures are designed in 0.25 μm standard CMOS technology ($f_t \approx 30$ GHz) using *spectreRF* simulator in Cadence environment. Layouts of the designs are performed using Cadence IC design tool *Virtuoso* and designs are fabricated by Taiwan Semiconductor Manufacturing Company (TSMC) through Canadian Microelectronics Corporation (CMC). Discussion of the results is provided in Section 4.9 that also gives comparison of this work and some other reported CMOS mixers from the recent literature.

In order to evaluate the effects of different CMOS mixer structures and topologies, it is necessary to design and optimize one configuration as a reference design and compare its performance with other topologies and structures with respect to the major performance parameters like conversion gain, linearity and noise figure. In this thesis, it was decided to choose single-balanced CMOS current-switching mixer as a reference configuration

because of its relatively simple structure and the fact that more complex structures like double-balanced current-switching mixers are just the combination of two single-balanced mixers.

It was discovered at the beginning of the thesis that good packaging models for RFICs were not available at frequencies above 1.5 GHz, hence it was concluded to employ direct wafer probing. The available probes were designed for 50 Ω environment which suggested the need for on-chip matching networks for each design. Lumped matching elements especially inductors are not very accurate and suffer from low Q levels, which could have affected the results of this work. Therefore, it was decided not to use lumped matching networks to avoid variations due to the matching networks in the comparison. However, output buffers were placed at the output of the designs for ease of measurement procedure, which also provided good output matching (output return loss greater than industrial standard of 10 dB). As the buffer structure used was similar for each design, its effect on the performance parameters was consistent, regardless of the configuration of the design. For all the simulations and measurements, the input RF frequency is 2.4 GHz, LO frequency is 2.15 GHz, therefore the output IF frequency is 250 MHz.

4.2 Design and Optimization of Single-Balanced CMOS Current-Switching Mixer

As discussed earlier, single-balanced CMOS current-switching mixer has been chosen as a reference design for comparison with all other designed CMOS mixers due to its relatively simple configuration. In Chapter 2, a substantial discussion was provided giving its operation, configuration and limitations. In Chapter 3, a general first order conversion gain

expression, without taking the parasitic capacitances and input/output impedances into account, was derived (Section 3.2.1) and it was shown how the transconductance of the input RF transistor affects the conversion gain and noise figure of the down-conversion mixers which, in turn, is directly proportional to the aspect ratio $\frac{W}{L}$ of a RF transistor (Equation 3.31).

The design is optimized to achieve moderate conversion gain as it is usually undesirable for active mixers to have large conversion gain because of the trade-off between conversion gain/noise figure and dynamic range of down-conversion mixers. This trade-off comes from the fact that higher conversion gain tends to overload the output of the mixer, resulting in lower input P_{1dB}. Also, to increase the linearity, the current flowing through the device needs to be increased but too much current tends to degrade the noise figure of the mixer due to the higher gate-source capacitance as discussed in Chapter 3. The noise figure and input P_{1dB} are also simulated for the optimized design and results are provided in the following discussion.

It was realized after the submission of designs for fabrication, that the simulator used for simulations (*spectreRF*) shows the output power in terms of dBV, instead of dBm. The relation between dBV and dBm, when the ports are matched to 50 Ω, is given as follows:

$$P_{dBm} = 10\log\left[\left\{\left(\frac{V_P}{\sqrt{2}}\right)^2\left(\frac{1}{50}\right)\right\}\left(\frac{1000mW}{1mW}\right)\right]$$

$$= 10\log(V_P^2) + 10\log\left(\frac{1000}{100}\right)$$

Therefore, $$P_{dBm} = P_{dBV} + 10dB$$

i.e. the power in dBV (at 50 Ω) is 10 dB less than the power expressed in dBm, therefore, to get the output power in dBm, 10 dB has to be added to the power given in dBV. However, the input power P_{RF} is specified in dBm in the simulator i.e. no correction is needed in input power and therefore, in the simulated input P_{1dB}. Summarizing,

$$\mathbf{P_{IF}(dBm)}|_{50\Omega} = \mathbf{P_{IF}(dBV)}|_{50\Omega} + \mathbf{10dB} \qquad (4.A)$$

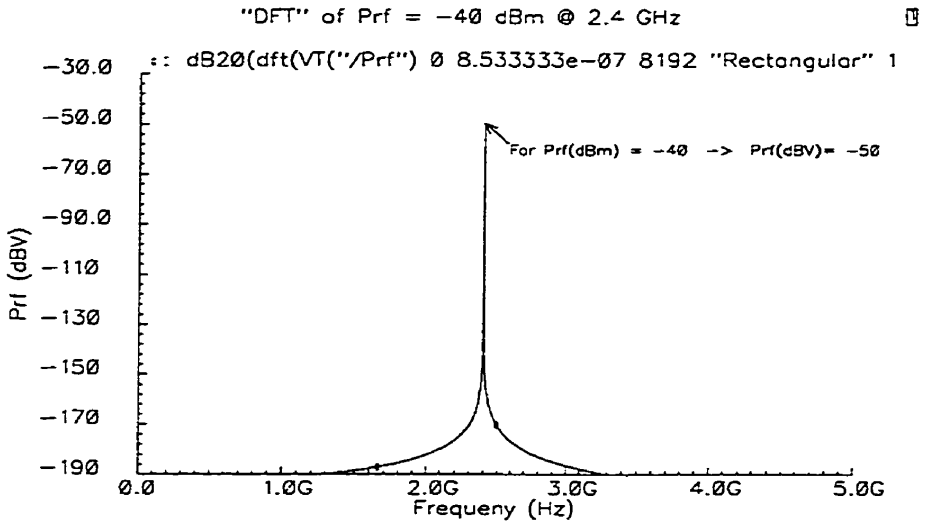

Figure 4.1: DFT of Input Power

Figure 4.1 shows the simulations of a signal having power equal to -40 dBm. The source used in *spectreRF* i.e. 'psin' has a source resistance of 50 Ω. By using a 50 Ω termination and performing Discrete Fourier Transformation (DFT), the output power level is -50 dBV which is exactly 10 dB down the input power level expressed in dBm as shown in Equation 4.A.

This 10 dB correction is shown in all the output IF power vs. Input RF power and the output IF power vs. LO power plots as a correction note for all the designed mixers. For the cases, where actual simulation plots are not provided, the 10 dB correction is manually made to the *matlab* plots, however the correction note is still given.

4.2.1 Schematic and Simulation Issues

Figure 4.2 shows the complete schematic of CMOS single-balanced current-switching mixer where an ideal transformer is used to convert the single-ended LO signal into a differential signal. Similarly, an ideal transformer is employed at the IF port to convert the differential output into a single-ended IF output. AC blocking inductors and DC blocking capacitors are placed at all signal inputs and outputs to keep the simulation environment as close to the measurement setup as possible where bias-tees would be used for DC biasing and signal inputs.

As the designs are not packaged, the bond-wire inductances are not an issue and their effects have not been included in the simulations. However, pad capacitances have been included in the post layout simulations.

PMOS transistors have been used as active load because of their high output impedance, which helps in achieving higher conversion gain as shown in Equation 3.9. Also, the gate bias of load transistors has been kept off-chip for better control over the output power during measurements. NMOS transistor is used as a current source at the source terminal of the RF transistor, with gate and drain tied together (diode-connected) so that it remains in saturation region of operation at all times.

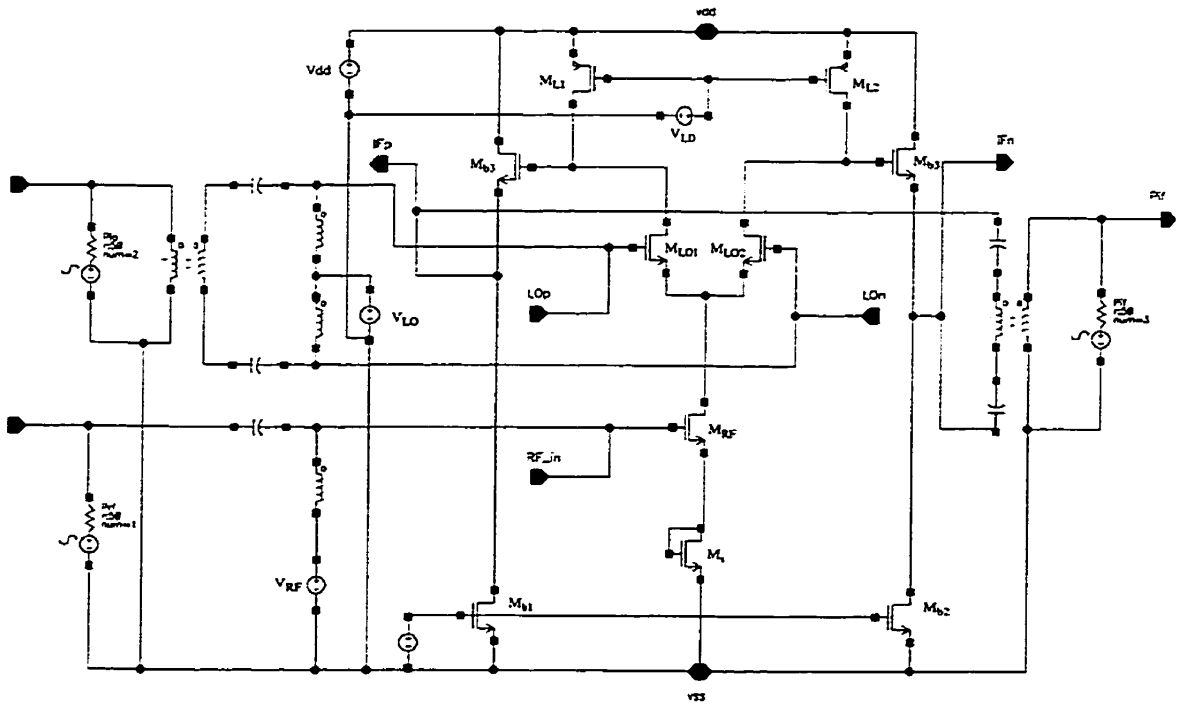

Figure 4.2: Complete Schematic of Single-Balanced Current-Switching Mixer

4.2.2 Device Sizes

In Chapter 3, it was shown how the transconductance g_m of input RF transistor affects the conversion gain and noise figure of a mixer. Therefore, the most critical task while designing a CMOS mixer, is the size of the RF transistor. RF and LO transistors should be of minimum available channel length so that they can operate at higher frequencies, due to the limitations of unity current gain cut-off frequency f_t (Section 3.5). In the case of switching mixers, the drain current flowing through each LO transistor is half the total drain current of the RF transistor, therefore, for same minimum channel lengths, the chan-

nel width of the LO transistors should be half as compared to the RF transistor channel width.

As the conversion gain depends on the transconductance g_m of the RF transistor, the $\frac{W}{L}$ ratio should be large for higher gain. However, it should not be too large because larger transistors have higher gate-source parasitic capacitance which tends to limit the high frequency operation and increases the noise figure of FETs as discussed in Sections 3.5.

For each transistor, the total channel width has been divided into a number of fingers to reduce gate resistance. For this thesis, a finger width of 10 μm has been standardized and each transistor's channel width is a multiple of 10 μm. The choice of using 10 μm finger width with minimum length is due to the fact that the available transistor model parameters from CMC are categorized according to the width and length of transistors and below 10 μm the model category changes. Also, by setting a standard width for each finger and then using its multiples, the layouts of the designs are greatly simplified.

The sizes of buffer transistors are set such that the current flowing through the lower buffer transistors (M_{b1} and M_{b2} in Figure 4.2) and their drain-source voltage show an approximate 50 Ω impedance at the output port. The buffer current can be controlled by varying the external gate bias voltage of lower buffer transistor.

The number of fingers for each transistor is shown in Table 4.1. The sizes of current-source transistor M_s and load transistors M_{L1} and M_{L2} are set such that the total current flowing through the mixer core is between 1 - 2 mA, which can further be controlled by adjusting the gate bias voltage of load transistors. Lower current limit is set to 1 mA as

below this limit, the RF transistor comes out of saturation and all the performance parameters degrade significantly. Although, higher current levels help in achieving better linearity but it was decided to fix the upper current limit of the single-balanced current-switching mixer to 2 mA in order to investigate its performance at lower power consumption.

Table 4.1: Transistor Sizes for Single-Balanced Current-Switching Mixer

Transistor	Width of Each Finger (μm)	Number of Fingers
M_{RF}	10	m_{rf}
M_{LO1} & M_{LO2}	10	$\frac{m_{rf}}{2}$
M_S	10	24
Buffer	10	12
M_{L1} & M_{L2}	10	6

The bias voltages and DC operating points are adjusted so that each transistor remains in its intended region of operation. The input RF power level of -30 dBm is also standardized for all parametric simulations. In *spectreRF*, "Single-point Periodic Steady-State (SPSS)" analysis gives the output power versus input power plot along with the input P_{1dB}. Also, same analysis can be used for multiple parametric sweeps of different variables against output power level.

The parametric simulation is performed by sweeping number of fingers 'm_{rf}' from 8 to 40. Figure 4.3 shows the corresponding plot of output IF power versus RF transistor width W_{RF}, which shows the highest conversion gain for $W_{RF} = 240$ μm.

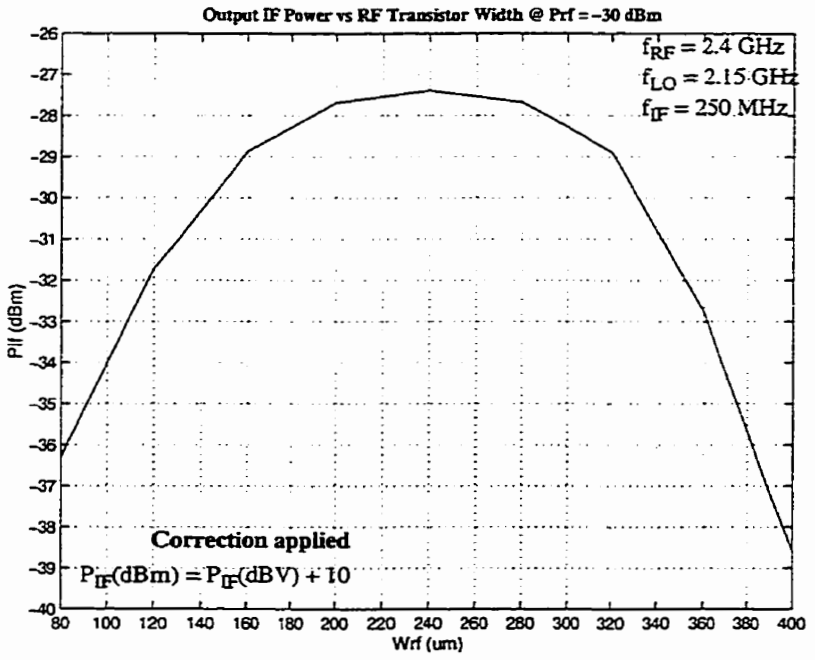

Figure 4.3: P_{IF} vs W_{RF} for Single-Balanced Current-Switching Mixer

Now keeping W_{RF} = 240 μm and W_{LO1} = W_{LO2} = 120 μm, another parametric simulation is done by sweeping the source transistor number of fingers 'm_s' from 6 to 60 to further optimize the design (Figure 4.4). It is ensured that the total DC current remains within the design specs of 1-2 mA and all the transistors remain in the saturation region of operation.

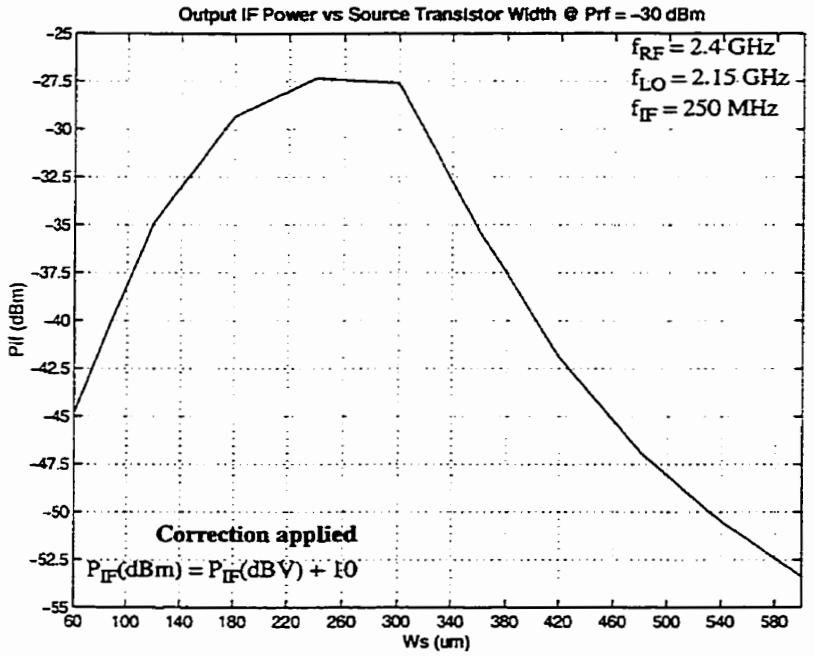

Figure 4.4: P_{IF} vs W_S for Single-Balanced Current-Switching Mixer

Same procedure is repeated by sweeping load transistor number of fingers 'm_{ld}' and the simulation results are shown in Figure 4.5.

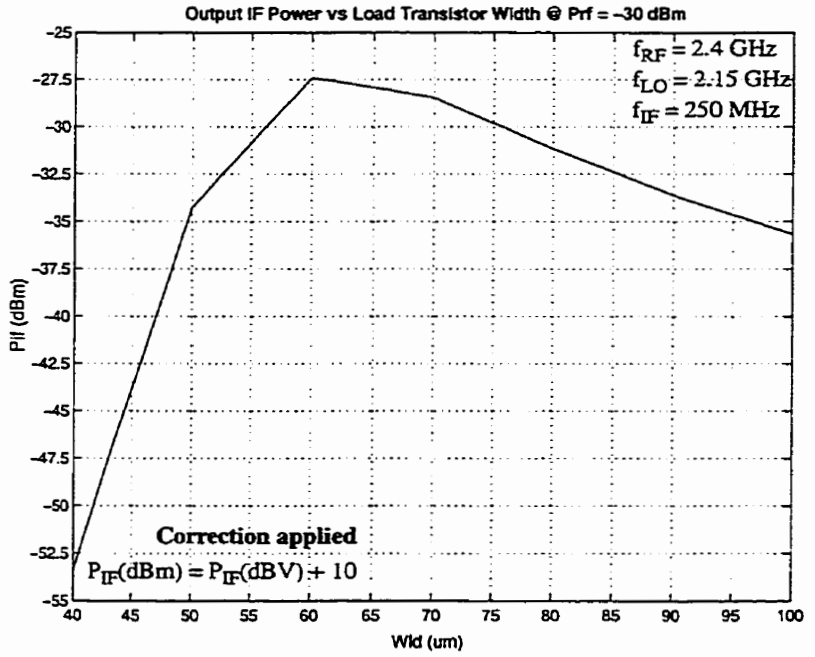

Figure 4.5: P_{IF} vs W_{LD} for Single-Balanced Current-Switching Mixer

After establishing all the transistor sizes, LO input power has been swept from -10 to 14 dBm at P_{RF} = -30 dBm and plot shows the best output IF power for P_{LO} = 2 dBm (Figure 4.6)

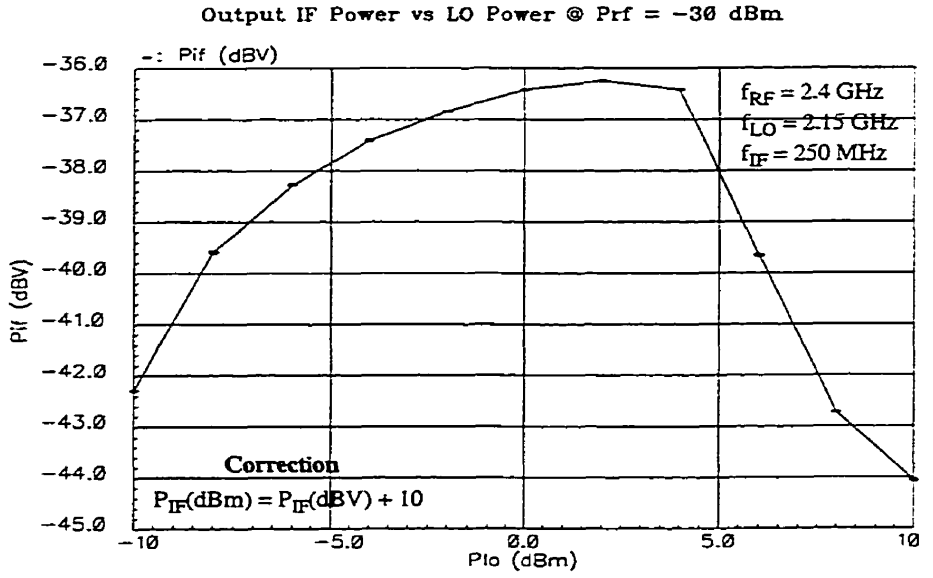

Figure 4.6: P_{IF} vs P_{LO} for Single-Balanced Current-Switching Mixer

The final optimized single-balanced current-switching mixer is given in Figure 4.7, where all the transistor sizes are provided.

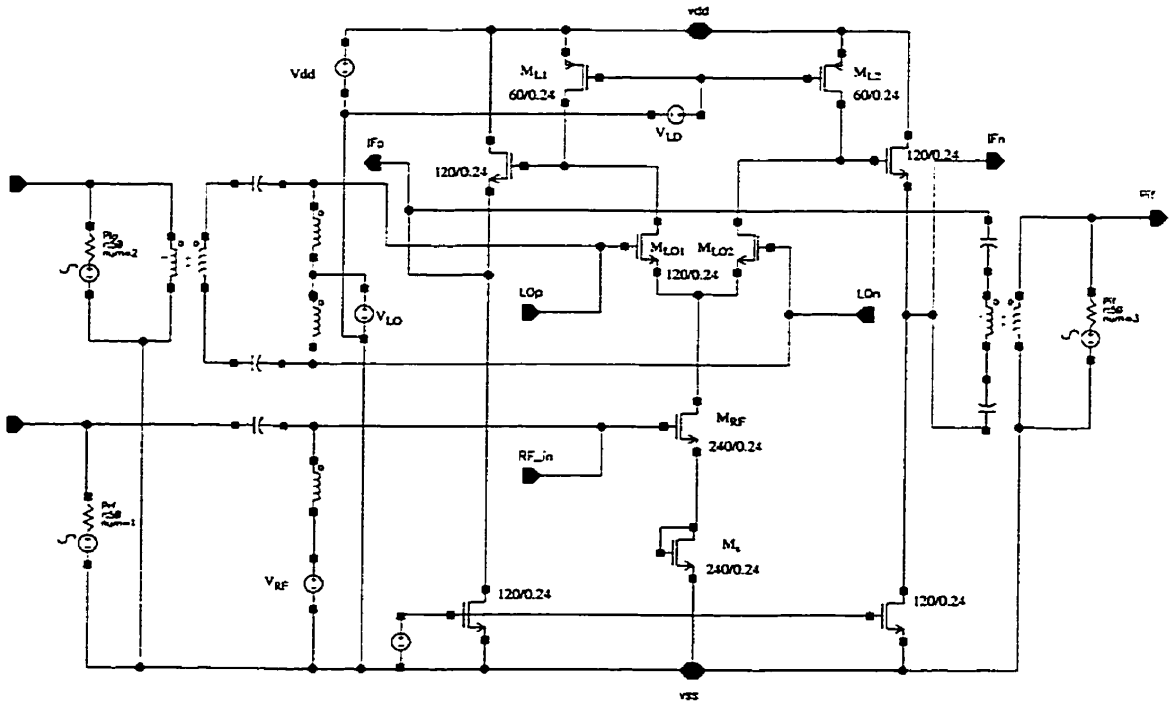

Figure 4.7: Single-Balanced CMOS Current-Switching Mixer

Again, using *spectreRF* SPSS analysis, RF power is swept from -70 dBm to 0 dBm at P_{LO} = 2 dBm, shown in Figure 4.8. Figure 4.9 gives the frequency spectrum of P_{IF}, P_{RF} and P_{LO} and we can see the presence of LO feedthrough in the output spectrum. The presence of a harmonic at 1.9 GHz in the RF spectrum is due to the LO leakage to the RF port which results in an image frequency signal.

The noise figure of the optimized design is also simulated in *spectreRF* simulation tool. The final single-balanced current-switching mixer exhibits a simulated noise figure of 15.6 dB and input P_{1dB} of -9.04 dBm.

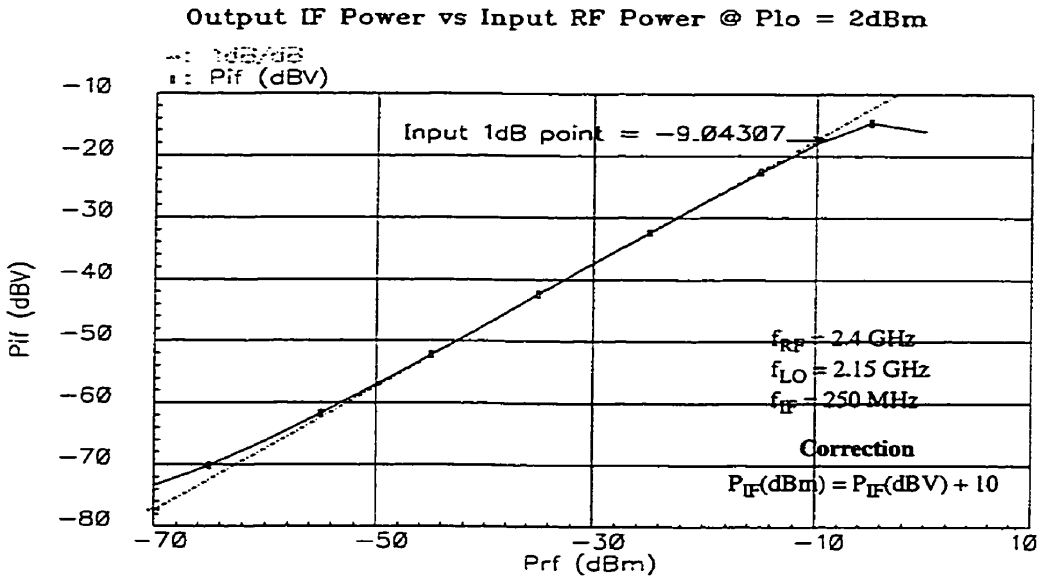

Figure 4.8: P_{IF} vs P_{RF} for Single-Balanced Current-Switching Mixer

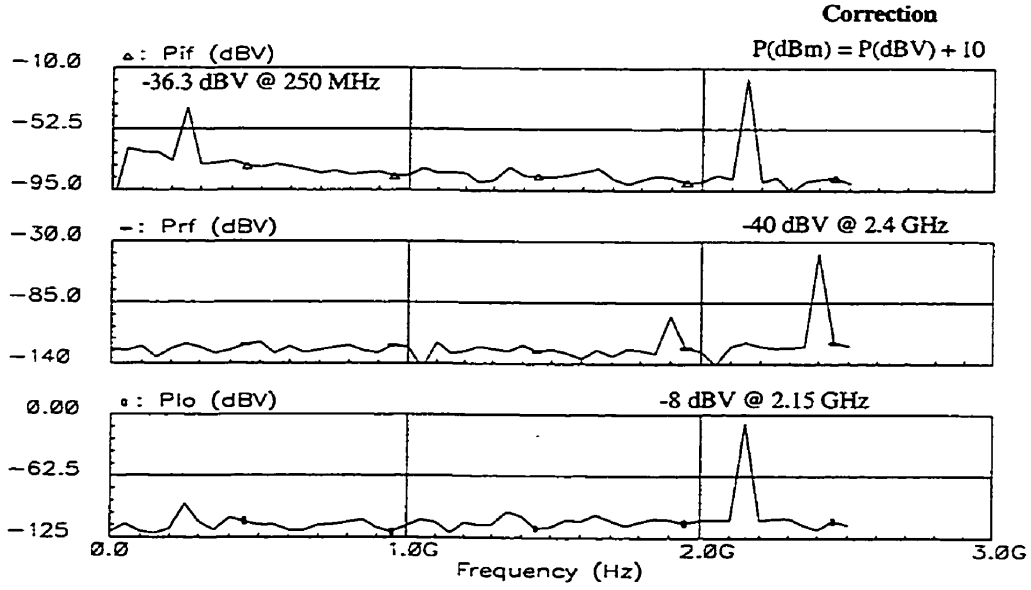

Figure 4.9: Frequency Spectrum of Single-Balanced Current-Switching Mixer

The whole design cycle can be summarized in a block diagram representation for quick reference as shown in Figure 4.10.

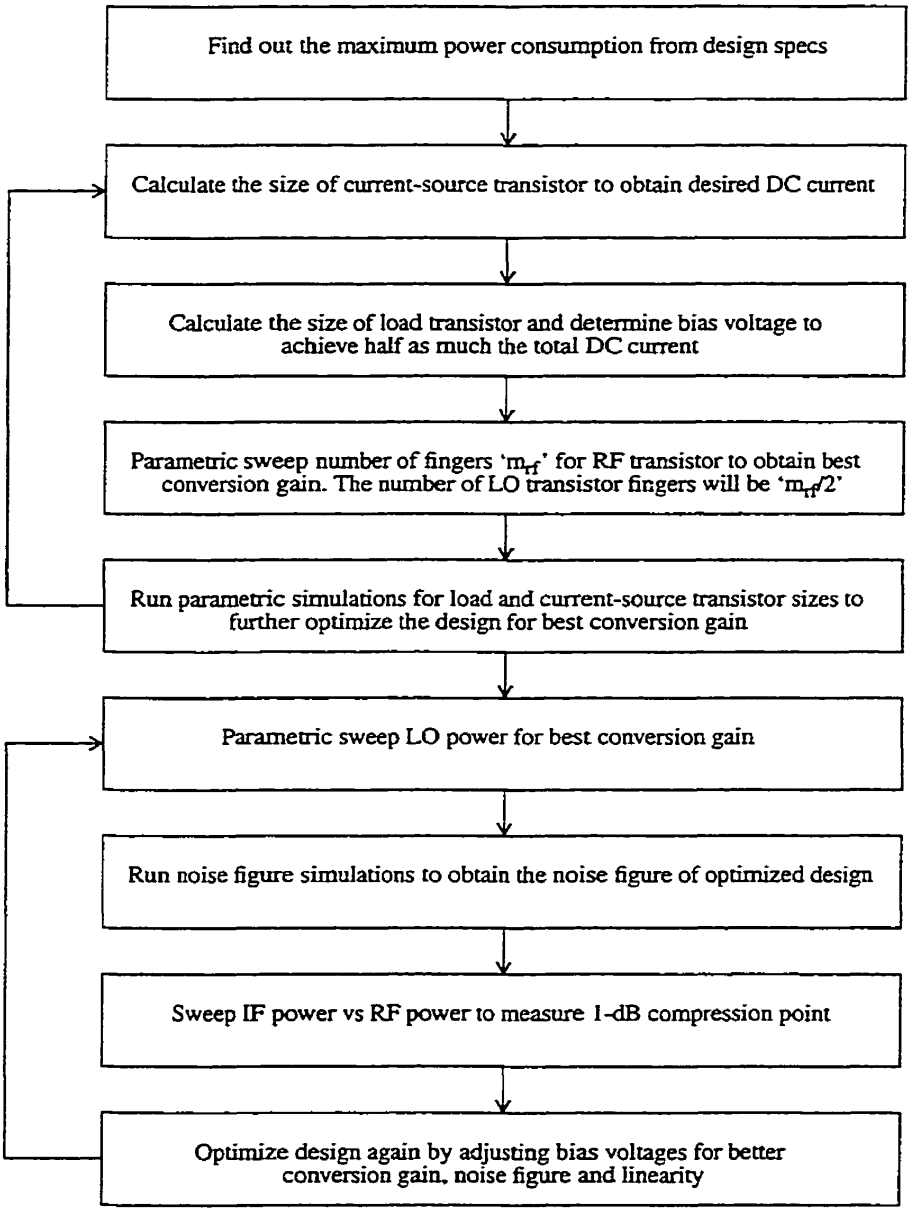

Figure 4.10: General Design Procedure for CMOS CS Mixer

4.3 Schematic and Simulations of Double-Balanced CMOS Current-Switching Mixer

As discussed earlier, double-balanced current switching mixer is a combination of two single-balanced mixers connected in parallel, therefore exactly the same configuration, shown in Figure 4.7, can be used to realize a double-balanced mixer. The complete schematic of double-balanced CMOS current-switching mixer is shown in Figure 4.11.

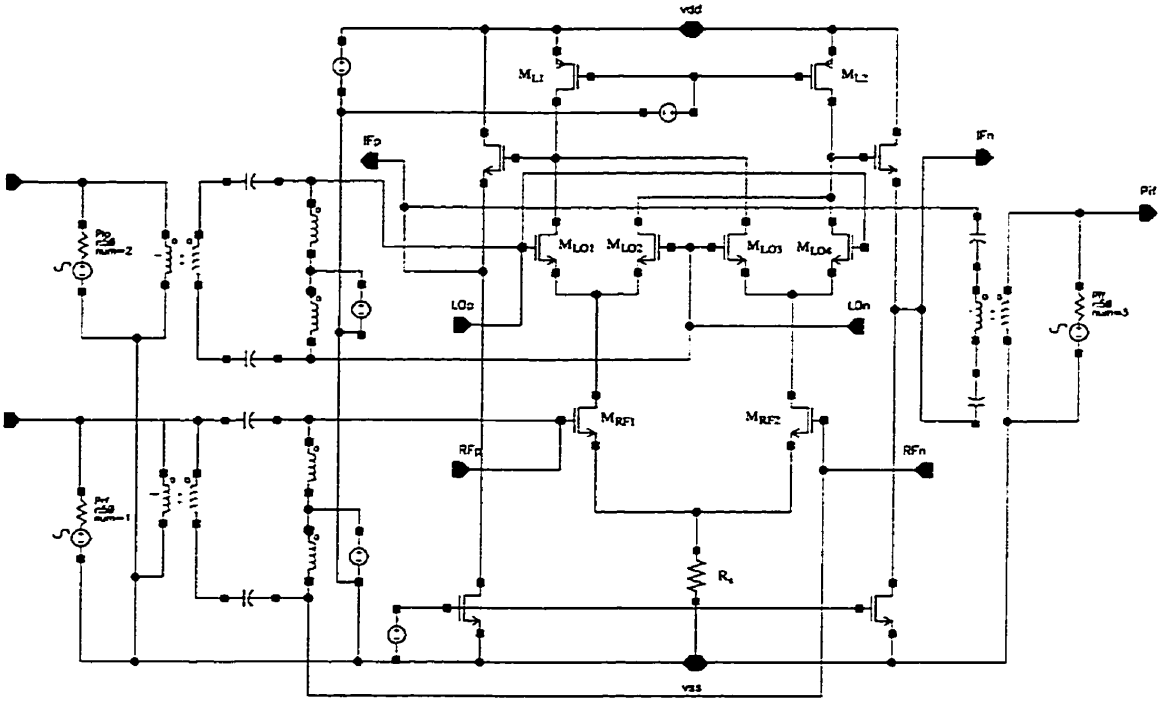

Figure 4.11: Complete Schematic of Double-Balanced Current-Switching Mixer

The only difference here is the current source, where the NMOS transistor M_s in the single-balanced structure, has been replaced by a current-source resistor R_s, whose value is chosen in such a way that the current flowing through R_s is twice as much the current

flowing through M_S. No effort, other than adjusting the bias levels, has been made to optimize the circuit because one of the purpose of this work is to compare all the balanced differential mixers with the reference single-balanced CMOS mixer.

Figure 4.12 shows the parametric simulation result of sweeping P_{LO} from -10 to 14 dBm at P_{RF} = -30 dBm to find the optimum LO power level. Figure 4.13 gives the input P_{1dB}, where again output IF power need to be corrected by adding 10 dB to the P_{IF} expressed in dBV. Figure 4.14 shows the frequency spectrum where we can observe significant improvement in LO rejection at the output although the RF spectrum still shows the presence of the image frequency due to the LO leakage at the RF port.

The double-balanced current-switching mixer shows a simulated noise figure of 8.33 dB and input P_{1dB} of -5.21 dBm.

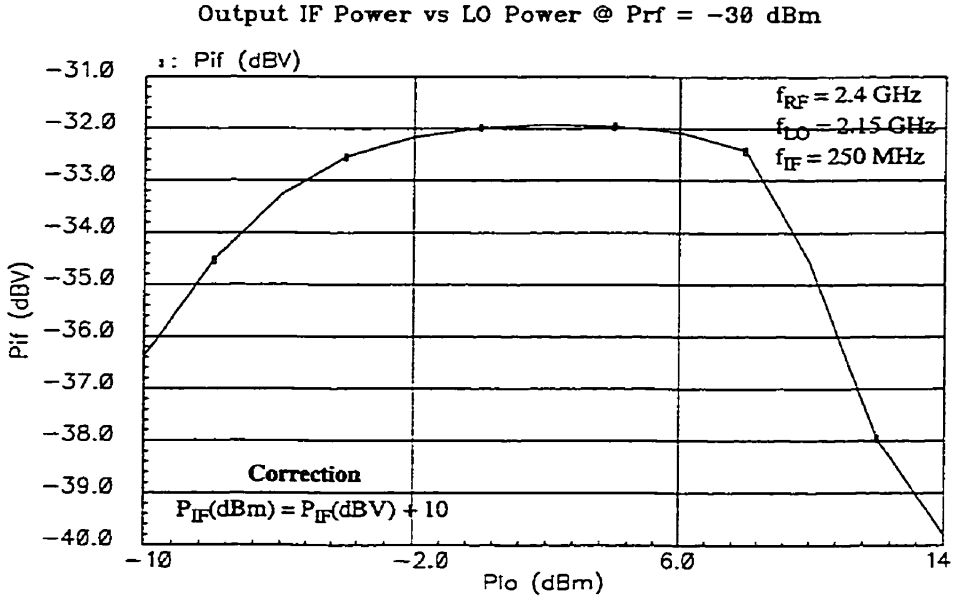

Figure 4.12: P_{IF} vs P_{LO} for Double-Balanced Current-Switching Mixer

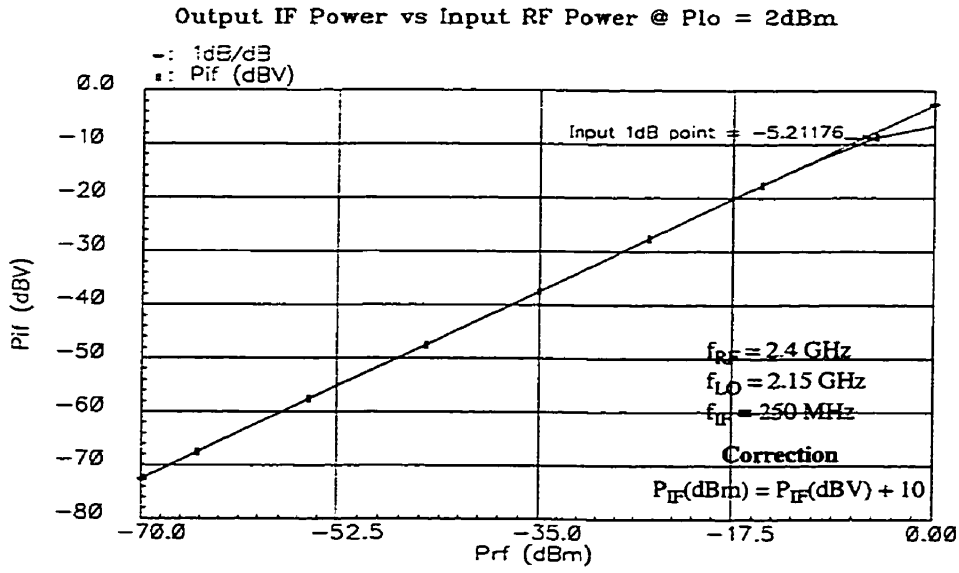

Figure 4.13: P_{IF} vs P_{RF} for Double-Balanced Current-Switching Mixer

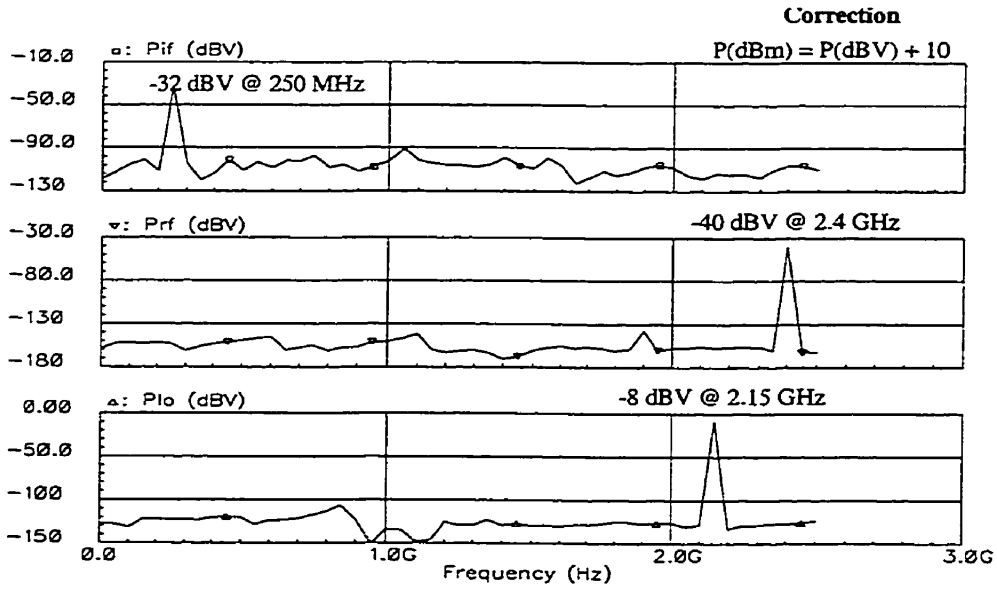

Figure 4.14: Frequency Spectrum of Double-Balanced Current-Switching Mixer

4.4 Schematic and Simulations of Single-Balanced CMOS Cascode Mixer

Although single-balanced CMOS cascode mixer represents different type of mixing operation, we can still compare it with the single-balanced current-switching mixer on the basis of major performance parameters, because of its differential structure. Figure 4.15 shows the complete working schematic of single-balanced cascode mixer, where again, only the biasing levels and LO input power are different. The current-source and the load transistors are exactly the same as for single-balanced current switching mixer. However, in this case both the RF and LO transistors have same channel width and length i.e. W = 120 μm and L = 0.24 μm, so that the current flowing through each branch is half the total current provided by the current-source transistor M_S.

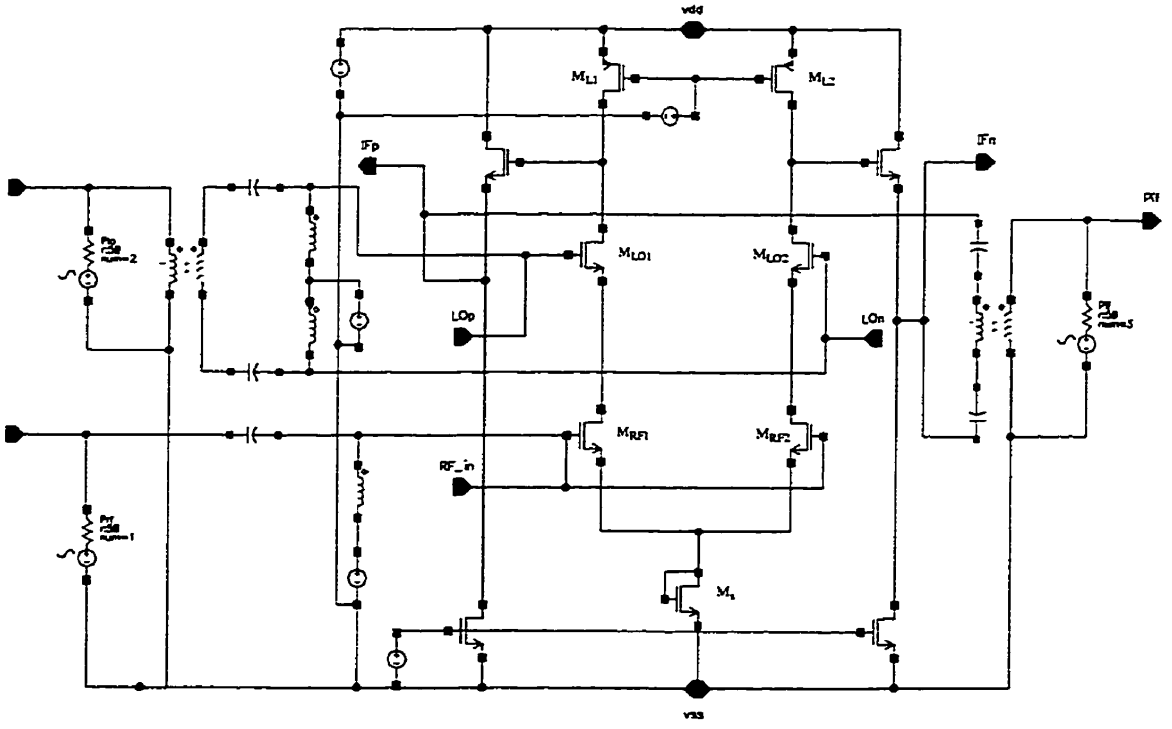

Figure 4.15: Complete Schematic of Single-Balanced Cascode Mixer

Figure 4.16 and Figure 4.17 show the simulation results of sweeping P_{LO} and P_{RF} respectively. Figure 4.18 gives the frequency spectrum of the single-balanced CMOS cascode mixer, where again we can observe the presence of LO harmonics at the output spectrum.

The single-balanced cascode mixer shows simulated noise figure of 14.5 dB and input P_{1dB} of -3.85 dBm. The improvement in input P_{1dB} is expected as the RF transistor is operating in the linear region of operation.

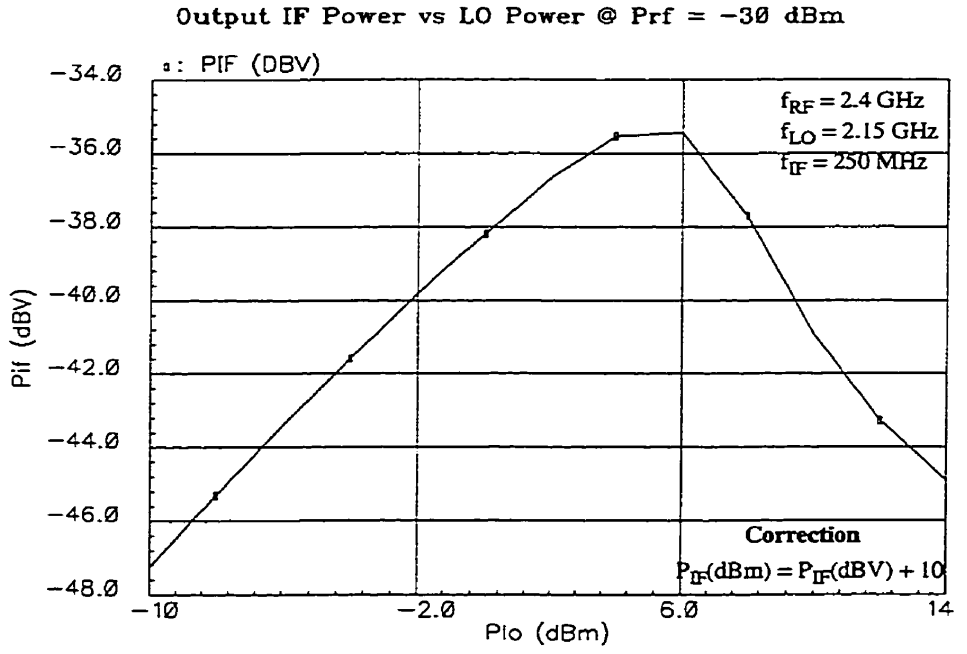

Figure 4.16: P_{IF} vs P_{LO} for Single-Balanced Cascode Mixer

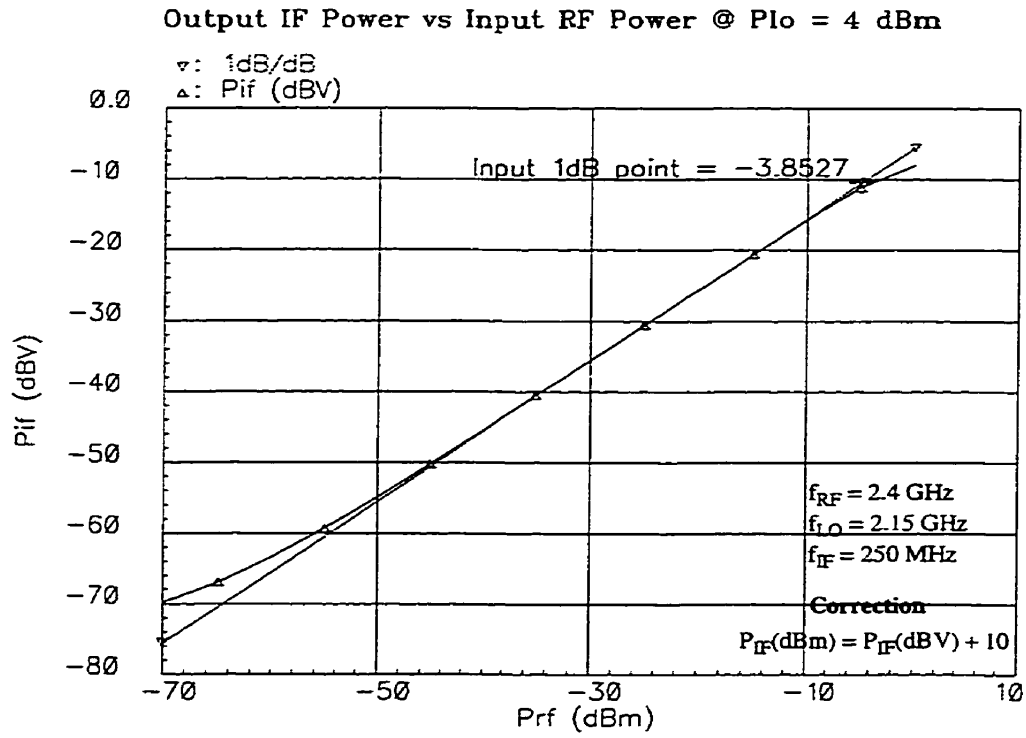

Figure 4.17: P_{IF} vs P_{RF} for Single-Balanced Cascode Mixer

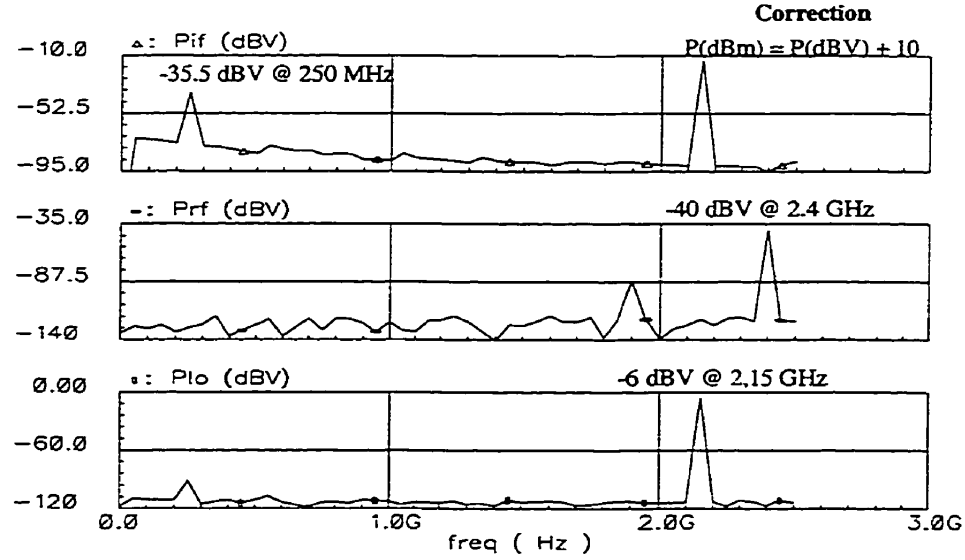

Figure 4.18: Frequency Spectrum of Single-Balanced Cascode Mixer

4.5 Schematic and Simulations of Double-Balanced CMOS Cascode Mixer

As in the case of double-balanced current-switching mixer, the only difference between double-balanced and single-balanced cascode mixers is the type of current source used. Figure 4.19 gives the complete schematic of double-balanced cascode mixer.

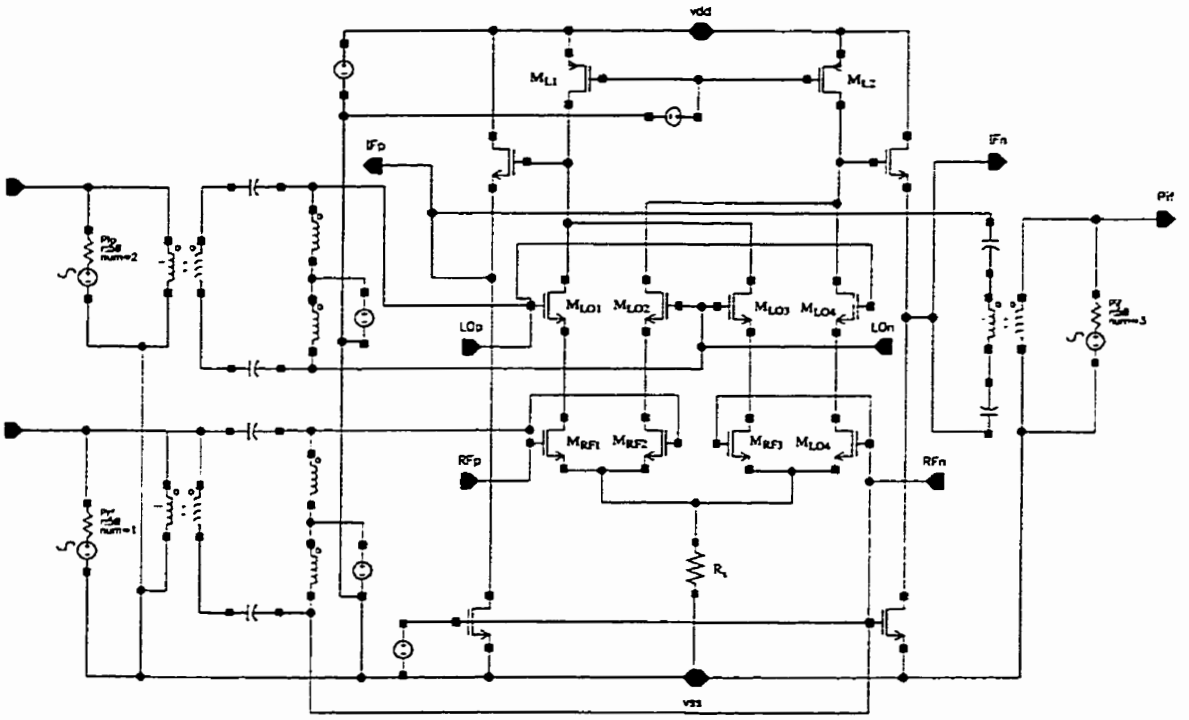

Figure 4.19: Complete Schematic of Double-Balanced Cascode Mixer

Figure 4.20, Figure 4.21 and Figure 4.22 show the swept LO power, swept RF power and the frequency spectrum of the double-balanced cascode mixer.

The double-balanced cascode mixer shows a simulated noise figure of 10.04 dB and input P_{1dB} of -5.2 dBm. Again the improvement in the input P_{1dB} is due to the linear region operation of the RF transistors and the complete rejection (ideally) of the LO harmonics at the output port (Figure 4.22).

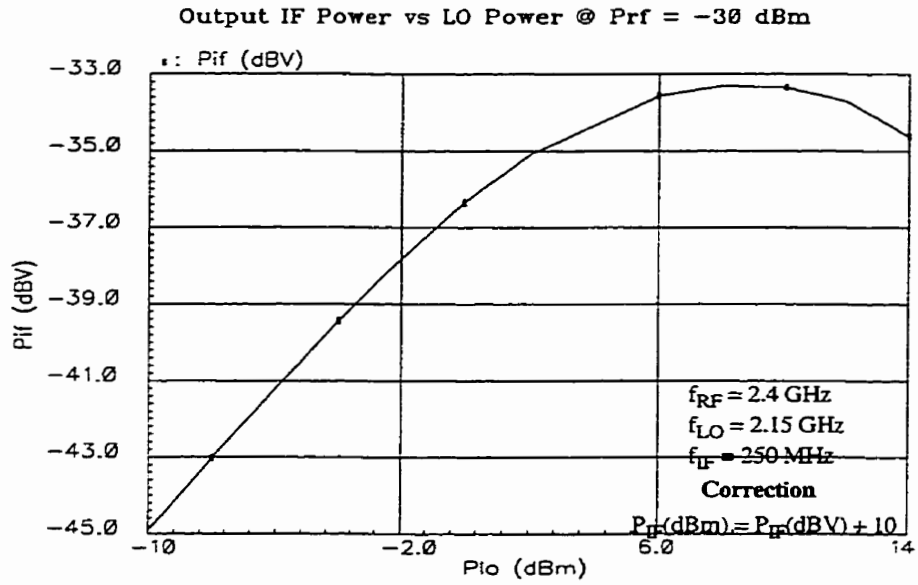

Figure 4.20: P_{IF} vs P_{LO} for Double-Balanced Cascode Mixer

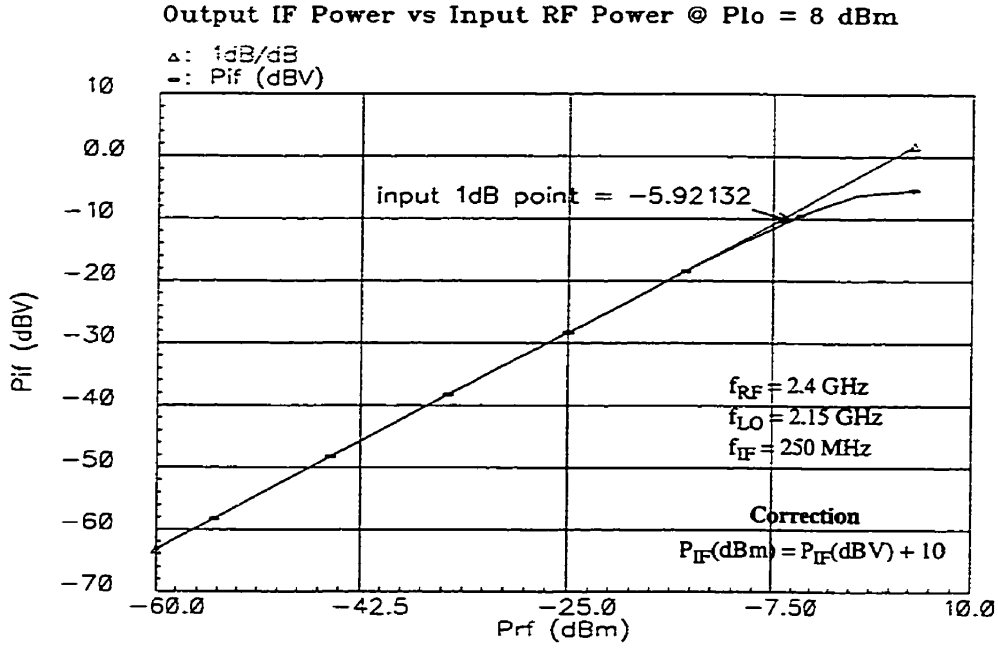

Figure 4.21: P_{IF} vs P_{RF} for Double-Balanced Cascode Mixer

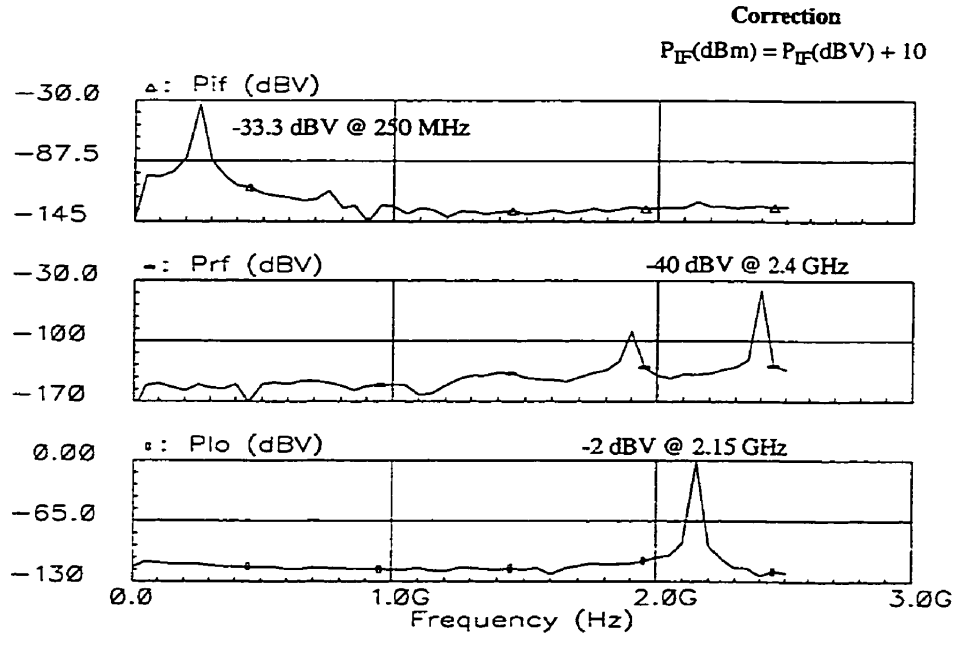

Figure 4.22: Frequency Spectrum of Double-Balanced Cascode Mixer

4.6 Design and Optimization of CMOS Single Cascode Mixer

The design methodology illustrated to design single-balanced current-switching mixer can directly be applied to design and optimize the simplest of the CMOS mixer structures i.e. the single cascode mixer. The single cascode mixer is designed in both 0.25 μm and 0.18 μm standard CMOS technologies but only 0.25 μm structure has been laid out and fabricated. The basic configuration is the same as shown in Figure 3.6.

The design and optimization of cascode mixer follows the same procedure prescribed in Section 4.2. First of all, transistor sizes have to be determined, which should be same for both RF and LO transistors, so that the common drain-source junction can be shared and the fact that same current flows through both the transistors. The complete schematic of single cascode mixer is shown in Figure 4.23.

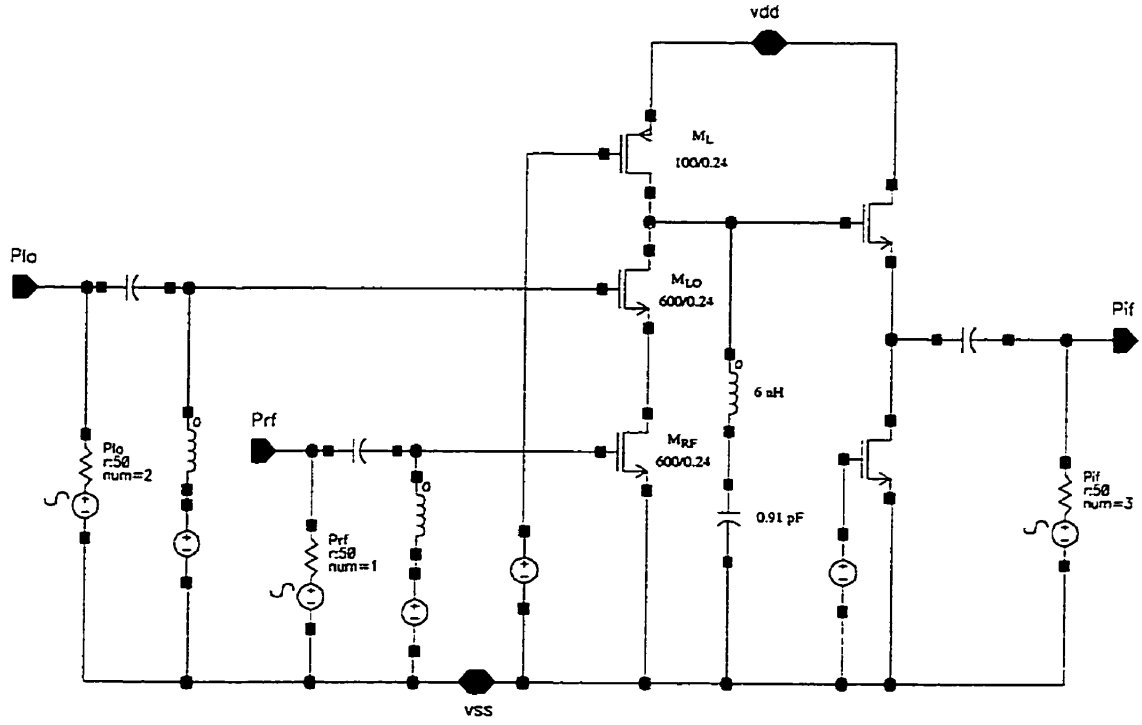

Figure 4.23: Complete Schematic of Single Cascode Mixer

As this structure is not balanced, the LO signal harmonics are not rejected at the output IF port, therefore, a passive tank circuit, tuned to LO frequency, has been connected at the output port to reject the LO frequency contents.

Setting reasonable bias levels, parametric simulations are performed, for both the mixers and simulation results are given in Figures 4.24 - 4.27 where continuous and dashed lines show the results of 0.25 μm and 0.18 μm CMOS single cascode mixers respectively. The final 0.25 μm single cascode mixer shows a noise figure of 10 dB and input P_{1dB} of -12.2 dBm. The RF, IF and LO spectrum show the presence of RF, LO and IF leakage at all the ports (Figure 4.26) due to the unbalanced nature of the single cascode mixer.

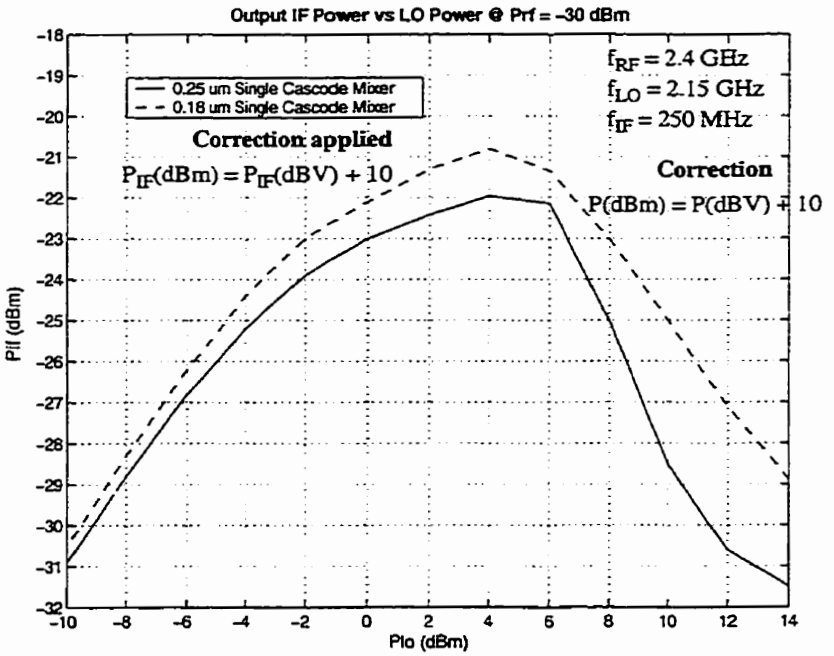

Figure 4.24: PIF vs PLO for Single Cascode Mixer

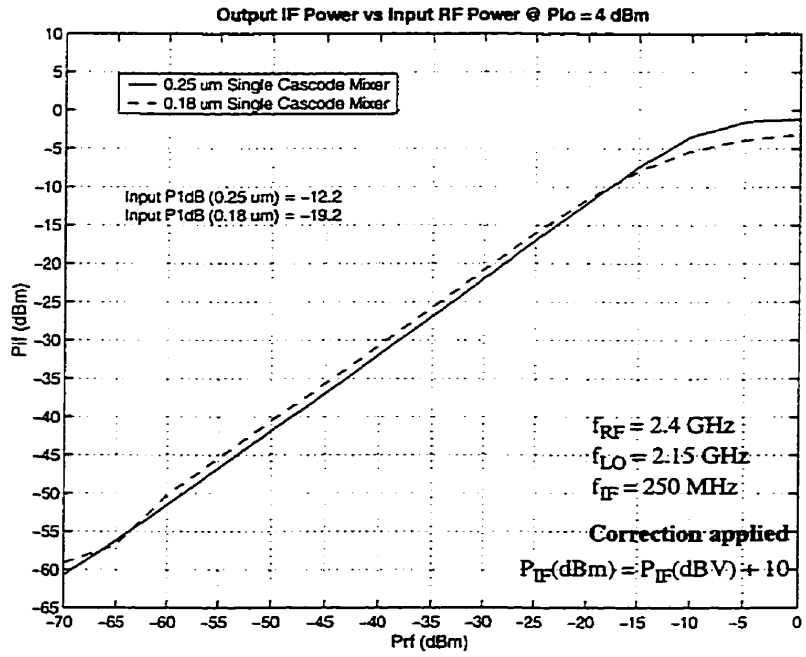

Figure 4.25: P_{IF} vs P_{RF} for Single Cascode Mixer

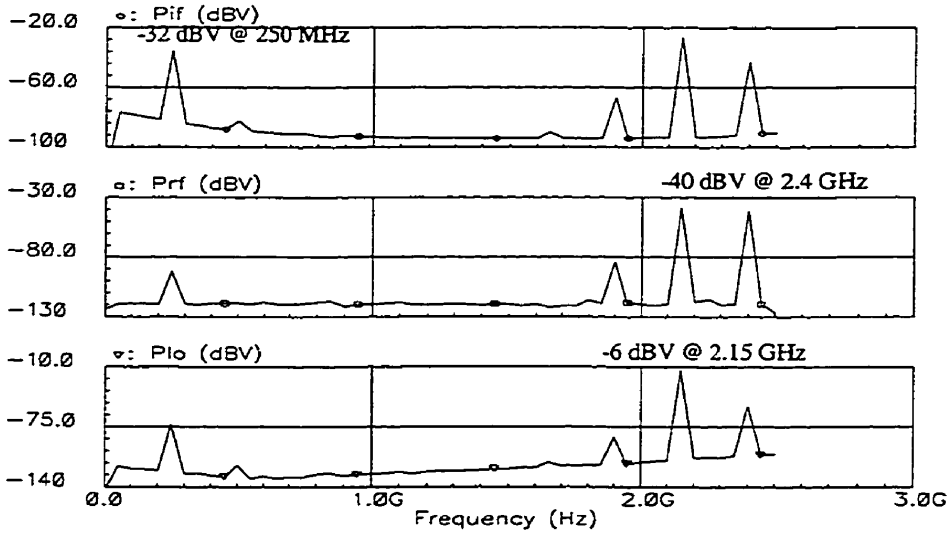

Figure 4.26: Frequency Spectrum of Single Cascode Mixer

4.7 Layout Design Issues

Layouts of all designs are done in Cadence IC design tool *Virtuoso*. "Layout versus Schematic (LVS)" has been performed for each layout to compare it with the schematic and fix any layout connectivity or size errors. Post layout simulations, with and without parasitics, are also done to confirm the functionality of the designs. Layouts for all the designs are provided in Appendix A.

Extreme care has been done while laying out balanced mixer structures to retain the symmetry of the designs. The differential signal connections to the pads are kept as much of equal length as possible to avoid any mismatch losses. De-coupling capacitors have been used to decouple power supply noise to the ground. Separate power supply and ground pads are provided for output buffers to keep their contributions in the mixer results as small as possible.

For single cascode mixer, the LO transistor source and RF transistor drain have been shared to reduce junction area and hence the capacitance of the shared junction. The LO rejection passive circuitry has been laid out using on-chip inductor and capacitor. The inductor has been designed using ASITIC (Analysis of Si Inductors and Transformers for ICs) design tool, developed by Ali M. Niknejad of University of California at Berkeley [21]. Top metal has been used to realize the inductor because of its lowest resistance and farthest distance from the substrate, which helps in reducing parasitic capacitances and resistances resulting in better quality factor Q. The simulated Q at 2.4 GHz is 4.03. The inductor has been modeled considering most of the parasitics as shown in Figure 4.27 and its layout has been provided in Appendix A.

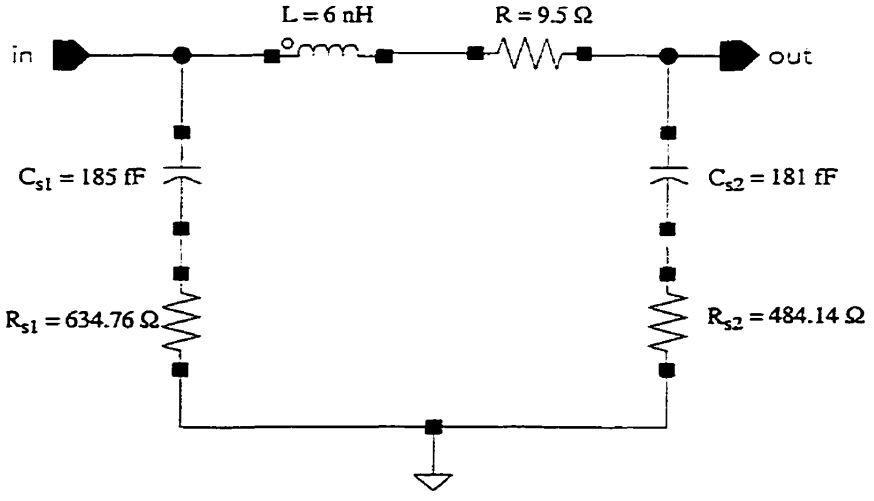

Figure 4.27: ASITIC Simulated Inductor Model for Single Cascode Mixer

The capacitor has been designed using large gate area NMOS transistor having source and drain tied together and connected to the substrate which also acts as the lower plate of the capacitor. The usual capacitance relation, shown below, has been used to estimate the area needed to realize the correct capacitance value.

$$C = \frac{\varepsilon_{ox}}{t_{ox}} A$$

where

$\varepsilon_{ox} = \varepsilon_{SiO2} \times \varepsilon_o$ = (Relative permittivity of SiO_2) × (Permittivity of free space)

t_{ox} = Thickness of gate oxide

A = Area of capacitor = W × L (W = Width of gate, L = Length of gate)

4.8 Measurement Results and Comparison with Simulations

As discussed earlier, wafer probing is employed to test the fabricated designs. Mini-Circuit power splitters/combiners are used to convert the single-ended signals into the differential signals and vice versa. DC biases are given to the circuit using Mini-Circuit bias-tees which effectively provide AC and DC blocking capabilities. The losses through the cables, power splitters/combiners, bias-tees, adapters etc. have been accounted for and adjusted in the final measurement results.

Figure 4.28 to Figure 4.37 show the measurement results in comparison to the simulated performance, where continuous and dashed lines represent measured and simulated results respectively. Figures 4.29, 4.31, 4.33, 4.35 and 4.37 show the simulation and measurement results of sweeping P_{LO} to obtain the best conversion gain. The difference in the reference input RF power P_{RF} in the simulations and measurements is due to the correction after subtracting the losses in the measurements, which is 3.3 dB for single-ended and 6.3 dB for differential input RF power at 2.4 GHz. As explained in Section 4.2, the text "correction applied" appearing in all the figures refers to a post simulation results normalization.

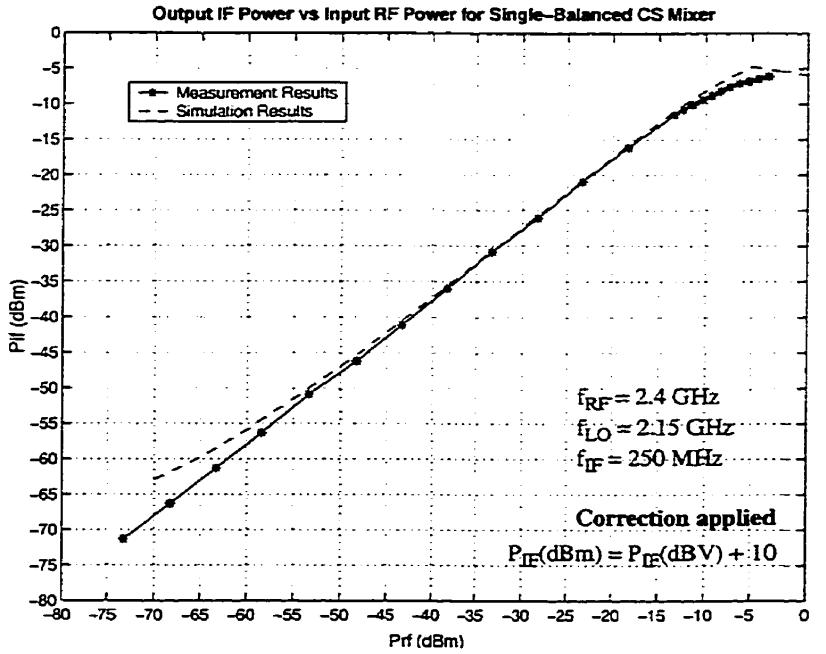

Figure 4.28: P_{IF} vs P_{RF} for Single-Balanced CS Mixer (Measured/Simulated)

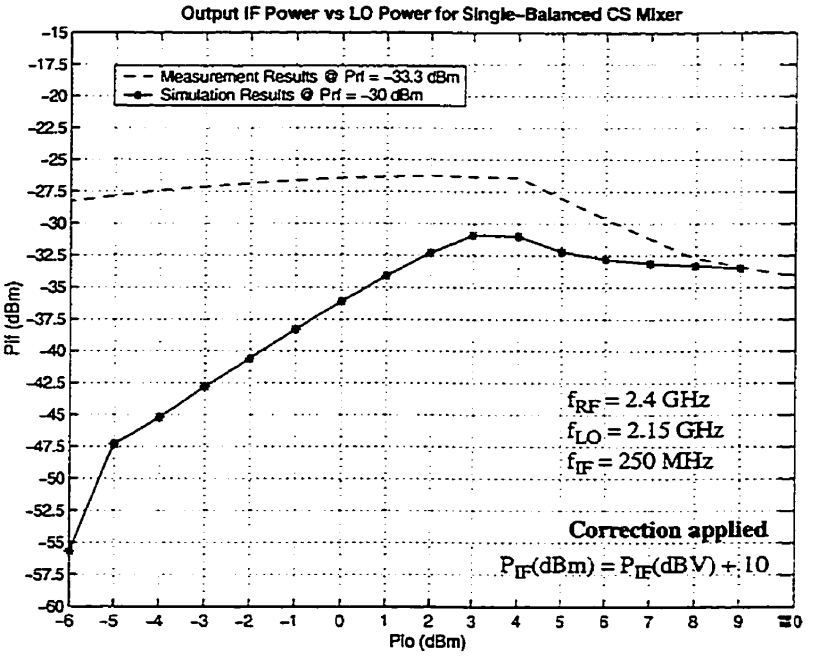

Figure 4.29: P_{IF} vs P_{LO} for Single-Balanced CS Mixer (Measured/Simulated)

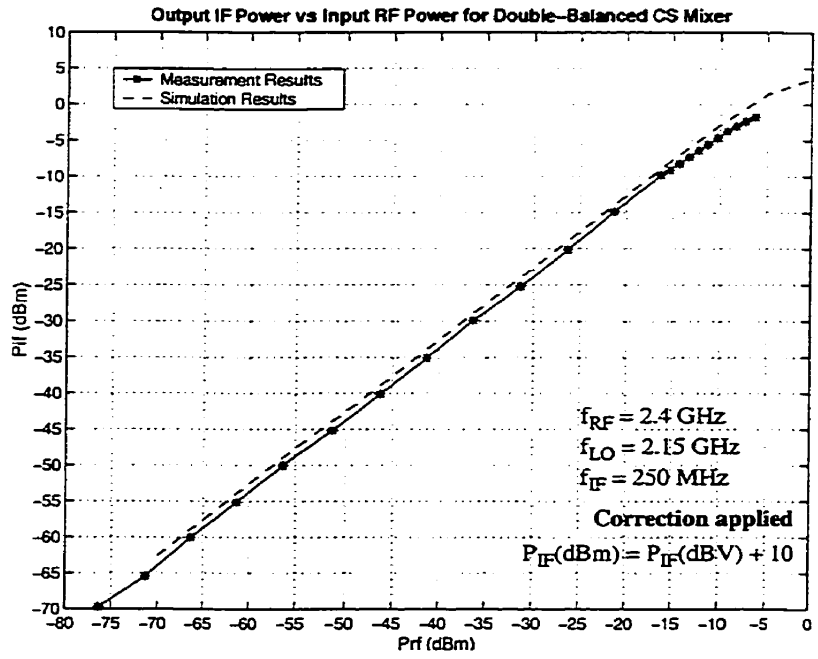

Figure 4.30: P_{IF} vs P_{RF} for Double-Balanced CS Mixer (Measured/Simulated)

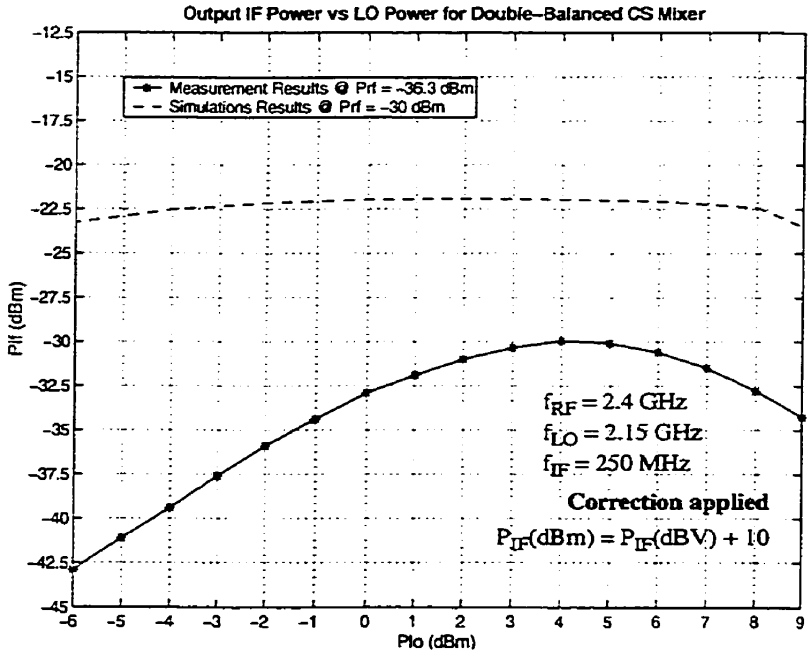

Figure 4.31: P_{IF} vs P_{LO} for Double-Balanced CS Mixer (Measured/Simulated)

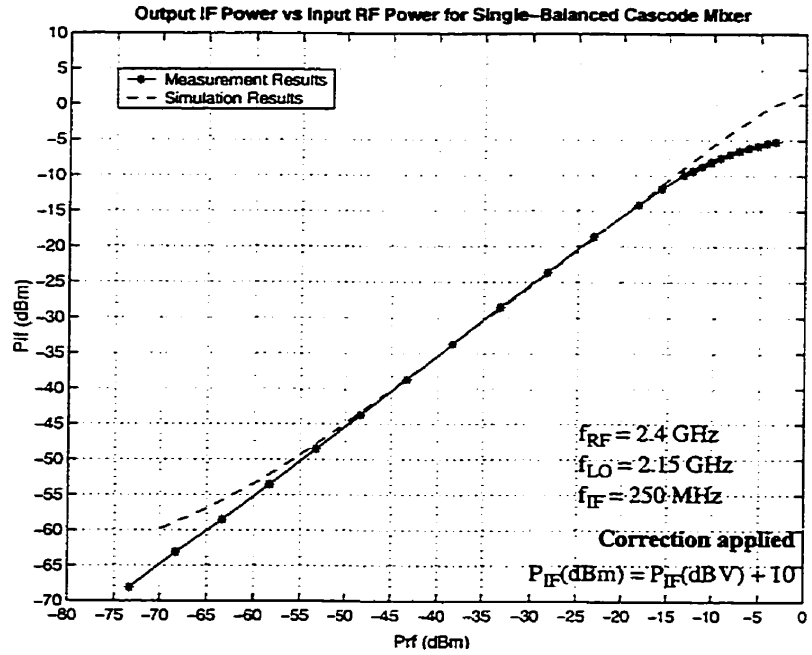

Figure 4.32: P_{IF} vs P_{RF} for Single-Balanced Cascode Mixer (Measured/Simulated)

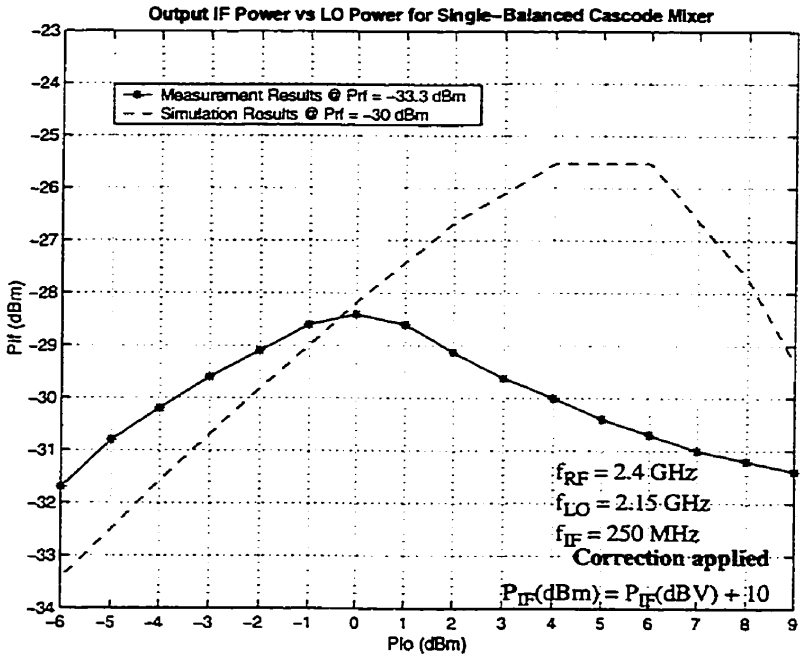

Figure 4.33: P_{IF} vs P_{LO} for Single-Balanced Cascode Mixer (Measured/Simulated)

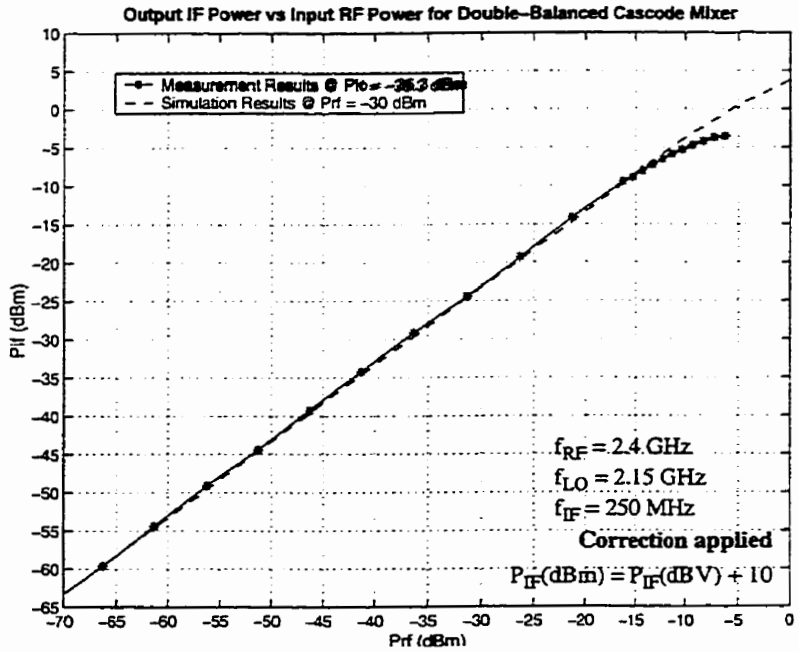

Figure 4.34: P_{IF} vs P_{RF} for Double-Balanced Cascode Mixer (Measured/Simulated)

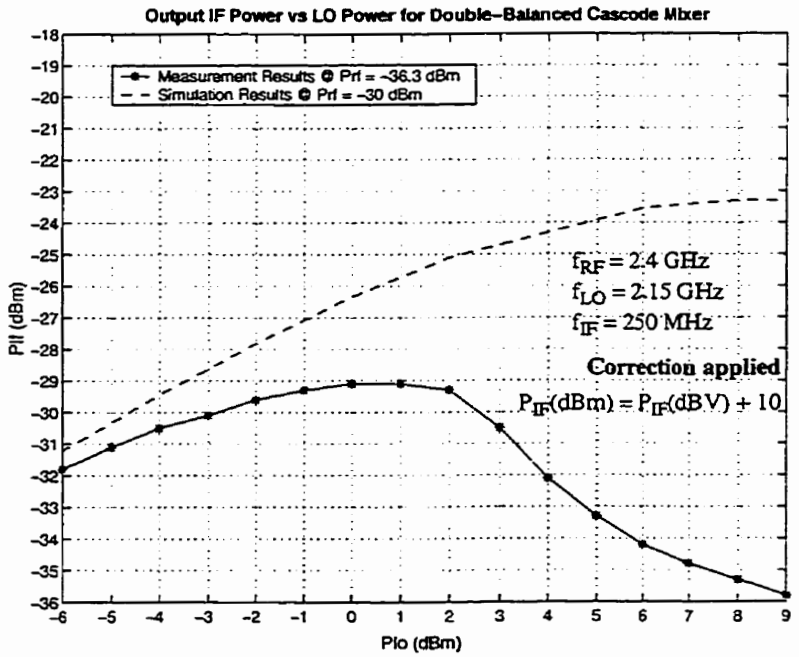

Figure 4.35: P_{IF} vs P_{LO} for Double-Balanced Cascode Mixer (Measured/Simulated)

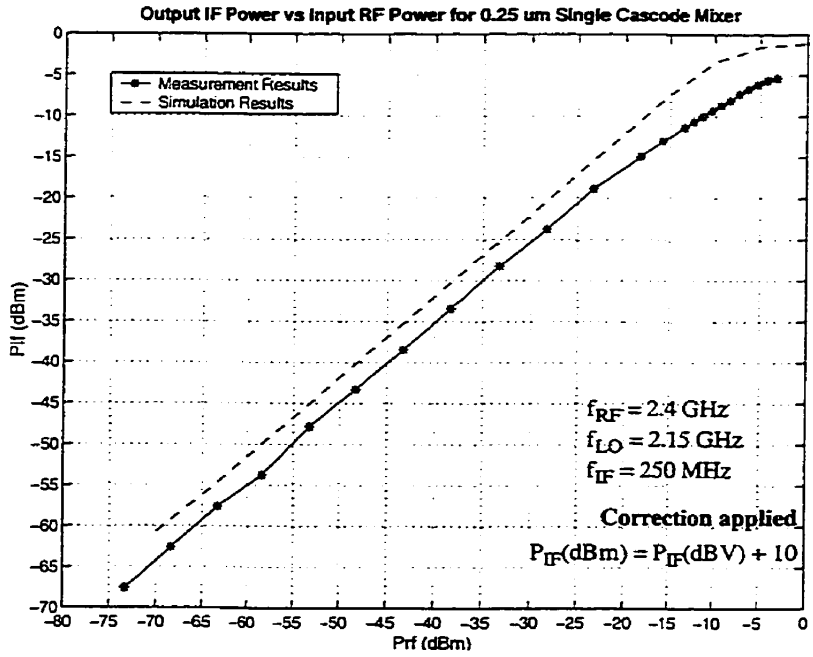

Figure 4.36: P_{IF} vs P_{RF} for Single Cascode Mixer (Measured/Simulated)

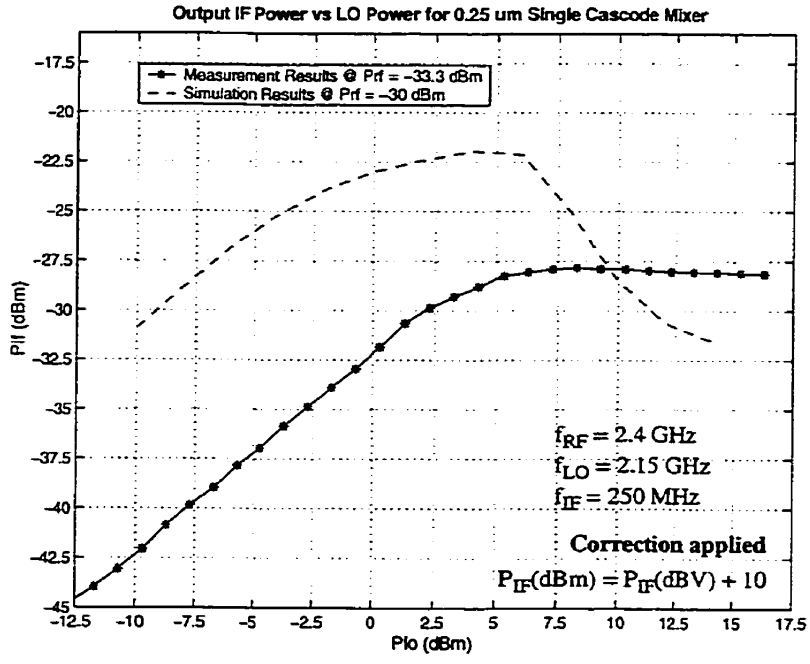

Figure 4.37: P_{IF} vs P_{LO} for Single Cascode Mixer (Measured/Simulated)

Table 4.2 gives the performance parameters in both the simulations and measurements for all the mixer structures designed in this thesis. Noise figure measurement results are not provided due to the inconsistencies in the measured results because of the non-availability of accurate noise figure measurement setup. Discussion of results and their comparison with some of the CMOS mixer structures reported in recent literature has been given in Section 4.9.

Table 4.2: CMOS Mixer Simulation and Measurement Results

Configuration of Mixer	P_{LO} (dBm)		Conversion Gain (dB)		Input 1 dB Compression Point (dBm)		Noise Figure (dB)	Mixer Current (mA)
	Sim @P_{RF}=-30dBm	Meas	Sim	Meas	Sim	Meas	Sim	Meas
Single-Balanced Current-Switching	2	4 @P_{RF}=-33.3dBm	3.8	2.4	-9	-11.3	15.62	1.32
Single-Balanced Cascode	4	0 @P_{RF}=-33.3dBm	4.5	4.7	-3.9	-14.6	14.5	1.43
Double-Balanced Current-Switching	2	4 @P_{RF}=-36.3dBm	8.1	6.1	-5.2	-8.3	8.33	2.24
Double-Balanced Cascode	8	0 @P_{RF}=-36.3dBm	6.7	6.9	-5.9	-13.3	10.04	2.18
Single Cascode (0.25 μm)	4	8 @P_{RF}=-33.3dBm	8	4.8	-12.2	-20.8	10	6.11

4.9 Discussion of Results and Comparison with Literature

In Table 4.2, simulation and measurement results of CMOS mixers are given side by side for comparison. Several interesting observations can be made on the basis of these results.

The conversion gain numbers in the measurements are generally in agreement with the simulation results except in the case of single cascode mixer where there is about 40% variation. In terms of input P_{1dB}, the comparison numbers are close when the simulated and measured LO power (both optimized for the best conversion gain) are also close e.g. in single and double balanced CS mixers. However, when the simulated and measured LO power differ significantly as in the case of all the cascode mixers, the input P_{1dB} numbers are also quite off.

If we look at the comparison of simulation and measurement results of available reported CMOS mixers in literature, we can observe the same simulation-measurement results discrepancy. This can be because of the fact that the device models in CMOS technology are optimized for the digital designs. The models, not optimized for high frequency RF design, might result in inaccuracies in the simulated values. Table 4.3 shows the simulation and measurement results comparison of few reported CMOS mixers.

Table 4.3: CMOS Mixer Simulation and Measurement Results from Literature

Reported By	P_{LO} (dBm)		Conversion Gain (dB)		Input 1 dB Compression Point (dBm)		Mixer Current (mA)
	Sim	Meas	Sim	Meas	Sim	Meas	Meas
[24]	5	5	4	0	-13	-10	10.2
[25]	-	-	5	-2.5	≈3	≈11	4.1

In terms of linearity, the double-balanced current-switching (Gilbert) mixer shows the best performance with nominal conversion gain at reasonable power consumption and LO power (4 dBm) even without much optimization in comparison to its single-balanced counterpart which was fully optimized for better conversion gain and linearity. Single and double balanced cascode structures also show some good results, however, measured performance differ from the simulations in terms of amount of LO power needed to obtain best conversion gain.

From the simulated noise figure, we can observe that, although single-balanced mixers have half the number of devices as compared to double-balanced mixers, their noise figure is still quite worse than double-balanced counterparts. The reason of this behavior comes from the fact that in double-balanced mixers, the noise introduced by the large LO signal is suppressed at the output port while in single-balanced mixers, where LO signal is not

suppressed at the output, it causes considerable increase in the total output noise power. The lower noise figure of single cascode mixer as compared to single-balanced mixers is because of its larger drain current and less number of devices used.

The input and output frequency spectrums shown in Figures 4.9, 4.14, 4.18, 4.22 and 4.26 show the presence of unwanted RF and LO harmonics at the output IF port with most harmonics present in the single-cascode mixer (even in the presence of LO rejection circuitry), and almost non-existent in double-balanced structures. It can also be observed, that only LO harmonics are present in the output spectrum of single-balanced structures while RF harmonics are rejected, as discussed in theory in Chapter 3.

Looking closely at the input RF spectrum, we can observe a harmonic at 1.9 GHz in almost all configurations. This harmonic represents the LO leakage to the input port, which again mixes down with RF signal, resulting in an image frequency term.

Table 4.4 shows the comparison of this work and some of the other CMOS mixers, reported in the recent literature.

Figures 4.38 and 4.39 give the comparison of conversion gain and input P_{1dB} against power consumption for CMOS Gilbert mixer reported in literature and this work.

Table 4.4: Comparison of Reported CMOS Mixer Designs and This Work

Reported By	Technology and Type	RF Frequency (MHz)	LO Power (dBm)	Conversion Gain (dB)	Input P_{1dB} (dBm)	Supply Voltage (V)	Current (mA)	DC Power (mW)
[4]	1 µm SB-CS	900	-	0	-	3	2.5	7.5
[22]	0.8 µm Analog Multiplier	2200	2	-1	-9	3	21	63
[23]	0.5 µm Gilbert Variant	1900	-	6	-10	1	7.5	7.5
[2]	0.5 µm Trans Mixer	900	-	8.8	-16.1	2.7	2.6	7
[10], [12]	0.8 µm Gilbert	1900	-8	6.5	-12	3	3.5	10.5
[12], [24]	0.8 µm DB-Cascode	1900	5	0	-10	3	8.8	26.4
[27], [28]	0.25 µm Gilbert	1000	-	-5	-4	2.5	6	15
This Work	0.25 µm SB-CS	2400	4	2.4	-11.3	2.5	1.32	3.3
This Work	0.25 µm SB-Cascode	2400	0	4.7	-14.6	2.5	1.43	3.6
This Work	0.25 µm Gilbert	2400	4	6.1	-8.3	2.5	2.24	5.6
This Work	0.25 µm DB-Cascode	2400	0	6.9	-13.3	2.5	2.18	5.5
This Work	0.25 µm Single Cascode	2400	8	4.8	-20.8	2.5	6.11	15.3

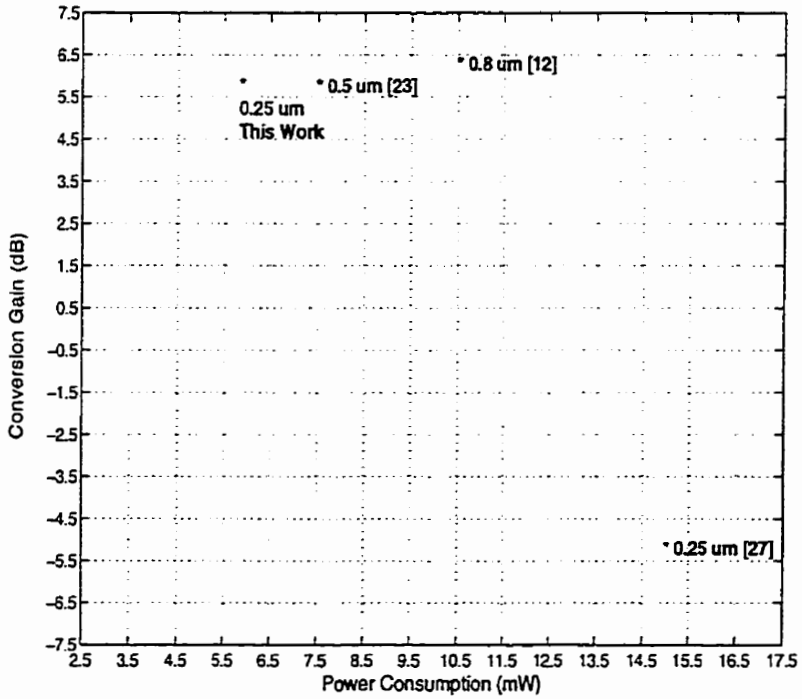

Figure 4.38: Conversion Gain vs Power Consumption of CMOS Gilbert Mixers

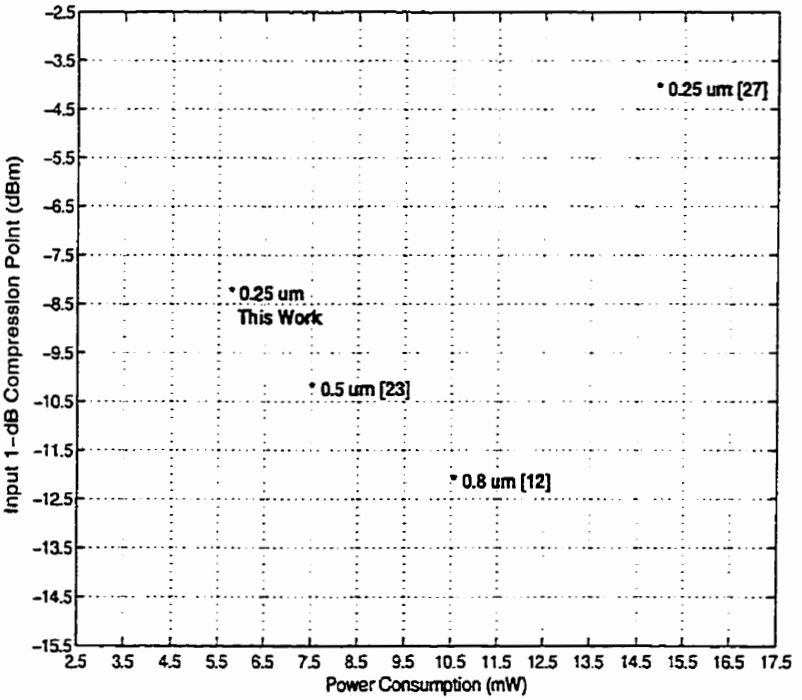

Figure 4.39: Input P_{1dB} vs Power Consumption for CMOS Gilbert Mixers

4.10 Summary

In this chapter, a comprehensive simulator based design methodology is presented which has been used to determine the major performance parameters of the fabricated CMOS mixer designs. Both the simulation and measurement results are, generally, in agreement with each other, with a few exceptions. In essence, it has been shown that *spectreRF* predicts the RF circuit behavior satisfactorily. Some of the discrepancies in the simulations and measurements, result from the CMOS device modeling problems at GHz range frequencies. New and improved MOSFET models have been proposed recently for high frequency RF applications which might help in solving these modeling problems [33].

CHAPTER 5 *Conclusions*

5.1 Thesis Summary

The thesis presents the design methodology to design and optimize 2.4 GHz CMOS RF down-conversion mixers. The choice of using CMOS technology to design RF mixers conforms to the present and future trends of evolving novel chip architectures, driving eventually towards a single-chip transceiver solution which will help in reducing the number of ICs and devices on the Printed Circuit Board (PCB). This solution will result in decreasing the cost and total power consumption of wireless products, effectively extending battery life and reliability.

Several CMOS mixers, including both differential and single-ended structures, have been investigated. The voltage conversion gain relation for each type of mixer has been derived, giving its relationship with the transistor device characteristics and dimensions. This information has been used to optimize the designs.

The single-balanced current-switching mixer has been chosen as a model design for optimization purposes. To keep the comparison as uniform as possible, all other structures are

designed using the same device sizes obtained from the optimization of single-balanced mixer. The input 1-dB compression point and noise figure of the designs have also been provided.

The simulations are performed in *spectreRF* simulation tool under Cadence environment and comparison between simulations and measurements have been provided. The comparison of designed mixer structures with few of the CMOS mixers, reported in literature, has been given to check the validity of the design methodology in terms of major performance parameters and total power consumption. The comparison with literature (Table 4.4) suggests that although designed mixer structures are working at higher frequencies, the performance numbers are still favourably comparable and in some cases better than the other reported mixer structures. This improvement in performance can be attributed to the design methodology, which offers a practical and time-saving approach towards design and implementation of RF down-conversion mixers.

In essence, this thesis contributes towards design and implementation of RF CMOS down-conversion mixers in 0.25 μm CMOS technology, by illustrating a simulator-based design methodology, with appropriate reference to the theory. This methodology can be incorporated successfully to newly emerging CMOS technologies as shown by implementing a test design in 0.18 μm CMOS technology. The methodology also helps in significantly reducing the time taken to design a major RF building block, by making efficient use of an existing simulation tool, thus satisfying a major industrial requirement of Time-to-Market (TTM) strategy.

5.2 Suggestions for Future Research

Although, all the CMOS mixer designs presented, work well under certain limits, there is, still, a lot of room for improvement. In this thesis, only the single-balanced current-switching mixer was fully optimized. The same procedure can be applied individually to other designs making full use of their circuit topologies, especially double-balanced structures, which not only provide comparable conversion gain but also help in significantly improving the dynamic range of the receivers.

In this thesis, the design optimization was done to achieve better conversion gain. This process can be modified meaningfully, by optimizing the design on the basis of better noise figure, which sometimes is regarded as more critical performance parameter for down-conversion mixers. For all the designs, degeneration inductors can be placed at the source of the input RF transistor to improve linearity.

One interesting design presented is the monolithic single cascode structure, which to author's knowledge, has been reported only in high frequency microwave applications using GaAs MESFET technology because of the difficulty in realizing small sized on-chip inductors at lower frequencies. However, as the operating frequencies are moving towards the upper microwave range applications, the values of inductors required to reject unwanted harmonics from the output of a mixer are getting smaller, providing a good opportunity of investigating this structure for those applications. While this mixer consumes more current than traditional designs, it can operate at lower voltage supplies as no current source is needed and most importantly one of the transistor is working in linear

region which requires less voltage headroom, in contrast to switching mixers, where all the transistors should remain in current-saturation.

Appendix A *Design Layouts*

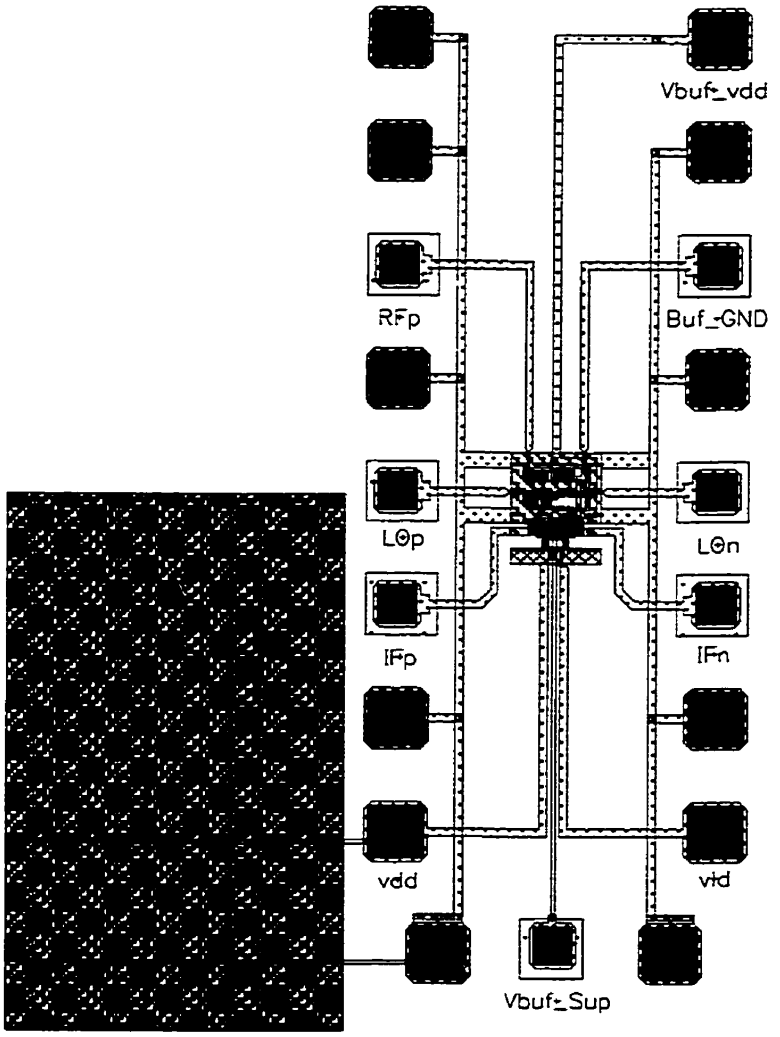

Figure A.1: Layout of Single-Balanced Current-Switching Mixer

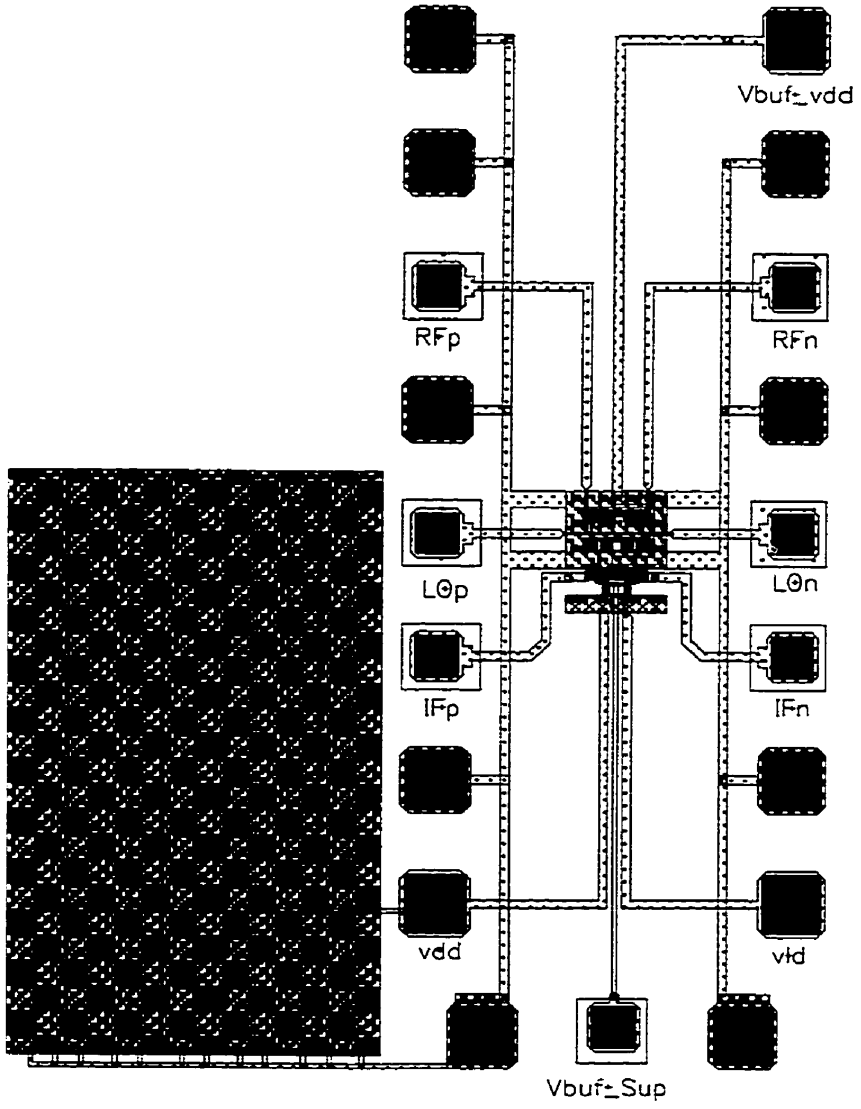

Figure A.2: Layout of Double-Balanced Current-Switching Mixer

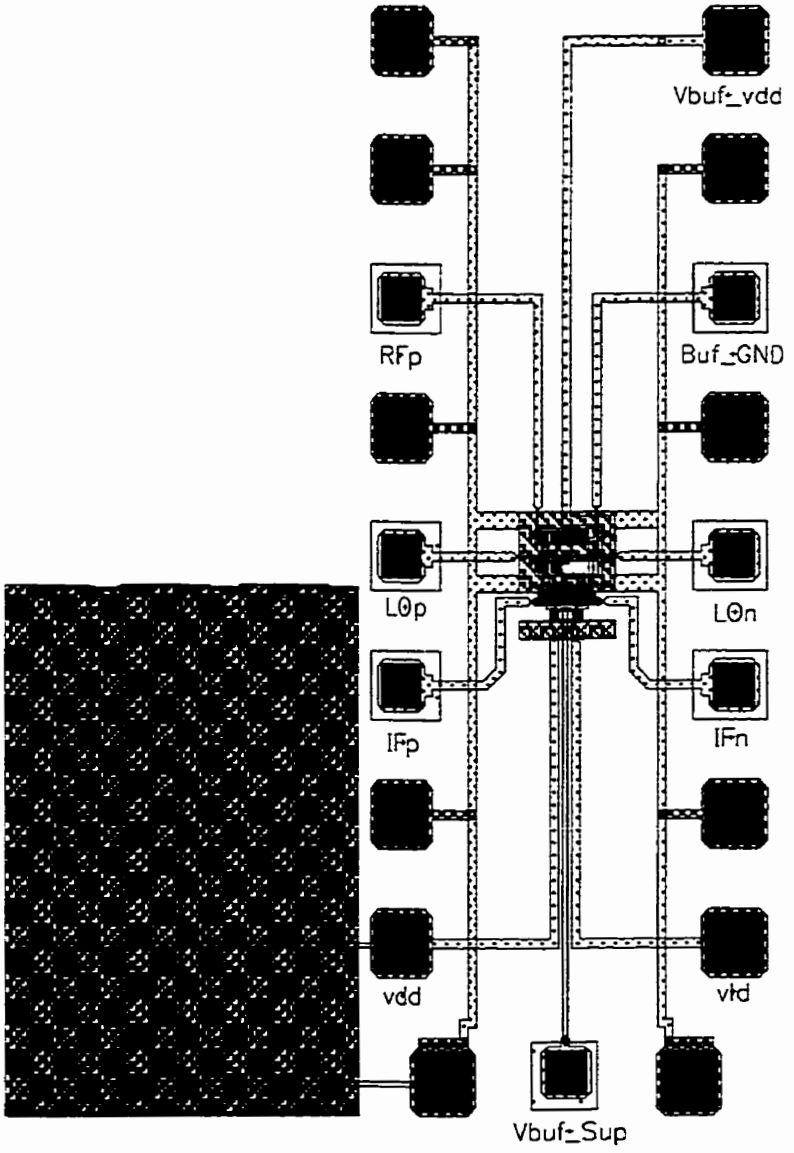

Figure A.3: Layout of Single-Balanced Cascode Mixer

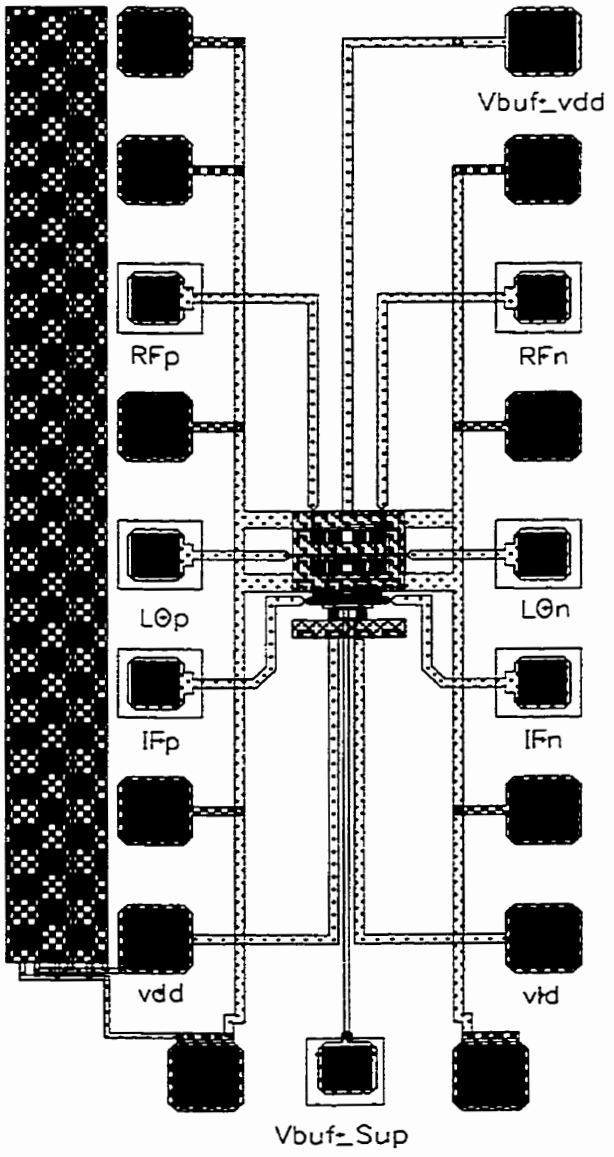

Figure A.4: Layout of Double-Balanced Cascode Mixer

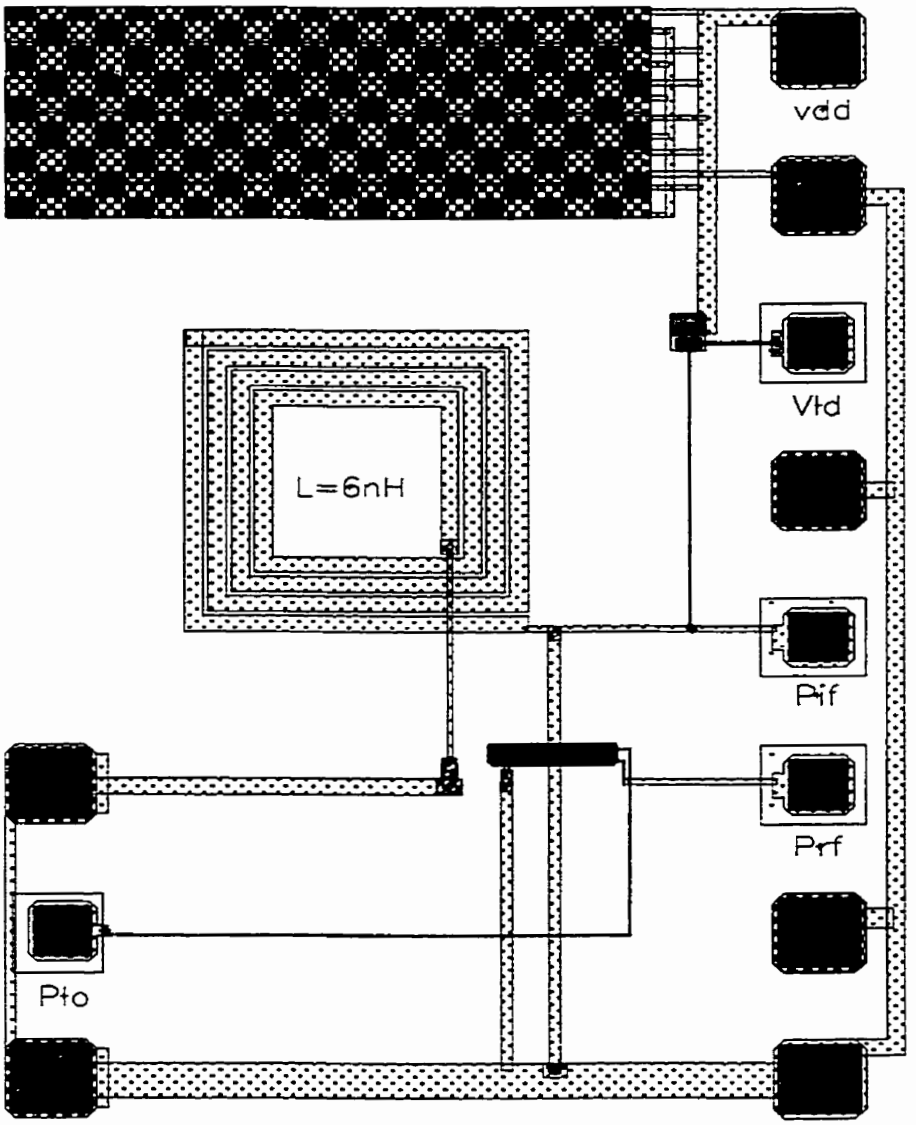

Figure A.5: Layout of Single Cascode Mixer

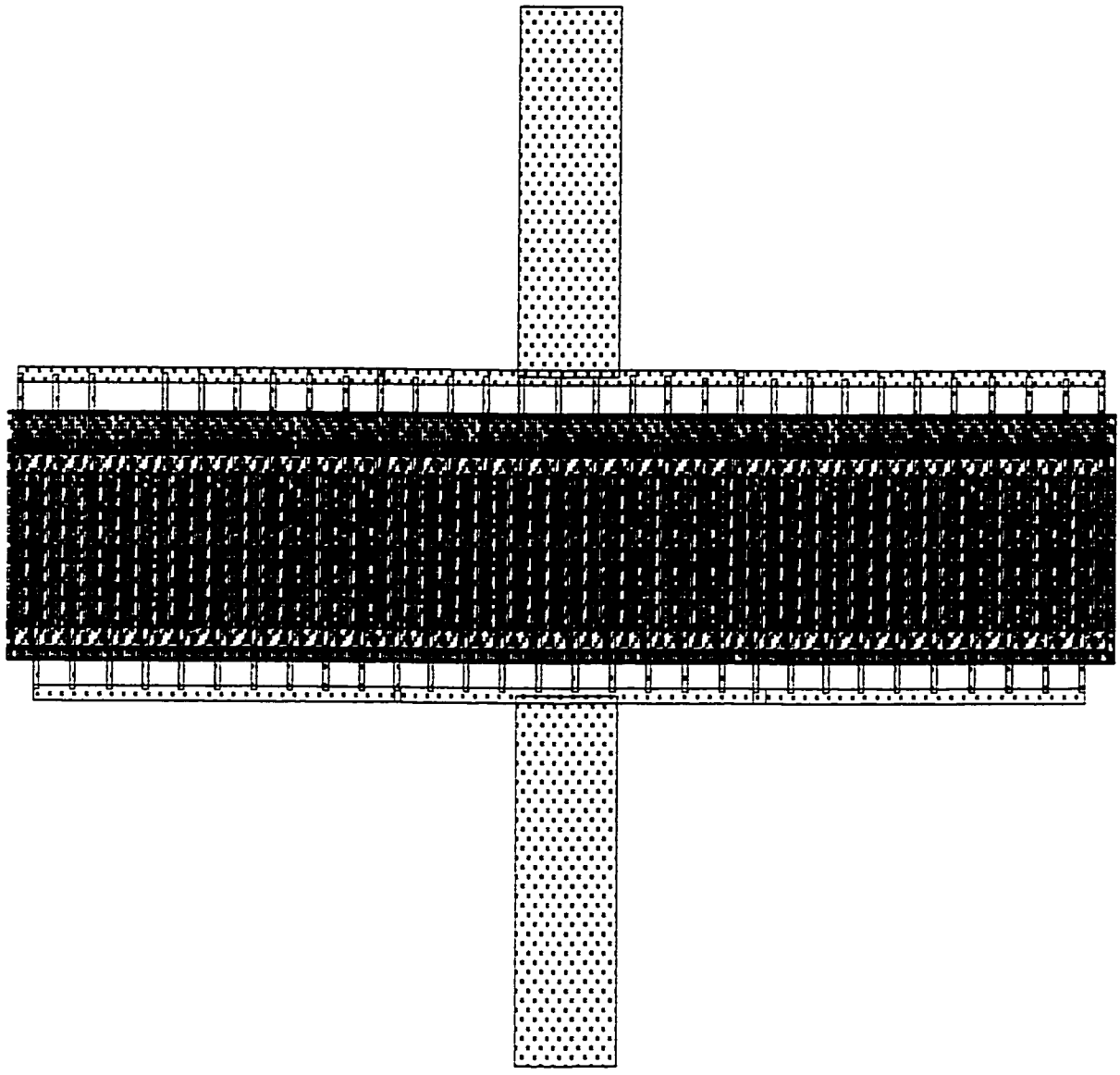

Figure A.6: Layout of Common Drain-Source Junction for Single Cascode Mixer

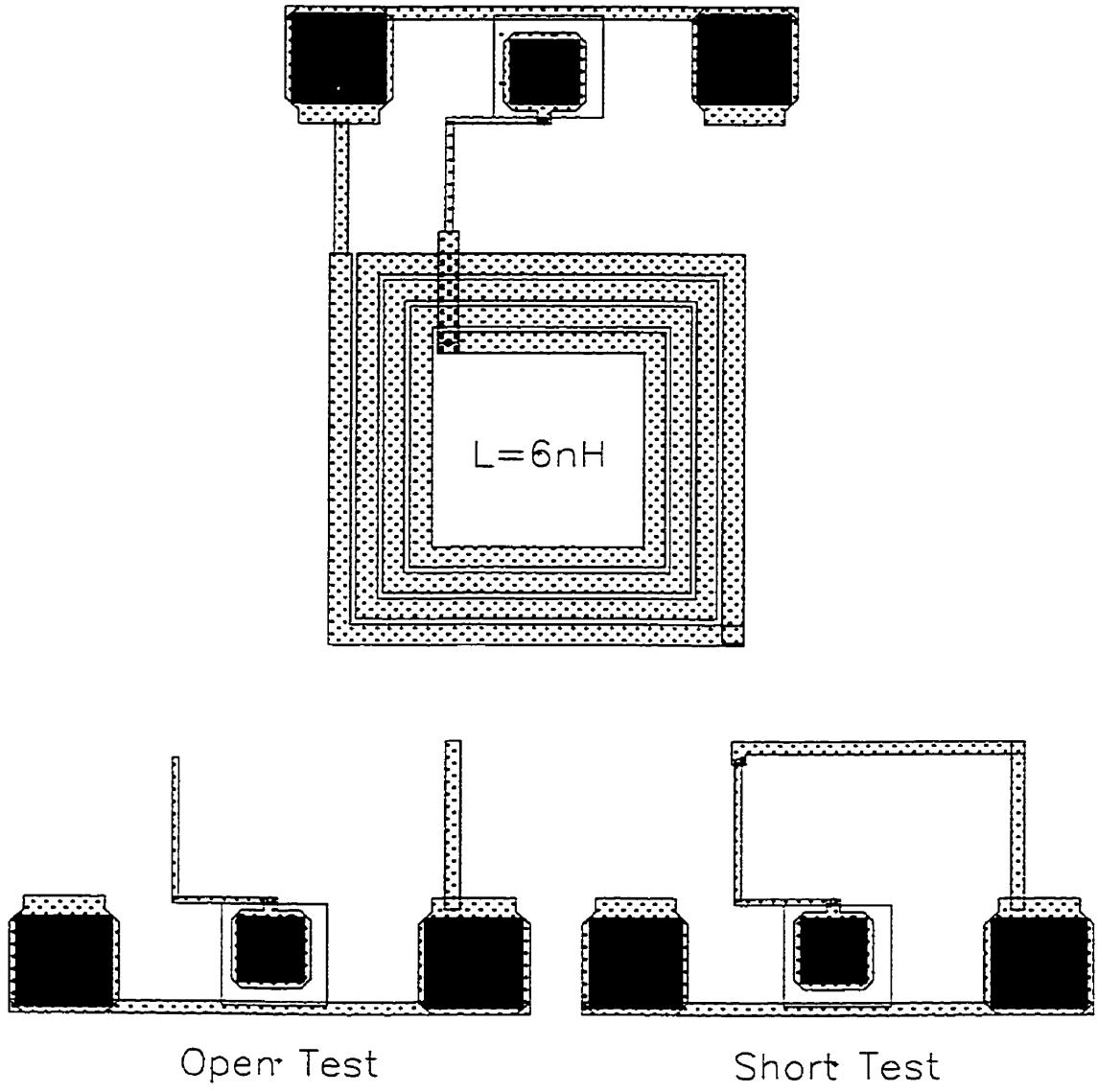

Figure A.7: Layout of Inductor with Open/Short Test Pads for Calibration

References

[1] T. Manku, "Microwave CMOS - Devices and Circuits", IEEE Custom Integrated Circuits Conference, 1998, pp. 59-66

[2] A. N. Karanicolas, "A 2.7V 900 MHz CMOS LNA and Mixer", IEEE Journal of Solid-State Circuits, vol. 31, NO. 12, Dec. 1996, pp. 1939-1944.

[3] J. Crols, M. Steyaert, "CMOS Wireless Transceiver Design", Kluwer Academic Publishers, 1997.

[4] A. A. Abidi et. al., "A Single-Chip 900 MHz Spread-Spectrum Wireless Transceiver in 1 um CMOS- Part I & II", IEEE Journal of Solid-State Circuits, vol. 33, NO. 4, April 1998, pp. 515-547.

[5] S. A. Sanielevici et. al., "A 900 MHz Transceiver Chipset for Two-Way Paging Application", IEEE International Solid-State Circuits Conference, 1998, pp. 44-45.

[6] T. Paulas et. al., "A CMOS IF Transceiver for Narrowband PCS", IEEE International Solid-State Circuits Conference, 1998, pp. 46-47.

[7] M. Steyaert et. al., "A Single-Chip CMOS Transceiver for DCS-1800 Wireless Communications", IEEE International Solid-State Circuits Conference, 1998, pp. 48-49.

[8] A. A. Abidi et. al., "The Future of CMOS Wireless Transceivers", IEEE International Solid-State Circuits Conference, 1997, pp. 118-119.

[9] C. Plett, "Radio Frequency Integrated Circuit Design", Graduate Course Notes, 1999-2000, Carleton University, Ottawa, ON, Canada.

[10] P. J. Sullivan, B. A. Xavier, W. H. Ku, "Low Voltage Performance of a Microwave CMOS Gilbert Cell Mixer", IEEE Journal of Solid-State Circuits, vol. 32, NO. 7, July 1997, pp. 1151-1155.

[11] B. Razavi, "RF Microelectronics", Prentice Hall Communications, 1997.

[12] P. J. Sullivan, W. H. Ku, "Active Doubly Balanced Mixers for CMOS RFICs", Microwave Journal, Oct. 1997, pp. 22-38.

[13] T. H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 1998.

[14] S. A. Maas, "Microwave Mixers", Artech House Inc., 1993.

[15] K. L. Fong, R. G. Meyer, "Monolithic RF Active Mixer Design", IEEE Transactions on Circuits and Systems-II, Analog and Digital Signal Processing, vol. 46, NO. 3, March 1999, pp. 231-239.

[16] M. T. Terrovitis, R. G. Meyer, "Noise in Current-Commutating CMOS Mixers", IEEE Journal of Solid-State Circuits, vol. 34, NO. 6, June 1999, pp. 772-783.

[17] S. A. Maas, "Nonlinear Microwave Circuits", Artech House Inc., 1988, Reprinted by IEEE Press, 1996.

[18] T. Manku, "Microwave CMOS- Device Physics and Design", IEEE Journal of Solid-State Circuits, vol. 34, NO. 3, March 1999, pp. 277-285.

[19] P. H. Ladbrooke, "MMIC Design- GaAs FETs and HEMTs", Artech House Inc., 1989, Chapter 8.

[20] H. Darabi, A. A. Abidi, "Noise in RF-CMOS Mixers: A Simple Physical Model", IEEE Journal of Solid-State Circuits, vol. 35, NO. 1, January 2000, pp. 15-25.

[21] A. M. Niknejad, R. G. Meyer, "Analysis, Design and Optimization of Spiral Inductors and Transformers for Si RFICs", IEEE Journal of Solid-State Circuits, vol. 33, NO. 10, Oct. 1998, pp. 1470-1481.

[22] S. Hsia, C. Wu, "A Parallel Structure for CMOS Four-Quadrant Analog Multipliers and Its Application to a 2 GHz RF Downconversion Mixer", IEEE Journal of Solid-State Circuits, vol. 33, NO. 6, June 1998, pp. 859-869.

[23] E. Abou-Allam, T. Manku, "1 V 1.9 GHz CMOS Front-End Receiver", 1998 Micro-net Annual Workshop, pp. 51-52.

[24] P. J. Sullivan, B. A. Xavier, W. H. Ku, "Doubly Balanced Dual-Gate CMOS Mixer", IEEE Journal of Solid-State Circuits, vol. 34, NO. 6, June 1999, pp. 878-881.

[25] F. Suelto, M. Conta, V. D. Torre, R. Costello, "A Low-Voltage Topology for CMOS RF Mixers", IEEE Transactions on Consumer Electronics, vol. 45, NO. 2, May 1999, pp. 299-309.

[26] P. J. Sullivan, B. A. Xavier, W. H. Ku, "A Common Source Input Cross-Coupled Quad CMOS Mixer", Analog Integrated Circuits and Signal Processing, 1999, pp. 181-188.

[27] Q. Huang F. Piazza, P. Orsatti, T. Ohguro, "The Impact of Scaling Down on CMOS RF Circuits". IEEE Journal of Solid-State Circuits, vol. 33, NO. 7, July 1998, pp. 1023-1036.

[28] Q. Huang F. Piazza, P. Orsatti, T. Ohguro, "GSM Transceiver Front-End Circuits in 0.25 um CMOS", IEEE Journal of Solid-State Circuits, vol. 34, NO. 3, March 1999, pp. 292-303.

[29] C. Tsironis, R. Meierer, R. Stahlmann, "Dual-Gate MESFET Mixers", IEEE Transaction on Microwave Theory and Techniques, vol. MTT-32, NO. 3, March 1984, pp. 248-255.

[30] M. L. de la Fuente, J. P. Pascual, E. Artal, "Analyze and Design a Cascode MESFET Mixer", Microwaves & RF, May 1998, pp. 129-138.

[31] S. Sheng, R Broderson, "Low-Power CMOS Wireless Communications - A Wide-bans CDMA System Design", Kluwer Academic Publishers, 1998.

[32] M. Niedzwiecki, M. Rasiukiewicz, "Nieliniowe elektroniczne uklady analogowe", Translated from Polish to English titled, "Nonlinear Analog Circuits", by Prof. Tad Kwasniewski, Carleton University, Ottawa, Canada

[33] C. C. Enz, Y. H. Cheng, "MOS Transistor Modeling for RF IC Design", IEEE Journal of Solid-State Circuits, vol. 35, NO. 2, February 2000, pp. 186-201.