DIFFERENTIAL TRANSMITTERS AND RECEIVERS FOR VERY HIGH FREQUENCY OPERATION IN A 0.25μM CMOS TECHNOLOGY

by

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ABSTRACT

The design of ICs for the implementation of communications standards such as Asynchronous Transfer Mode (ATM), is always pushing CMOS technologies to its operating frequency limits. As CMOS technologies progress deeper into the submicron range, the IC scale of integration and clock frequencies are increasing. Concurrently, process supply voltages are decreasing, ultimately requiring I/O circuits to be designed for lower voltages. Therefore, reliable I/O standards are needed which can meet increasing operating frequency specifications while still capable of being implemented in decreasing supply voltage environments. To meet these needs, a new group of low-voltage I/O standards using differential-mode signals have been in use over the past decade for high-frequency applications. These differential I/O circuits offer a greater frequency of operation than previously used CMOS-level I/O circuits.

This thesis offers a comparative analysis of the PECL, LVDS and GLVDS low-voltage differential I/O standards presently used in industry for high-frequency (>622Mb/s) applications. Comparisons of these differential I/O standards will be made through each stage of I/O circuit design: standard specifications, common I/O circuit topologies, simulation results, physical design and the final measured results from fabricated I/O circuits. Analysis of the advantages and disadvantages of these known I/O standards allows the proposition of a new I/O solution named the OSDS transmitter. Along with a comparison of existing differential I/O standards, a novel on-chip I/O test system for bandwidth-limited test environments is proposed.

The circuits under study were simulated, fabricated and measured, yielding strong agreement between simulated and measured circuit performances. The successful performance of the on-chip I/O test system verified each of the low-voltage differential I/O circuits to be capable of transmitting and receiving a ~1.5GHz continuous signal. Further analysis of the simulated performance, the I/O standard specifications, and the physical design for each of the I/O circuits provides a basis for comparison of each low-voltage differential I/O standard to conclude the thesis.

ACKNOWLEDGEMENTS

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1.0 Introduction

Over the past decade, the use of 5V supplies offered convenience in communications between circuits from different technologies and manufacturers [1]. However, as IC technologies progress further into the submicron range, limitations on electric field strengths have forced the reduction of circuit supply voltages to 3.3V, 2.5V and 1.8V.

The change in circuit supply voltages have added a new hurdle in interfacing ICs from different technologies. In an effort to provide the same convenience of previous 5V CMOS interfaces, but for ICs with different supplies, several new I/O standards have been introduced. This section describes previous 5V I/O schemes and their limitations, introduces the basics of new I/O standards, and summarizes the content of this thesis.

1.1 I/O on the Integrated Circuit

Typically, I/O circuits are located at the outer boundary of the IC. The transmitting and receiving circuits are often integrated with the bonding pad and a circuit for electrostatic discharge (ESD) protection [2]. Fig. 1.1 shows a schematic for a standard I/O pad.

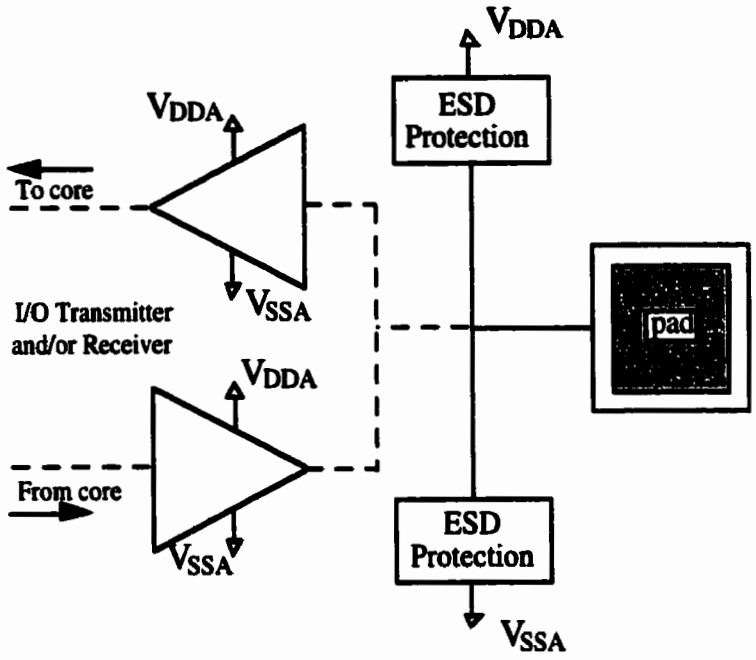

Figure 1.1: Typical I/O Pad Schematic [2]

As seen in Fig. 1.1, I/O circuits are powered from a noisy analog supply which is separated from the power supplies for the IC core logic. The rapid switching of I/O circuits can generate simultaneous switching noise on their supply buses which may cause false transitions in core logic if they shared common supplies.

The role of I/O on the IC is to either convert an input core signal to a transmitted level off-chip or to convert a signal coming on chip to core CMOS levels. For many years, IC technology was powered by 5V supplies and I/O signals were single-ended CMOS levels (0V to +5V swing). CMOS I/O levels made the design of I/O circuitry simple, as CMOS buffers could be used in both transmitting and receiving I/O signals on-chip (Fig. 1.2).

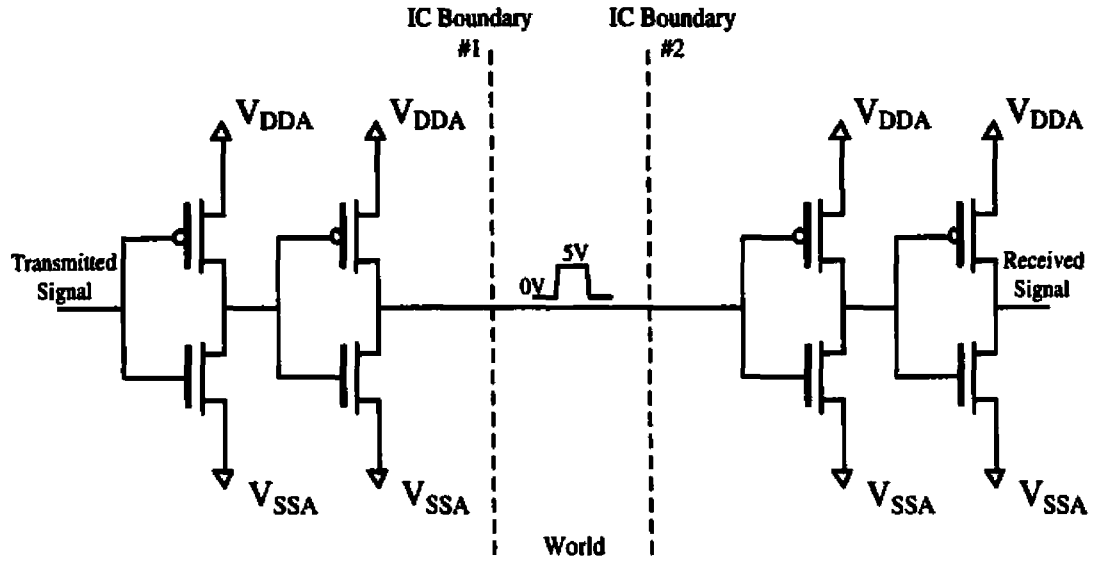

Figure 1.2: I/O Circuits for CMOS Levels

Transmitting CMOS levels also made the interfacing of several ICs on a board easier as on-board termination was unnecessary.

1.2 I/O on the Board

When designing an electronic system on a board, it is often necessary to implement board function with several interconnected ICs. To facilitate the interface of several ICs on a board, I/O standards are developed and distributed. If I/O circuits on a chip are designed to the specifications of the I/O standard, they can be interfaced with I/Os on another IC which are also designed to standard.

In lower frequency circuits, single-ended I/O standards like CMOS or TTL are commonly used. The advantages of these single-ended I/O standards are:

- One pin per I/O.

- I/Os can be directly coupled without external termination.
- Wide output voltage swing provides large noise margins.

However, in the face of advancing CMOS technologies, single-ended I/Os on CMOS ICs suffer from increasing disadvantages:

- Large signal swing limits I/O output frequency.
- Rapid signal transitions couple onto power supplies and affect other I/Os.
- Charge/discharge of I/O load consumes excessive power.

These disadvantages have become more significant as IC technologies progress, requiring I/O frequencies to increase.

1.3 Effects of Advancing IC Technology on Single-Ended I/Os

In the early 1990s, CMOS technology moved to 0.35μm feature lengths for active devices. To improve the reliability of the circuits in the 0.35μm technology, supply voltages were changed from +5V to +3.3V. The reason for the supply adjustment was to avoid rapid device degradation due to hot electron effects. Since the 0.35μm CMOS technology, the process V_{DD} has changed to +2.5V and +1.8V for 0.25μm and 0.18μm CMOS technologies respectively. This change in supplies over several technologies has made the interfacing of single-ended CMOS I/Os more problematic as supply voltages may differ from one IC to the other.

As technologies advance, so too do the clock frequencies and transistor density on the IC. The result is an increase in core logic frequency and input/output signal density. Therefore, the I/Os must be able to operate at higher frequencies to both accept higher frequency core data and multiplex several core signals into a single I/O at a time. The use of single-ended I/Os has several limitations in its frequency of operation:

- Finite slew-rate.
- Increase in power consumption.
- Increase in simultaneous switching noise (SSN).

Slew Rate Limitation

The output stage of any CMOS circuit has a constant slew-rate (SR) determined by its maximum output current, and internal and load capacitances. If the transition between voltage levels is approximated as linear (ramp), the circuit slew rate can be described as in eq. 1.1.

$$SR = \frac{V_{swing}}{t_r} \tag{1.1}$$

If we assume the SR is similar for both positive and negative voltage transitions, the maximum output frequency is inversely proportional to t_r, and therefore directly proportional to the output voltage swing.

Therefore, the large voltage swing of single-ended I/O standards limits the I/O circuit's maximum frequency of operation. As I/Os drive large output capacitances (relative to core circuit loads) which further reduce circuit SR, single-ended I/O schemes are hard-pressed to meet bandwidth requirements for high-frequency operation.

Power Consumption Limitation

A large component of power dissipated in CMOS I/Os is typically in the charge and discharge of internal and load capacitances. For a given load capacitance C, the charge/discharge power dissipated in a CMOS I/O is described by eq. 1.2 [3]:

$$SR = 2 f_{\max} V_{swing} \tag{1.2}$$

where f is the switching frequency of the circuit. According to eq. 1.2, high-frequency operation of single-ended I/Os results in excessive power consumption on the IC due to the large output voltage swing equivalent to the circuit supply voltage.

Simultaneous Switching Noise

During I/O transitions, the dynamic power consumption results in a current surge referred to as 'crowbar current' [2]. When several single-ended I/Os switch at the same time, the resultant rate of change in the net I/O crowbar current is increased. The rate of current change can be so significant that it generates an opposing voltage across parasitic inductances in the IC packaging [4]. This simultaneous switching noise (SSN) or 'ground-bounce' can couple onto static I/O outputs and generate false logic transitions at the receiving end of the I/O signals. The magnitude of the crowbar current per I/O circuit is proportional to the output voltage swing of the I/O.

1.4 Low-Voltage Swing Differential I/O Circuits

The greatest factor limiting the high-frequency operation of single-ended I/O schemes is the large output voltage swing. To increase an I/O circuit's output frequency, and reduce its power consumption and SSN, new I/O standards have been developed with low output voltage swing. A disadvantage to reducing the output voltage levels is the reduction of noise margins. Therefore, new low-voltage swing I/O standards incorporate differential outputs in an effort to increase I/O frequency and maintain adequate noise immunity. A general schematic of a differential I/O interface is shown in Fig. 1.3.

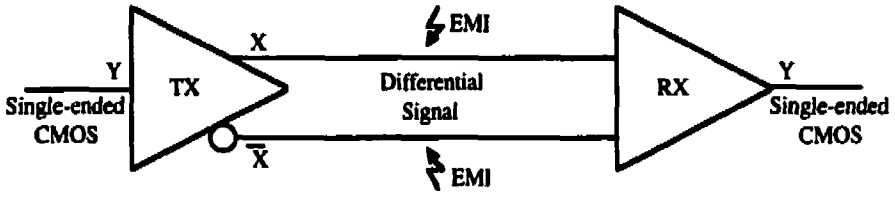

Figure 1.3: General Differential I/O Transceiver Schematic

The low output swing allows the rapid charge and discharge of load capacitances with lower crowbar currents, resulting in higher operating frequencies and less SSN than single-ended I/Os. It may seem that the lower differential output swing still will not offer as great a noise margin as single-ended I/Os. An additional amount of noise immunity is built-in to the physical nature of the differential I/O circuit. Provided that the differential output paths are physically close, any external electromagnetic interference (EMI) will couple onto both paths as a common-mode signal (Fig. 1.3). If the I/O receiver is designed with a high common-mode rejection ratio (CMRR), the coupled EMI signal will be rejected at the receiver.

Several differential I/O standards have been implemented over the past decade. Each of these I/O standards have a low output voltage swing and have been documented in literature to operate at frequencies of 622Mb/s-1.5Gb/s [1, 5, 6, 7]. However, as was the case with the original +5V CMOS I/Os, designers are looking for an I/O standard that won't be gone with the next progression in CMOS technology. An I/O standard which will stay for many years facilitates the interfacing of ICs and reduces the cost of research into new I/O circuits for every new IC process. Therefore, it would be beneficial to study existing and emerging low-voltage differential I/O standards, and to propose new solutions in this area.

1.5 Thesis Goal

This thesis offers a comparative analysis of commonly used low-voltage differential I/O standards for high-frequency (>622Mb/s) operation. Comparisons of the I/O standards will be made through each stage of I/O circuit design: standard specifications, common I/O circuit topologies, simulation results, physical design and the final measured results from fabricated I/O circuits. Analysis of the advantages and disadvantages of known differential I/O standards will allow the proposition of new I/O solutions.

This thesis also introduces a novel method of testing the high-frequency operation of I/O circuits on-chip, necessary to overcome the high-frequency limitations of ceramic packaging. Each I/O circuit's high-frequency performance will be assessed through this

novel test method and compared. The goal of this thesis will be to decide the most effective low-voltage differential I/O standard based on:

- Circuit performance – power consumption, output bandwidth.
- Process robustness – sensitivity of designs to process variation, scalability to lower supply voltages.
- Physical design – layout area, on or off-chip termination requirements, necessity for extra supply or bias pins.

The second Chapter will provide an introduction to known low-voltage differential I/O standards and their general implementation. The novel method of testing the high-frequency operation of I/O circuits in an on-chip 'I/O testbench' is presented in Chapter 3. The HSPICE simulation results of the I/O circuits under study and the I/O testbench circuits will be shown and discussed in Chapter 4. Chapter 5 presents the physical layout of the circuits chosen for fabrication in this thesis. The measured results of the fabricated I/O circuits will be given and compared with simulation results in Chapter 6. Chapter 7 summarizes the content of the thesis and concludes with an overall comparison of the I/O standards under study.

2.0 High-Speed I/O Transmitters and Receivers

Several new I/O families have been developed over the past few years which operate at supply voltages less than 5V. But the time when these I/O families will require supply voltages greater than that allowable by the CMOS technology is fast approaching. Between the accelerating evolution of IC technology and the increasing market for low-power battery operated equipment, there is motivation to design I/O standards with lower supply voltages than those dictated by the technology alone [1]. Currently, process options exist allowing higher supply voltages in the I/O areas, but these also provide a penalty in cost and performance for the IC.

The most recent types of I/O families that have been developed are predominantly low-voltage supply, differential I/O transmitters and receivers. These circuits offer low-power dissipation and high-frequency operation (> 622Mb/s) due to their low supply voltage. Several well known low-voltage differential I/O families include Pseudo- or Positive-ECL (PECL), Low-Voltage Differential Signalling (LVDS) and an Ericsson proprietary LVDS standard: Ground-Referenced-Impedance-Matched LVDS (GLVDS).

Differential I/O standards may seem counter-productive to implement on ICs which are already plagued by a shortage of package leads [1]. However, this need for more pins per signal is partially compensated by a need for less power pins to supply the I/O circuits. The low-voltage differential I/O circuits require less DC and AC current than single-ended I/Os, and therefore require less power pins to mitigate simultaneous switching noise (SSN) problems. In addition, the differential I/O circuits can be designed with

bandwidth substantially higher than that of the core circuitry. This allows the multiplexing of several signals into the I/O circuits to further reduce I/O pin counts. A comparison of the output voltage swing and common-mode voltage of several differential I/O circuits is shown in Fig. 2.1.

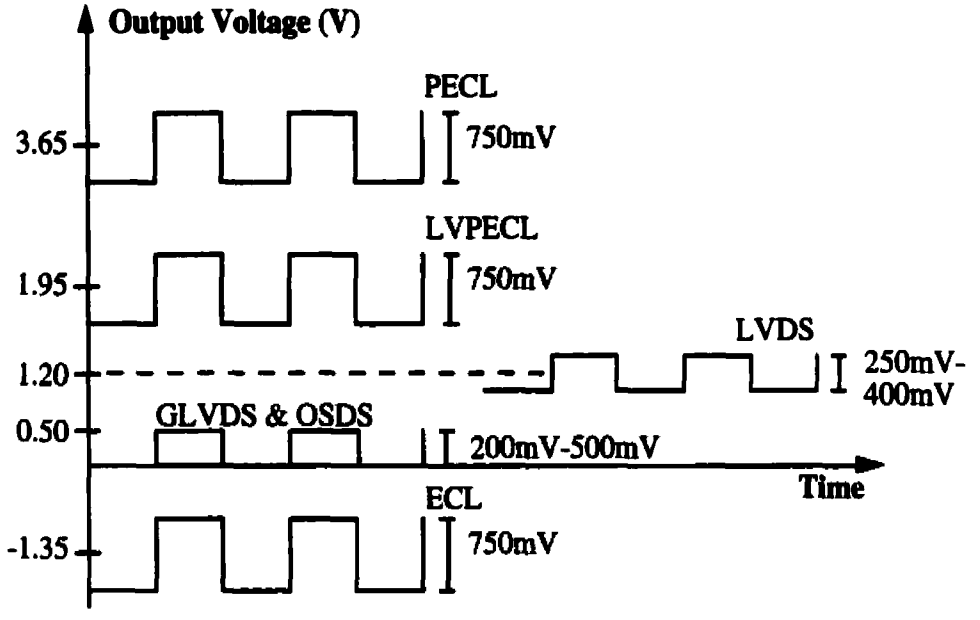

Figure 2.1: Relative AC and DC Voltage Comparison of ECL and LVDS Standards

In this section, the I/O circuit families which will be focused upon are PECL, LVDS and GLVDS. A novel I/O transmitter design named Open Source Differential Signaling (OSDS) which adheres to the GLVDS transmitter output levels will also be presented. Each I/O family's voltage standards and general transmitter/receiver circuit schematics will be discussed.

2.1 The PECL I/O Family

There are several groups within the PECL family of I/O circuits. These groups have been named PECL (V_{DD} = +5V) and Low-Voltage PECL (LVPECL, V_{DD} = +3.3V) [5]. For the purpose of this thesis I will refer to all groups within this I/O family as PECL and denote the level of V_{DD} for the specific technology. A quantitative comparison of the voltage levels for the original bipolar ECL standard and the PECL (V_{DD} = +5V and +3.3V) standards is given in Table 2-1 [5].

Table 2-1: Quantitative Comparison of ECL I/O Standards [5]

Symbol	Parameter	LVPECL	PECL	ECL	Unit
V_{CC}		+3.3	+5.0	GND	V
V_{EE}		GND	GND	-5.2, -4.5, -3.3	V
V_{OH}	Min. Output HIGH Level	2.275	3.975	-1.030	V
V_{OH}	Typical Output HIGH Level	2.345	4.045	-0.955	V
V_{OH}	Max. Output HIGH Level	2.420	4.120	-0.880	V
V_{OL}	Min. Output LOW Level	1.490	3.190	-1.810	V
V_{OL}	Typical Output LOW Level	1.595	3.295	-1.705	V
VOL	Max. Output LOW Level	1.680	3.380	-1.620	V

In the original +5V PECL standard, the output levels are differential with a 750mV swing on a 3.65V offset. For all PECL standards, the offset level scales down 1:1 with VDD but the output swing remains constant at 750mV. This standard yields the output values in Table 2-2 for a VDD = +2.5V and +1.8V PECL I/O. Table 2-2 displays the inevitable obsolescence of the PECL standard as CMOS technologies progress from VDD = +2.5V (0.25μm CMOS) to VDD = +1.8V (0.18μm CMOS). As core supplies are reduced with changing CMOS technology, PECL I/O circuits are forced to retain +3.3V and +2.5V supplies which increases both package pin count and total power dissipated in the IC.

Therefore, even the new low-voltage differential I/O circuits must eventually be replaced with lower voltage I/Os, as was the case for their +5V predecessors.

Table 2-2: PECL Standard Required Output Levels for VDD = +2.5V and +1.8V

Symbol	Parameter	LVPECL	LVPECL	Unit
VCC		+2.5V	+1.8V	V
VEE		GND	GND	V
VOH	Min. Output HIGH Level	1475	775	mV
VOH	Typical Output HIGH Level	1545	845	mV
VOH	Max. Output HIGH Level	1620	920	mV
VOL	Min. Output LOW Level	690	< 0	mV
VOL	Typical Output LOW Level	795	95	mV
VOL	Max. Output LOW Level	880	180	mV

2.1.1 The PECL Transmitter Circuit

The PECL transmitter circuit is an open-drain circuit and therefore requires output termination as illustrated in Fig. 2.2. The termination is composed of two resistors RT which match the characteristic impedance of the output transmission line. As the PECL transmitter's output current is 'steered' from one output to the other during switching, the resistors RT and the output current determine the output differential swing. The third common-mode resistor Rtc and the PECL output current determine the value of VOH (eq. 2.1). Sometimes an active pull-up circuit is placed at the transmitting end to compensate for the delay of the passive pull-up at the receiving end [6]. The common-mode capacitor CTC is placed in the termination network to smooth out receiver-end voltage spikes due to output switching noise.

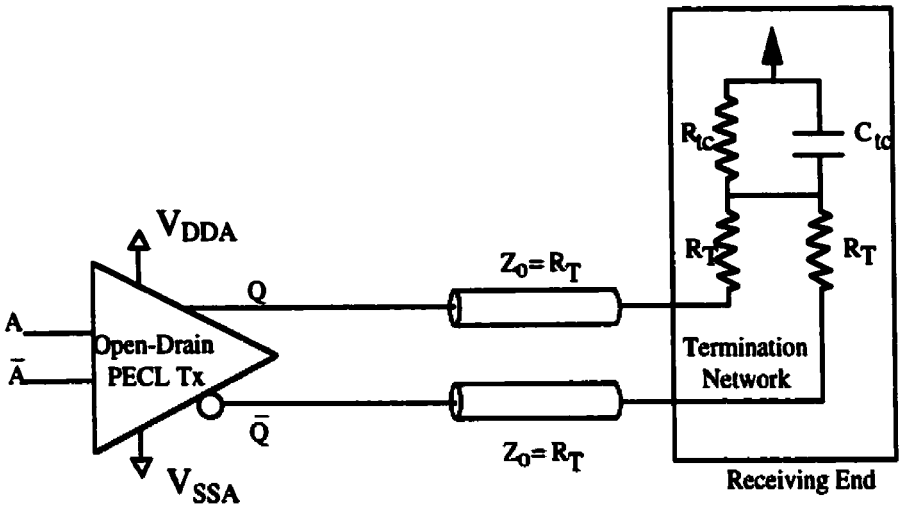

Figure 2.2: Schematic of PECL Transmitter and Termination at Receiving End [6]

$$R_{tc} = \frac{V_{DD} - V_H}{V_H - V_L} \cdot R_T \tag{2.1}$$

The V_{DD} = +3.3V PECL circuits have been reported in literature to operate asynchronously at frequencies of 1.24 Gb/s [6] for circuits fabricated in a 0.35μm CMOS technology. It is expected that VDD = +2.5V PECL circuits with the same topology fabricated in a 0.25μm CMOS technology will operate at the same bit rate and higher.

2.1.2 The PECL Receiver Circuit

As the PECL signalling has a low-voltage swing and is differential, a simple open-loop differential amplifier is all that is needed to convert the PECL signals back to single-ended CMOS. Each input of the amplifier is connected between each transmission line and its terminating resistor RT, as seen in Fig. 2.3.

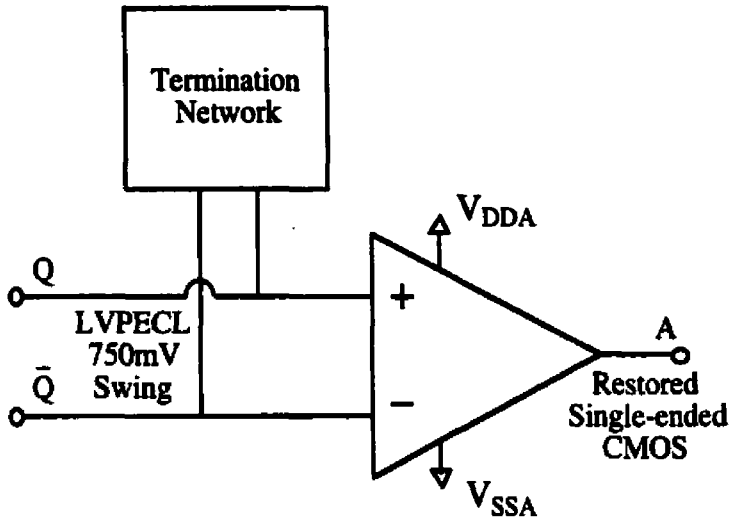

Figure 2.3: Connection of the PECL Receiver to the Termination Network

The major requirement for the PECL receiver is a high CMRR in the common mode output voltage range of the transmitter. A large amount of differential input sensitivity (proportional to its open-loop gain) is also necessary for the PECL receiver. However, the relatively large output swing of the PECL standard makes sensitivity less of an issue than it would be in smaller output-swing I/O standards such as LVDS or GLVDS.

2.1.3 Summary of the PECL I/O Standard

The PECL I/O standard is inflexible relative to decreasing IC supply voltages. As seen in Tables 2-1 and 2-2 the PECL standard can not be easily implemented for supply voltages below 2.5V. Further use of the PECL standard requires 3.3V or 2.5V supplies on-chip which contributes unecessarily to power dissipated on the IC. As not all ICs on-board operate with the same voltage supplies, the relatively high PECL output voltages may make it difficult to interface with other on-board circuits. A disadvantage of PECL signalling is the size of its output swing. The 750mV output swing offers high noise

immunity (and ease of interfacing with other ECL circuitry) but is too large to be efficiently implemented in low-supply circuits.

2.2 The LVDS I/O Family

The demand for greater computer processing power has led the need for using a large number of processors cooperatively. This cooperation has motivated the development of the Scalable Coherent Interface (SCI, IEEE Std 1596-1992), a high-speed packet transmission protocol. The initial physical implementation of SCI is based on ECL signal levels which consume more power than is practical in a low-cost workstation environment [7]. The low-cost solution was to implement the I/O circuits in CMOS, reduce the output voltages for low-power, and reduce the output signal swing to increase bandwidth. The resulting standard IEEE Std 1596.3-1996 [6] is known as Low-Voltage Differential Signaling (LVDS) of which the general and low-power transmitter/receiver specification is summarized in Table 2-3.

Table 2-3: General and Low-Power LVDS Standard Specifications [7]

Symbol	Parameter	General Spec.		Low Power Spec.		Unit	Condition
		Min	Max	Min	Max		
Transmitter							
V_{OH}	Output high voltage		1475		1375	mV	$R_T = 100\Omega$
V_{OL}	Output low voltage	925		1025		mV	$R_T = 100\Omega$
V_{PP}	Output diff. voltage	250	400	150	250	mV	$R_T = 100\Omega$
V_{OS}	Output offset voltage	1125	1275	1150	1250	mV	
Receiver							
	Input voltage range	0	2400	0	2000	mV	$V_{id} < 950mV$
	Diff. high threshold		+100		+100	mV	$V_{id} < 950mV$
	Diff. low threshold	-100		-100		mV	$V_{id} < 950mV$

2.2.1 The LVDS Transmitter

The standard transceiver connection schematic for LVDS I/Os is shown in Fig. 2.4. Assuming 50Ω characteristic impedance (Z_o) transmission lines between the LVDS transmitter and receiver, a 100Ω (R_T) termination resistor is required between the differential outputs at the receiver. It is this 100Ω termination resistance which the differential output swing is generated across.

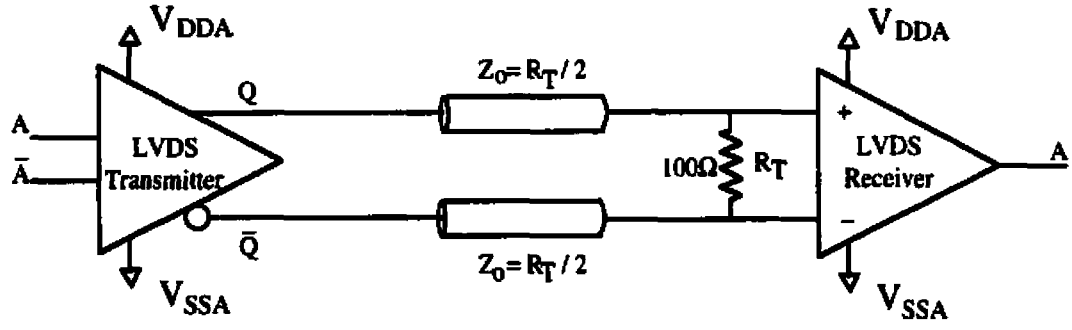

Figure 2.4: Standard LVDS Transmitter and Receiver Connection

The LVDS transmitter output behaves as a constant current source which can switch the polarity of its output current depending on its input. Assuming an LVDS design with 300mV output swing and logic 1 as the input A, the 3mA output current will leave terminal Q and pass through the 100Ω resistor on its way back into the LVDS transmitter. With a logic 0 as the input A, the output Q will sink the 3mA current to generate the 300mV swing at the receiver in the opposite polarity as the logic 1 input case.

2.2.2 The LVDS Receiver

As for the PECL standard receiver, the differential nature of the transmitted LVDS signal makes an open-loop operational amplifier an excellent receiver for the LVDS standard

(see Fig. 2.4). Again, the major design requirement for the receiver is a high CMRR at the LVDS common-mode output voltage (~1.2V). Input sensitivity of the LVDS receiver is a greater issue than for the PECL receiver, as the LVDS differential output swing is ≤400mV rather than the PECL 750mV swing. However, relatively low gain is necessary to rectify a 400mV differential signal to a single-ended CMOS level.

2.2.3 Summary of the LVDS I/O Standard

In comparison with the PECL standard, LVDS consumes less power and can be more easily implemented in low-voltage supply environments. The LVDS differential voltage swing still provides good noise immunity while not consuming so much voltage as to make it feasible only with 3.3V or 2.5V supplies. However, the LVDS standard can not easily be implemented in CMOS technology below the standard 1.8V supply level being used in 0.18μm CMOS cores. The maximum LVDS standard output voltage is 1.475V making design for a 1.8V supply very difficult. Currently 0.25μm and 0.18μm CMOS ICs allow 3.3V and 2.5V I/O designs, so the 1.8V LVDS design limit may not be reached for several advances in CMOS technology.

2.3 The GLVDS I/O Standard

The GLVDS standard is a proprietary standard of Ericsson Telecom [1]. The GLVDS standard is a ground-referenced differential output standard with an output swing of 200mV-500mV. A brief summary of the GLVDS standard is given in Table 2-4.

Table 2-4: Summary of the GLVDS I/O Standard [1]

Parameter	GLVDS Standard	Unit
Transmitter		
Differential Output Swing	200-500	mV
Output Impedance	50 ±30%	Ω
Receiver		
Common Mode Range	-0.6 to (VDD+0.6)	V
Input Sensitivity	50	mV

The most desirable attribute of the GLVDS standard is that the output voltage of the transmitter is ground-referenced. As many different chips on a board can be powered from differing supply voltages, interfacing their I/O circuitry can be difficult. Because ground is a common voltage among the different ICs on a board, GLVDS's ground-referenced output can be used to signal between all on-board circuitry. Additionally, GLVDS transmitters and receivers are compatible with LVDS circuits, making the interface of GLVDS with existing I/Os possible [1].

2.3.1 The GLVDS Transmitter

The GLVDS transmitter is connected to its receiver as shown in Fig. 2.5. As seen in Fig. 2.5, the GLVDS transceiver requires no external (on-board) termination. The GLVDS transmitter's output transistors operate in the linear region allowing its output impedance to be easily matched to that of the characteristic impedance of the transmission lines which minimizes output signal reflections [1].

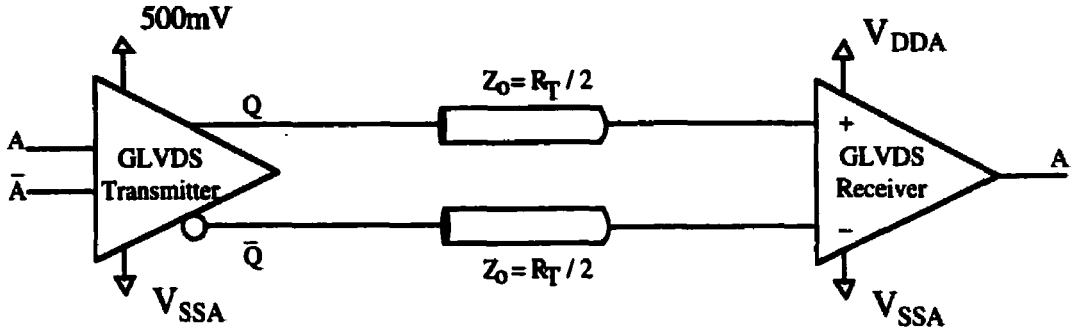

Figure 2.5: Standard GLVDS Transmitter and Receiver Connection

The GLVDS transmitter requires an extra low-voltage supply pin (V_{DD} = 500mV-200mV) which matches that of the desired output voltage swing.

2.3.2 The GLVDS Receiver

The low common-mode output voltage of the GLVDS transmitter forces the receiver to have a high CMRR at voltages near ground. If using a voltage-mode receiving op-amp, the receiver input transistors are forced to be PMOS devices to meet the low-voltage CMRR requirement. Unfortunately, PMOS input transistors have limited high-frequency operability, and NMOS input devices would work best if possible. To avoid the use of PMOS input gates, Ericsson designed a current-mode differential receiver with a common-mode voltage range of –0.6V to VDD+0.6V [1]. Ericsson Telecom further supports the use of the current-mode receiver in a low-voltage swing environment because it offers greater immunity to voltage noise. The Ericsson receiver design also saves on-board real estate as the termination resistors are in-circuit linear-biased NMOS devices.

2.3.3 Summary of the GLVDS Standard

The GLVDS standard is a very advanced I/O. Its low-voltage, low-power, high-speed capabilities exceeds that of the I/O standards already discussed. The 500mV and less supply voltage makes GLVDS a standard which will not be out-dated in quite a long time as 500mV core supplies have not yet been projected for CMOS IC technology. Another strength of the GLVDS standard is the current-mode receiver architecture. The GLVDS receiver design provides a high input sensitivity and wide CMRR range with in-circuit termination. However, a drawback of GLVDS is that the GLVDS standard and circuit architectures are proprietary to Ericsson Telecom making its wide use unpredictable in the future.

2.4 The OSDS I/O Circuit

As mentioned above, GLVDS is a very good I/O standard relative to coming changes in CMOS IC technology. In an effort to implement the GLVDS standard without infringing upon existing patents, I have proposed another standard: Open Source Differential Signaling (OSDS). To date, only the OSDS transmitter has been designed and simulated. The ultimate goal of the OSDS standard is to offer the advantages of the GLVDS standard without the disadvantage of patent infringement. The OSDS standard design specifications are the same as the GLVDS standard (see Table 2-4).

2.4.1 The OSDS Transmitter

The OSDS transmitter of Fig. 2.6 is a differential open-source current 'steering' circuit. As a proper receiver has not yet been designed for OSDS, current transmitter designs

incorporate external termination resistances at the receiving end. The OSDS transmitter runs as a constant current source. As the transmitter input is changed, the constant output current is switched between the differential outputs. The output current then generates a voltage at one receiver input and leaves the other at ground potential.

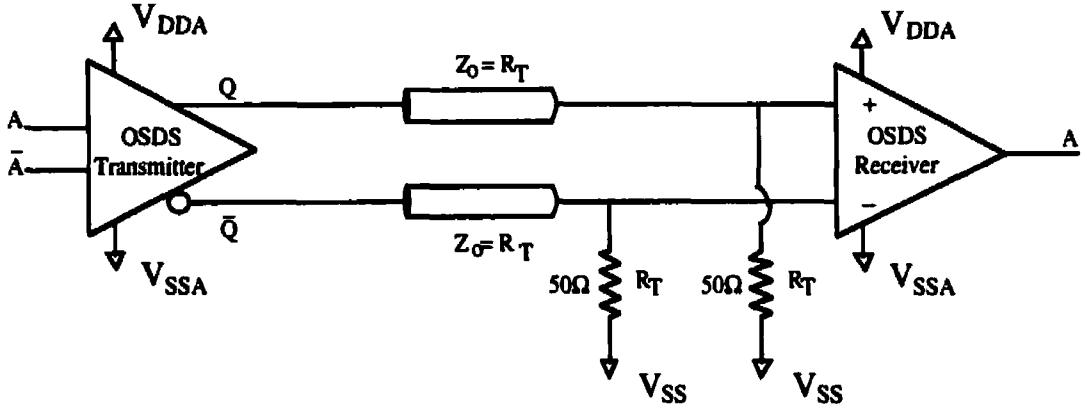

Figure 2.6: OSDS Transmitter and Receiver Connectivity

The open-source topology of the circuit makes it quite easy to set the circuit's output impedance to match the characteristic impedance of the driven transmission line and minimize reflections. The OSDS transmitter can be powered by core voltages and does not require additional power pins. However, in comparison to the GLVDS transmitter, OSDS consumes more power. Assuming a 50Ω transmission line and 50Ω termination resistance, 10mA is required to generate a 500mV signal at the receiving end.

2.4.2 The OSDS Receiver

As was the case with the GLVDS receiver, the low-voltage common-mode signaling of the OSDS transmitter requires a receiver with a high CMRR at low voltages. During the design of the OSDS transmitter, several wide-range CMRR amplifier designs were

investigated. However, time constraints forced the use of the GLVDS receiver design as an OSDS receiver for this thesis.

2.4.3 Summary of the OSDS I/O Circuit

There are several advantages to the OSDS transmitter design:

- High output current allows fast charge/discharge of parasitic capacitances from ESD protection, the package, and the transmission lines.
- If a very low differential swing is used (200-300mV), the drive current and thus the on-chip power dissipation is reduced. This point is dependent on an appropriate low-noise, high CMRR OSDS receiver.
- A reduction in the differential output swing reduces the minimum allowable power supply for OSDS transmitter implementation.
- OSDS can be implemented with core voltage levels, reducing the necessary supply pins for the IC.

Although the OSDS transmitter in its current topology can not be designed with power supplies below ~1V, it will still be some time before CMOS technology moves below 1V supplies.

2.5 Comparative Analysis of the Differential I/O Standards

A quantitative comparison of which is the better differential I/O standard is not possible from the information in this Chapter alone. However, an initial comparison is possible from knowing the output levels and termination values for each I/O standard.

A drawback to the PECL, LVDS and OSDS I/O standards is that they rely on a DC output current from a high potential (> V_{out}) to develop a low potential across their termination resistance (Fig. 2.7). The result is that most of the DC circuit power is being dissipated on-chip in the transmitter rather than the output termination.

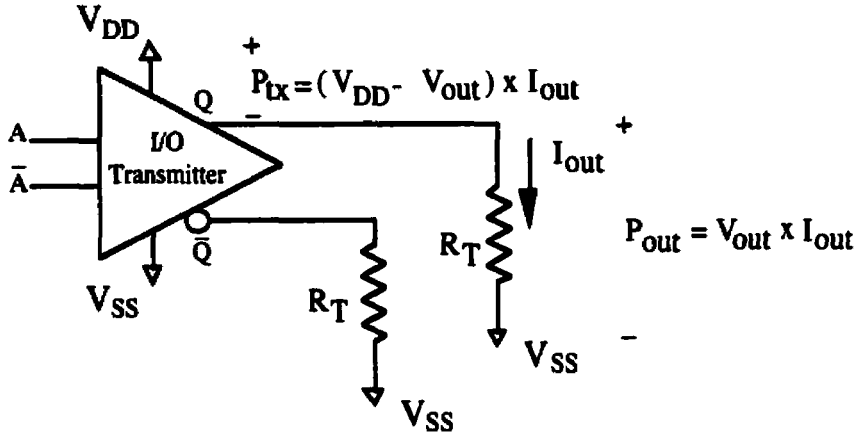

Figure 2.7: I/O Transmitter Example Showing Excessive On-Chip Power Due to Current Biasing

The major reason for the excessive on-chip power dissipation in the current-biased I/O schemes is the low characteristic impedance signaling environment. If the termination resistors could be made larger, smaller bias currents would be necessary to generate output levels, which would reduce the overall circuit power consumption. However, the termination resistors must be made to match that of the signaling environment's characteristic impedance which is typically 50Ω.

The GLVDS transmitter offers a comparatively low-power specification because it is a voltage-biased circuit. In the GLVDS transmitter, the V_{DD} = 500mV and V_{SS} supplies are switched between the outputs rather than a bias current. The result is that most of the circuit's DC power is dissipated in the GLVDS termination rather than in the transmitter.

For DC power consumption alone, the GLVDS, LVDS, OSDS, and PECL I/O circuits which represent their respective I/O standard, rank from best to worst respectively. However, power consumption is not the only method of rating an I/O circuit, maximum output bandwidth is also a factor. A ratio of the maximum power consumption to maximum output bandwidth would be a better rating of the I/O circuits. Therefore, a method of testing the output bandwidth of I/O circuits implementing these differential I/O standards must be investigated to assess the overall value of the I/O standard.

3.0 On-Chip Testing of Low-Voltage Differential I/O Circuits

A significant challenge in evaluating high-speed differential I/O circuits is testing their high-frequency operating performance. The frequencies of interest for the I/O circuits in this thesis are the >622Mb/s values used in ATM applications. The equipment to test 622Mb/s – 2.5Gb/s I/O operation is available but costly and complex. Additionally, the IC ceramic packaging provided by the Canadian Microelectronics Corporation (CMC) contributes parasitics which suppress output frequencies above 50MHz [8].

Therefore, a method must be devised to test the high-frequency operability of the differential I/O circuits under study. This test method must:

- Allow the high-frequency I/O signals to run on-chip where they are not heavily bandwidth-limited.
- Have no need for high-frequency signals either as an input or output of the system where they will be suppressed by package parasitics.
- Output a low-frequency signal proportional to the high-frequency signal of the transmitter/receiver pair under test.

This section will justify the need for an on-chip test method, and then propose the circuits for the on-chip I/O test system or "I/O testbench".

3.1 IC Package Bandwidth Limitations

Parasitics associated with the IC packaging and bonding process force bandwidth limitations on signals going on, or coming off-chip. For the circuits which will be fabricated for this thesis, the IC packaging is provided by the Canadian Microelectronics Corporation. The 'fastest' package offered by CMC is the 24-pin Ceramic Flat Package (24-CFP). The actual package which will house the ICs for this thesis is the 44-pin Ceramic Quad Flat Package (44-CQFP). As a 44-CQFP package model was not available, the 24-CFP package model will be used to demonstrate package enforced I/O bandwidth limitations. This substitution is valid as the 24-CFP is a 'faster' package than the 44-CQFP, and failure of the 24-CFP at a specific frequency ensures failure of the 44-CQFP at the same frequency [8].

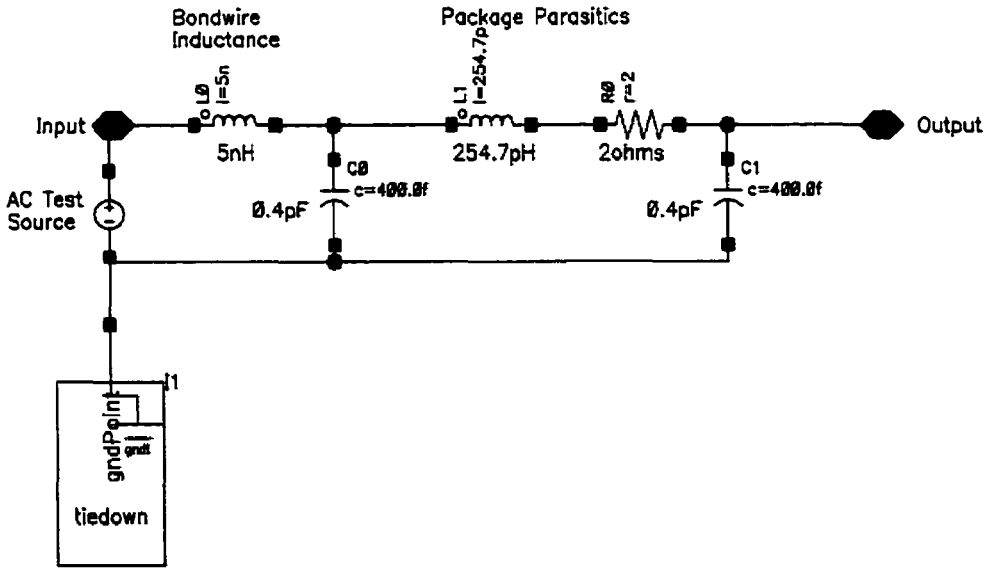

Figure 3.1: Typical Model of 24-CFP Pin Including Bond-Wire [8]

An HSPICE AC simulation of the 24-CFP package parasitics in Fig. 3.1 yields the frequency response shown in Fig. 3.2. This AC simulation makes it obvious that even the 24-CFP package is unsuitable at frequencies above 622Mb/s. Simulations of 622Mb/s signals through the 24-CFP pin parasitics show the output waveform to include severe sinusoidal oscillations at the resonant frequencies between 2.1GHz and 2.5GHz. Therefore, an on-chip system to test the high-frequency performance of the I/O transceivers must be implemented on ICs within the 44-CQFP.

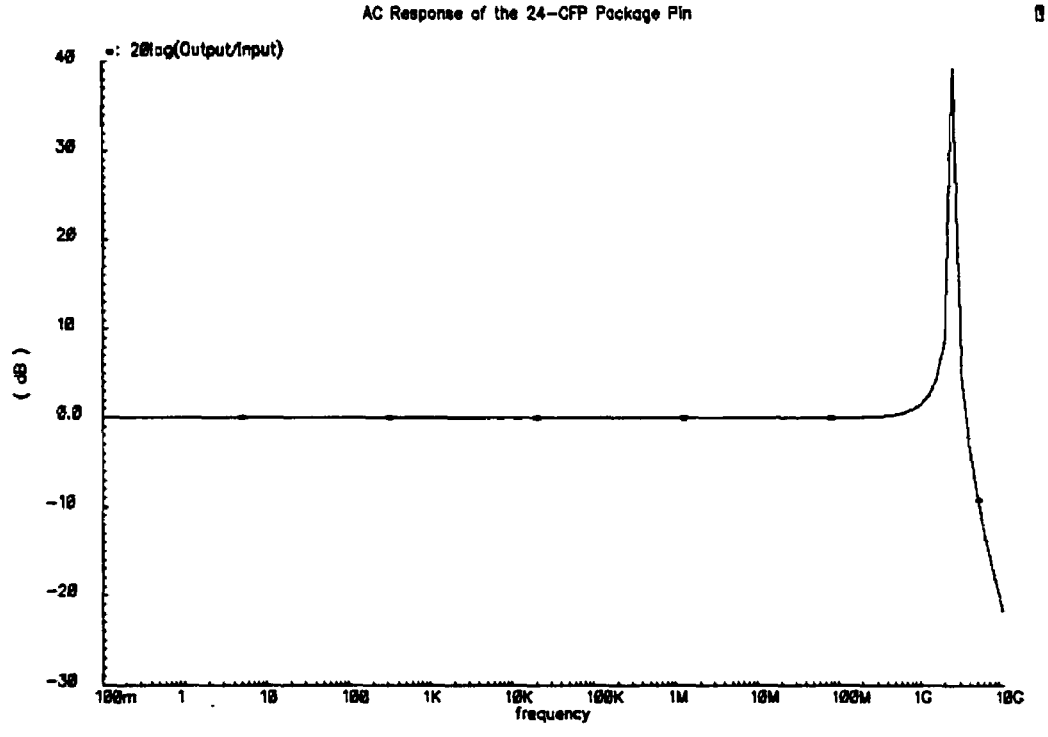

Figure 3.2: Bode Plot of the HSPICE AC Response of a 24-CFP Pin

3.2 On-Chip Test System Requirements

As the desired I/O circuit test frequencies of 622Mb/s-2.5Gb/s may not be transmitted on or off-chip due to the packaging, the transmitter/receiver pairs must be coupled on-chip in

a test system where those frequencies are allowable. The transmitter requires a high-frequency periodic stimulus to both test the high-frequency I/O performance and provide predictability in the input and hence the output of the testbench. The output of the receiver must be connected with a circuit which will drive a low-frequency signal off-chip that is proportional to the transmitted high-frequency I/O signal. The block diagram of the proposed high-frequency I/O test system is shown in Fig. 3.3.

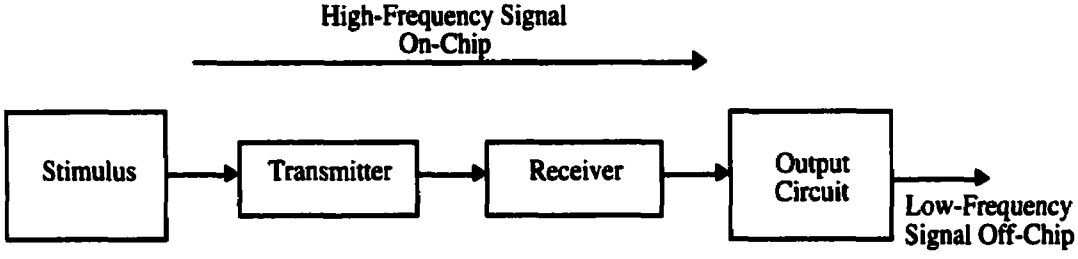

Figure 3.3: Block Diagram of the Proposed High-Frequency I/O Test System

The following sections will describe each of the above circuit blocks and the type of circuit chosen to implement them.

3.3 The Transmitter Stimulus Circuit

To implement a periodic high-frequency input for the I/O transmitter under test, an on-chip oscillator circuit must be used. There are several types of on-chip oscillators: ring oscillators, VCOs, Colpitts oscillators and others. For the sake of simplicity, a ring oscillator was chosen to generate the transmitter input (see Fig. 3.4).

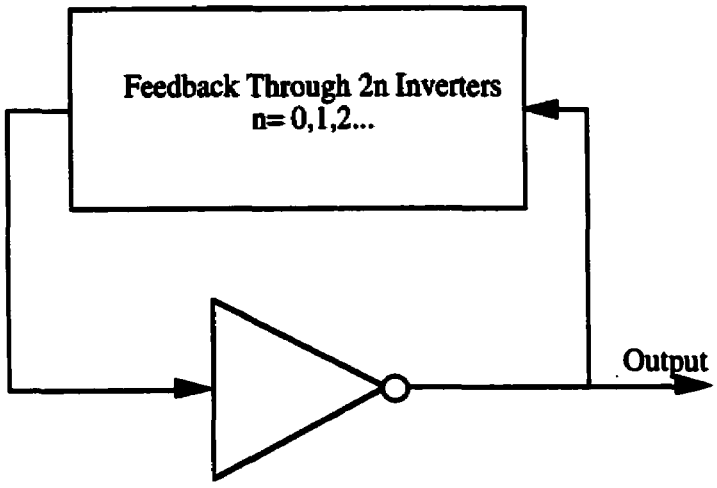

Figure 3.4: Typical Ring Oscillator Schematic

As mentioned, the advantage of using a ring oscillator is its simplicity in both design and layout. The only disadvantages of using a standard ring oscillator circuit is the relatively high sensitivity of its output frequency to process variation and environment conditions (mostly temperature), and the lack of external control of the output frequency [9]. Because the output frequency of a ring oscillator is not controllable, several ring oscillators circuits are necessary to test several operating frequencies.

3.4 The Transmitter/Receiver Pair

The transmitter and receiver circuits under test will be directly connected to each other on-chip as in Fig. 3.5. The area between the transmitter and receiver circuits must be occupied by the required termination for the I/O standard.

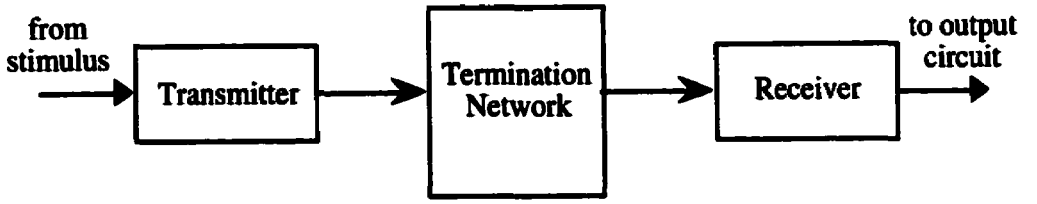

Figure 3.5: Block Diagram of Transmitter and Receiver Connectivity Including Required Termination

The area between the transmitter and receiver is also a place to add circuits which will additionally test the I/O standard's performance. An on-chip capacitor can be laid out between the transmitter and receiver to test the I/O circuit performance in the presence of parasitics due to ESD protection circuitry or packaging. However, testing the effects of ESD protection circuitry in the I/O testbench is for future work and is beyond the scope of this thesis.

3.5 The Input-Frequency Proportional Output Circuit

There are two types of circuits which could be designed as the output for the I/O test system: a circuit with its output voltage proportional to the input frequency, or a circuit with its output frequency proportional to the input frequency. It was decided that the latter option would be most easily implemented as a CMOS circuit.

Figure 3.6: Prescaler Implementation as I/O Test System Output Block

The circuit chosen for the output block is a ÷128 prescaler [10] (Fig. 3.6). For a periodic CMOS input of frequency *f*, the prescaler will output a periodic CMOS signal of frequency *f/128*. For the I/O test frequencies of 622Mb/s – 2.5Gb/s, the prescaler would drive a signal off-chip at frequencies of 4.86MHz – 19.5MHz which is within the 44-CQFP's bandwidth capabilities.

3.6 Overview of the Chosen On-Chip I/O Circuit Test System

Fig. 3.7 shows the on-chip I/O testbench, including the chosen circuits to implement the blocks in Fig. 3.3. Buffers have been placed at the input and output of the transceiver to reduce loading of the ring oscillator and receiver circuit outputs respectively. An additional buffer is necessary at the prescaler output to drive the probe capacitance of the off-chip measurement equipment.

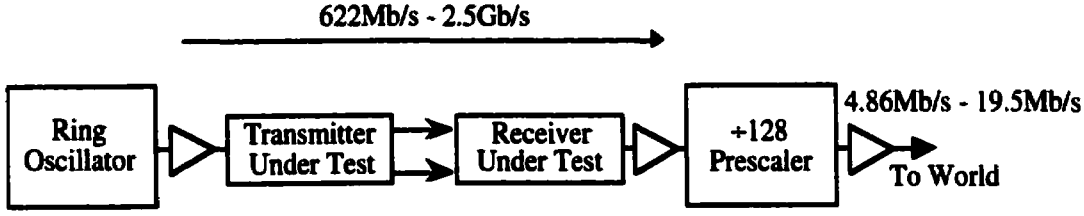

Figure 3.7: Chosen High-Frequency I/O Test System

Because of the lack of control of the ring oscillator output frequency, there will be 3 I/O testbenches corresponding to 3 different test frequencies for each I/O standard under test. To act as a control, systems will be designed with the 3 different ring oscillators coupled with the prescaler only (Fig. 3.8). The output frequency of these control circuits will provide a reference for the output frequency of the I/O testbenches when they are fabricated.

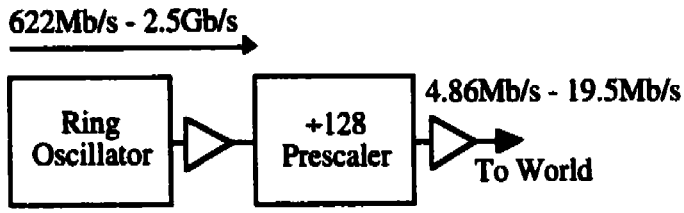

Figure 3.8: Control Circuit for the High-Frequency I/O Test System

3.7 Implementation of the On-Chip I/O Testbench

To this point, the operating specifications of the I/O circuits and the I/O testbench have been determined. What has not yet been determined is the exact circuit architectures or the technology which the proposed circuits will be implemented in. The next step is to choose a technology and vary the active device characteristics of a chosen circuit in simulation until all circuit specifications are met. Once circuit specifications are met in simulation which includes possible process variation, the circuits may be physically designed and submitted for fabrication.

4.0 Simulated Operation of the High-Frequency I/O Circuits and On-Chip I/O Testbench

The I/O transmitters and receivers, and the on-chip testbench are to be designed for the TSMC 0.25μm CMOS process through CMC and PMC-Sierra Inc. The HSPICE typical and corner device models for the 0.25μm process have also been provided through CMC. The circuit schematics were created in Cadence Composer and are simulated in HSPICE through Cadence Analog Artist.

This section will present the device-level circuit schematics for each transmitter, receiver and testbench component. The results of DC simulations of the transmitters and receivers will be presented and used to support the selection of the circuit's device aspect ratios. HSPICE transient simulation results of the testbench components and the I/O testbenches will also be presented as justification for the fabrication of these circuits.

4.1 DC Simulations of the I/O Transmitters and Receivers

Before simulating the transient behaviour of the I/O transmitter/receiver pairs in the on-chip testbench circuits, the I/O circuits must be designed within their respective DC I/O standard specifications. Therefore the I/O circuit topology must first be determined, and then the device aspect ratios varied and DC simulated until output levels are within the I/O family's specifications.

In the case of PECL, LVDS and GLVDS I/O circuits, literature-based topologies are used in their design leaving only device aspect ratios to be chosen and varied in HSPICE DC

simulations. The OSDS transmitter design is based upon a PECL-like topology but the device dimensions are varied in simulation to achieve GLVDS-like output levels.

4.1.1 The PECL Transmitter

The PECL transmitter circuit is shown in Fig. 4.1 with devices and their aspect ratios clearly marked. The chosen circuit topology is based on the common open-drain PECL transmitter published in literature [6]. The circuit in Fig. 4.1 is an open-drain design with two nMOS 'drive' transistors M1 and M2, and a current sink transistor M3.

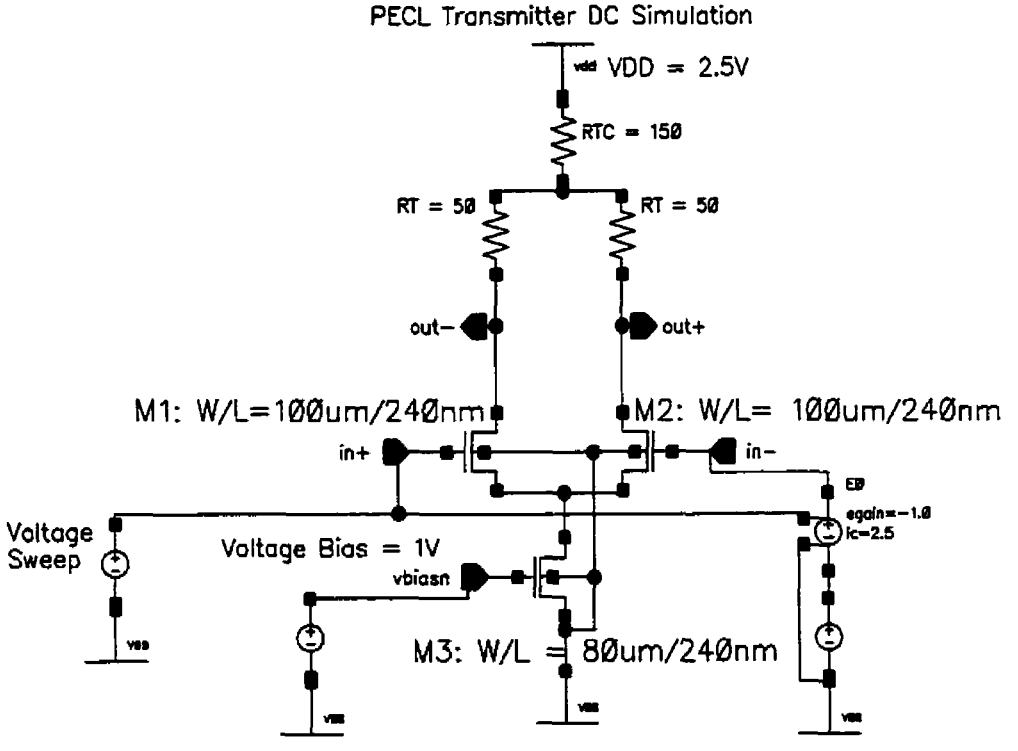

Figure 4.1: PECL Transmitter Circuit Including DC Simulation Bench

Also shown in Fig. 4.1 is the HSPICE DC simulation bench: a DC source, current-sink bias supply, output transmission lines, and external termination. The external termination is calculated from Eq. 2.1 to be within the LVDS range of output values from Table 2-2

for reasons described below. The transmission lines were selected with the common characteristic impedance of 50Ω.

The primary constraint in the design of the PECL transmitter is the signal transmission environment. To minimize output signal reflection, the termination resistors R_T must match the transmission line 50Ω impedance. As the typical PECL output voltage swing of 750mV is generated across the two 50Ω resistors R_T, the PECL output current is forced to be 15mA. A 15mA current drive is much more than the currents in the other I/O transmitters, and presents problems in its physical design (Ch. 5.0). Therefore, the PECL I/O standard was ruled out at this point due to excessive power consumption. However, the above circuit topology will be used to provide LVDS standard output levels. This will provide a comparison of different circuit topologies for the same LVDS I/O output levels.

A 7mA sink current is required for the ~350mV typical LVDS output swing from the PECL transmitter circuit across the 50Ω termination resistors. Therefore M3 must sink a constant 7mA DC current while complementary CMOS signals at the gates of M1 and M2 'steer' the 7mA through one output or the other.

Fig. 4.2 shows the HSPICE DC simulation results of the simulation bench in Fig. 4.1. The DC simulation was performed using the typical (TT) 0.25μm process device models. Table 4-1 gives the output levels for the TT and extreme process corner device models: SS (slow transistors), and FF (fast transistors).

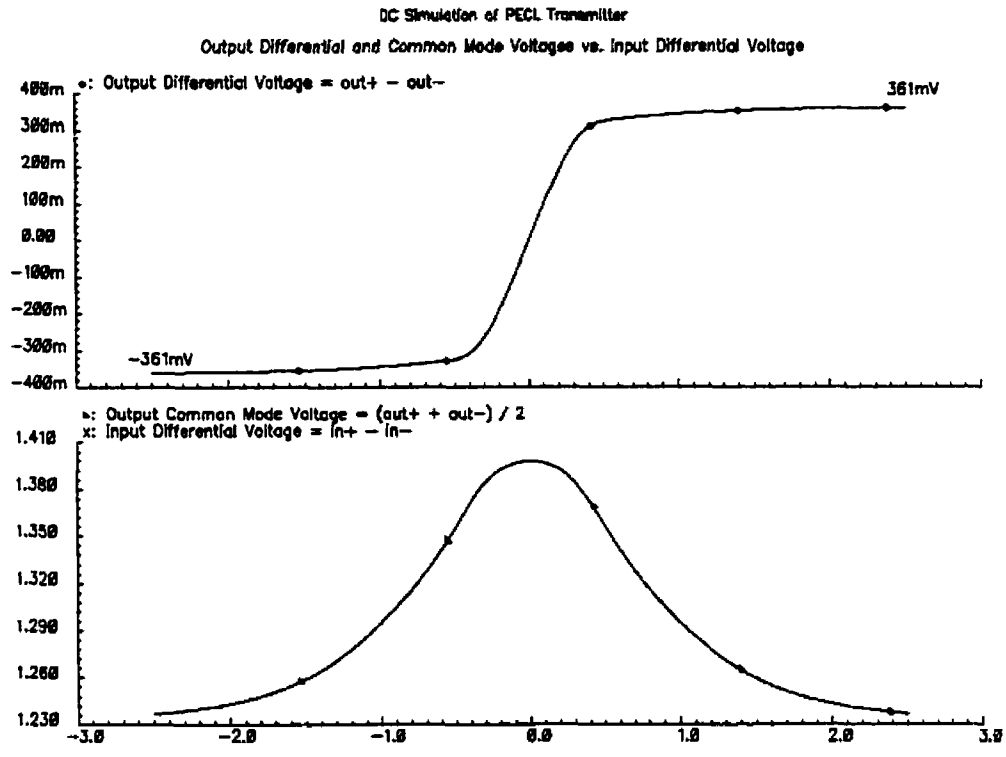

Figure 4.2: HSPICE DC Simulation Results of the PECL Transmitter Simulation Bench

Table 4-1: PECL Transmitter Simulated Output Levels for SS, TT and FF Device Models

Transmitter Output Parameter	SS	TT	FF
Output Differential Swing	277mV	361mV	446mV
Output Common Mode Voltage	1.531V	1.236V	939mV

The output levels of the Fig. 4.1 PECL transmitter circuit fall within the LVDS standard differential output range (Table 2-3). The output common-mode values for the PECL transmitter are acceptable for typical (TT) simulations but fall out of the LVDS specification for the SS and FF device models. The Fig. 4.1 circuit's dependence on the biasing transistor M3 is what makes the simulated output values change significantly with

process models. However, the wider range of output common-mode voltage will not be a problem when the circuit is implemented if the receiver's input common-mode range (CMR) accepts the Table 4-1 output values.

4.1.2 The LVDS Transmitter

The LVDS transmitter circuit topology in Fig. 4.3 that was proposed in [11], has been adapted for this thesis. As with the PECL transmitter, the primary constraint on the LVDS transmitter is the signaling environment. In a 50Ω characteristic impedance environment, a 100Ω resistor is used as termination between both signal lines at the receiving end. Therefore, to develop the 300mV differential swing across the terminating resistor, the transmitter must source a 3mA current.

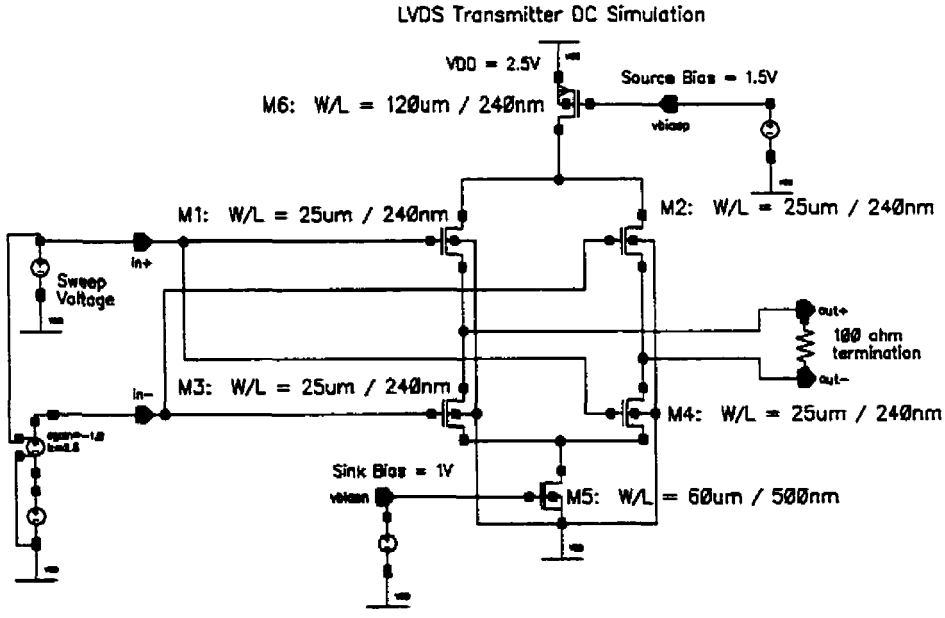

Figure 4.3: LVDS Transmitter Circuit and HSPICE DC Simulation Bench

The pMOS current source and nMOS current sink M6 and M5 supply the 3mA DC current and consume some potential to establish both the 300mV differential output

swing and the output common-mode voltage of ~1.2V. The transistors M1-M4 act as current switches: when in+ is logic 1 and in- logic 0, current may pass out the out+ terminal and back in the out- via the 100Ω resistor. The opposite case is true for a in+ of logic 0, making the LVDS transmitter a constant current source with switchable polarity to generate two output differential voltage states.

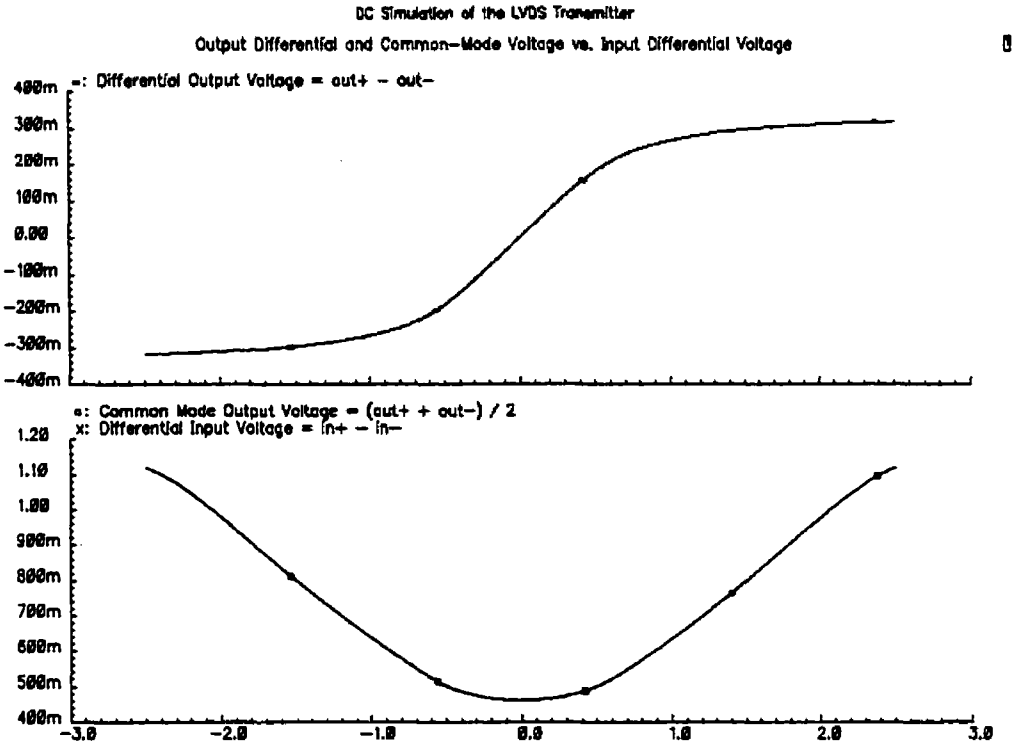

Figure 4.4: HSPICE DC Simulation Results of the LVDS Transmitter

The first criteria for designing the LVDS transmitter was to establish both the 3mA current through the current source/sink and their appropriate resistance to achieve the LVDS output common-mode voltage. The second criteria was to add the M3-M6 transistors and change their aspect ratios until the LVDS output voltages were simulated.

The typical output differential and common-mode voltages versus the input differential voltage for the Fig. 4.3 circuit is shown in Fig. 4.4. The output swing and common-mode voltage levels of the simulated LVDS transmitter are given in Table 4-2.

Table 4-2: LVDS Transmitter Simulated Output Levels for SS, TT and FF Device Models

Transmitter Output Parameter	SS	TT	FF
Output Differential Swing	216mV	317mV	412mV
Output Common Mode Voltage	584mV	1.12V	1.175V

The simulated output values from Table 4-2 adhere to the LVDS standard in all cases but the SS simulations. The deviations from the LVDS standard are tolerable provided a receiver with appropriate CMR and gain is receiving the output signal. The Fig. 4.3 transmitter circuit's dependence on two biasing transistors makes it sensitive to process variation.

4.1.3 The PECL and LVDS Receiver

The simple single-stage CMOS amplifier with current-mirror load of Fig. 4.5 was chosen as a receiver for both the PECL and LVDS I/O standards. The amplifier is composed of two nMOS input transistors M1 and M2, the pMOS mirror-load devices M3 and M4, and the current-sink transistor M5. Designing the amplifier with enough gain to rectify a 300mV-750mV differential input signal to CMOS output levels is not a difficult specification to achieve with this circuit. The single-stage amplifier with mirror load easily provides enough gain to rectify a >200mV differential signal to a single-ended CMOS level.

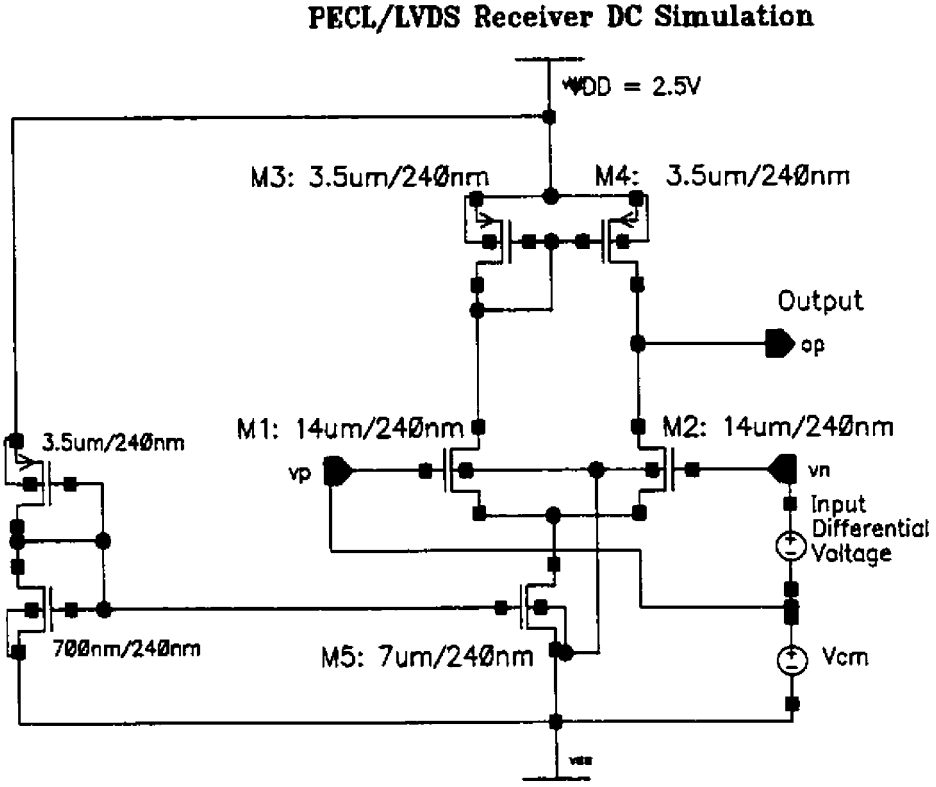

Figure 4.5: PECL and LVDS Receiving Amplifier Including Testbench

The most important design specification of the receiving amplifier is a broad CMR. For the PECL and LVDS I/O standard, the CMRR should be high for the CMR above 1.2V (LVDS has ~1.2V common-mode). To determine whether the receiver has an adequate CMR for the differential I/O standards, a DC simulation test was devised and is included in Fig. 4.5 with the receiver schematic. Two DC simulations are performed: one with a +200mV differential input and the other with -200mV. Both simulations are conducted while sweeping the input's common-mode voltage between V_{DD} and V_{SS}. The points at which the receiver's output switches to an incorrect value in DC simulation will determine the CMR for a ±200mV differential signal. Fig. 4.6 shows the typical DC

simulation results in HSPICE for determining the CMR of the Fig. 4.5 differential receiver.

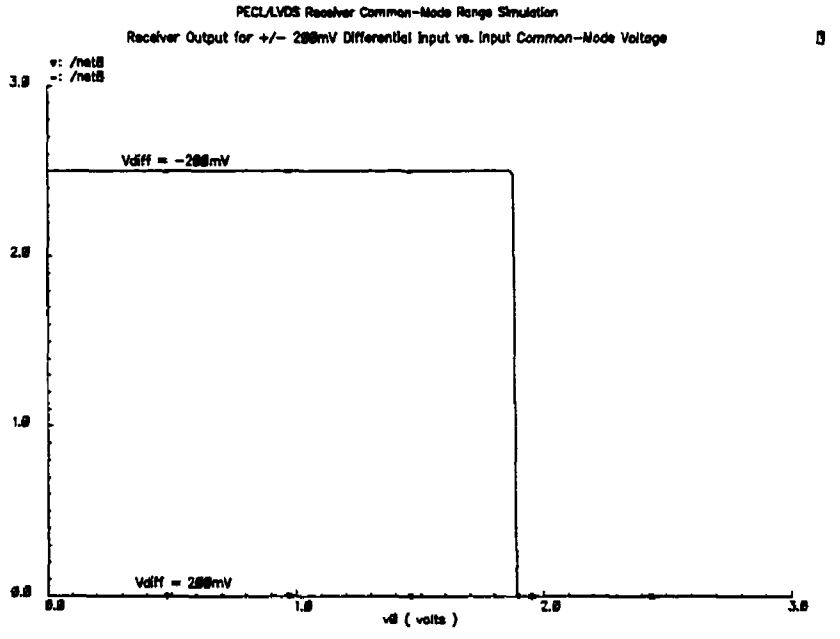

Figure 4.6: CMRR Plot from HSPICE DC Simulation of the Differential Receiver

Table 4-3: Simulated Common-Mode Range for the PECL/LVDS Receiver

	SS	TT	FF
CMR	< 1.92V	< 1.89V	< 1.85V

The CMR values in Table 4-3 were determined at the point when the correct +2.5V output voltage fell to an incorrect 0V level for the –200mV differential input voltage test. The voltages recorded in Table 4-3 provide confidence that the receiver in Fig. 4.5 is acceptable for the typical 1.2V common-mode output of the LVDS standard.

4.1.4 The GLVDS Transmitter

The GLVDS transmitter circuit proposed by Ericsson Telecom [1] is shown in Fig. 4.7. The GLVDS transmitter is composed of an nMOS "super-buffer" [3] (M1-M4) that is powered with 500mV and ground supplies which make up the differential output voltage levels.

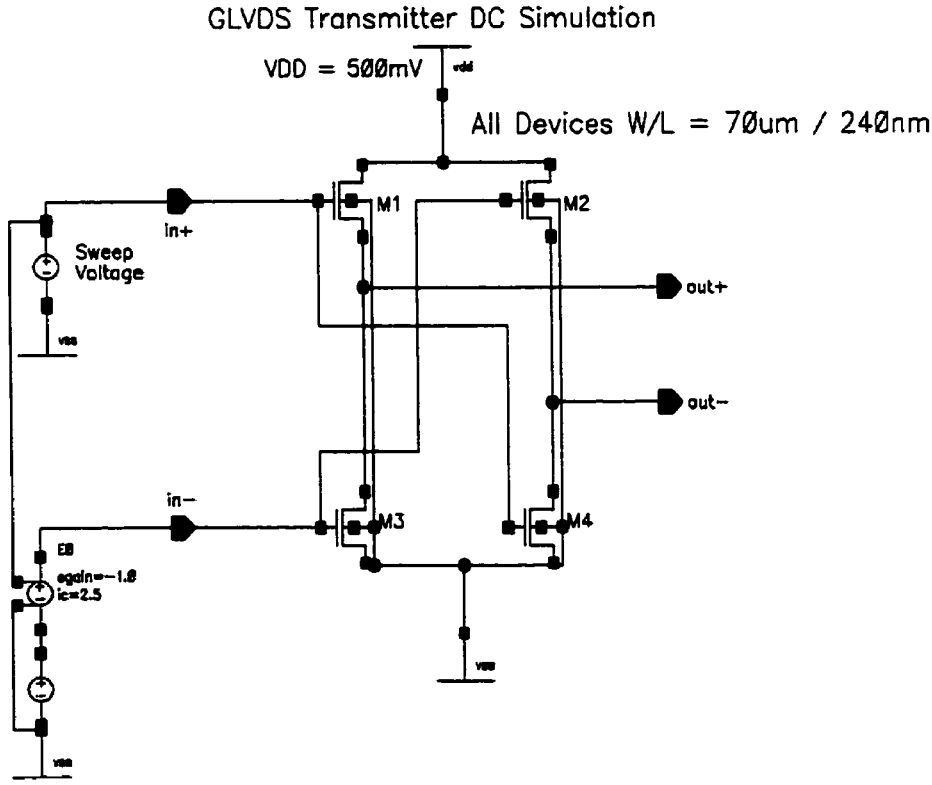

Figure 4.7: GLVDS Transmitter Circuit and HSPICE Simulation Bench

The device aspect ratios in the GLVDS transmitter were made quite large to lower the circuit output resistance and increase the output drive capability.

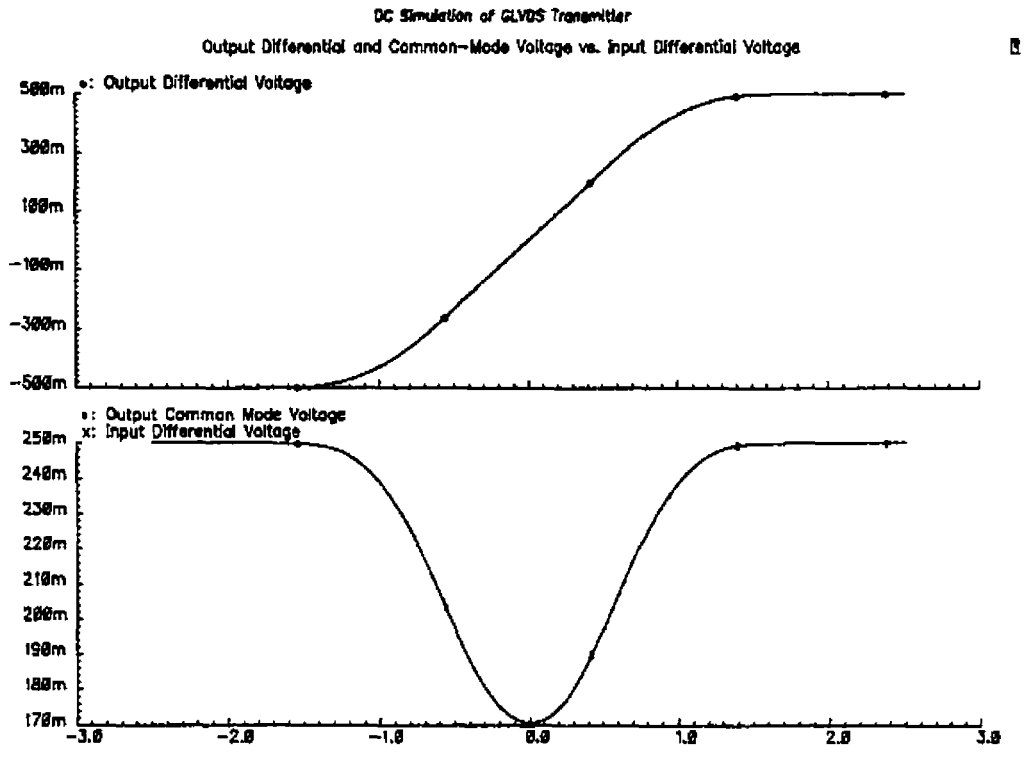

Figure 4.8: HSPICE DC Simulation Results of the GLVDS Transmitter

The typical DC simulated differential and common-mode output voltages of the Fig. 4.7 GLVDS transmitter are plotted in Fig. 4.8 versus the input differential voltage. Table 4-4 provides the simulated output differential swing and common-mode voltages of the GLVDS transmitter over several process corners.

Table 4-4: GLVDS Transmitter Simulated Output Levels for SS, TT and FF Device Models

Transmitter Output Parameter	SS	TT	FF
Output Differential Swing	500mV	500mV	500mV
Output Common Mode Voltage	250mV	250mV	250mV

As seen in Table 4-4, the output swing remains a constant 500mV for each process corner simulated. There are no biasing devices in the GLVDS transmitter, making the design

less sensitive to process variation and therefore more robust relative to the current-biased transmitters of the PECL, LVDS and OSDS standards.

4.1.5 The OSDS Transmitter

The OSDS transmitter circuit is shown in Fig. 4.9. The circuit has a PECL-like topography with a current source M3, and open-source nMOS drive transistors M1 and M2. Again, the 50Ω signaling environment forces the use of 50Ω termination resistors. To develop the maximum output swing of 500mV across the terminating resistors, the OSDS current source must provide a maximum of 10mA DC current.

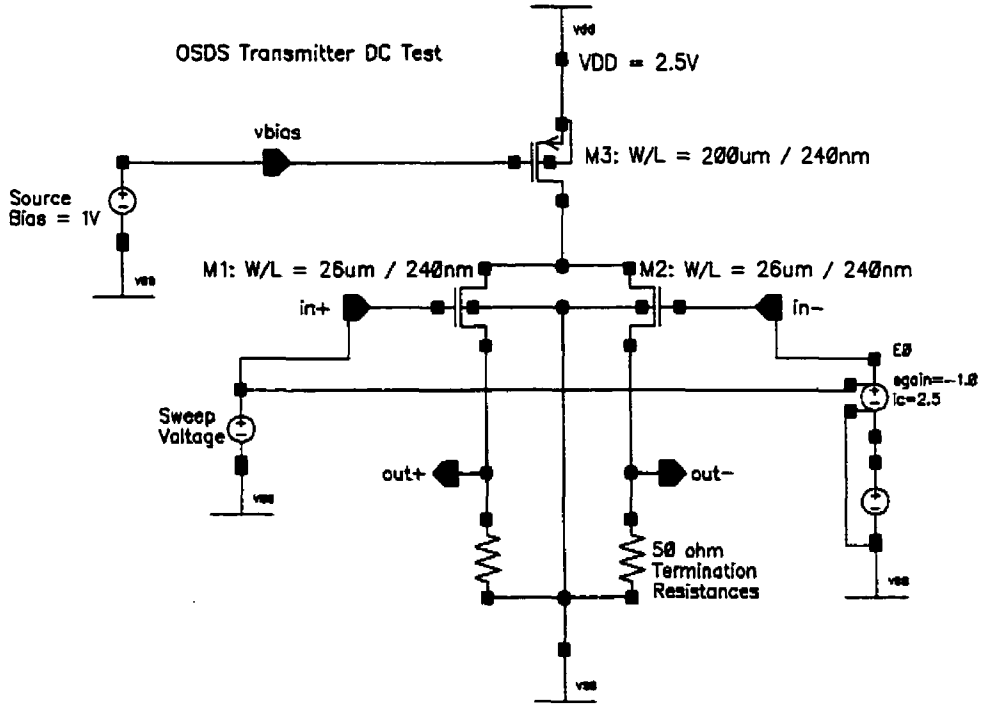

Figure 4.9: OSDS Transmitter Circuit and HSPICE DC Simulation Bench

M1 and M2 receive complementary CMOS inputs, which switch the source current across either termination resistor. As the output signaling levels are 500mV at maximum,

the V_{GS} of the driving transistor is still large enough to conduct the 10mA, allowing an open-source circuit configuration. Fig. 4.10 plots the typical HSPICE DC simulated output differential and common-mode voltages versus input differential voltage for the OSDS transmitter circuit in Fig. 4.9.

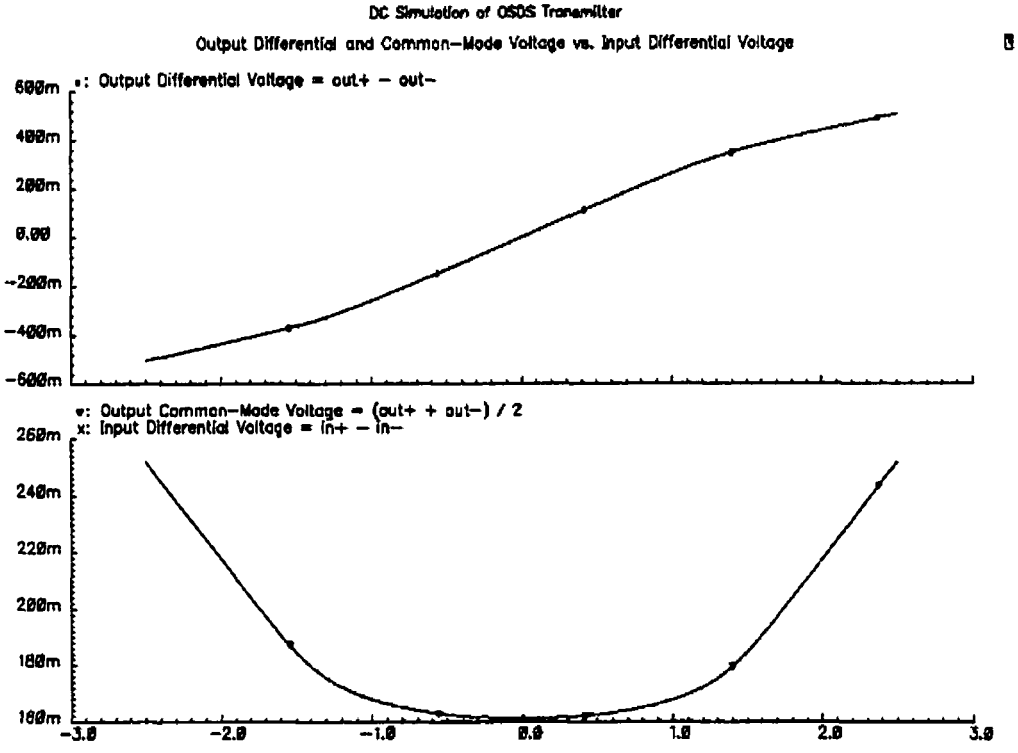

Figure 4.10: HSPICE DC Simulation Results of the OSDS Transmitter

Table 4-5: OSDS Transmitter Simulated Output Levels for SS, TT and FF Device Models

Transmitter Output Parameter	SS	TT	FF
Output Differential Swing	455mV	504mV	562mV
Output Common Mode Voltage	228mV	252mV	281mV

As seen in Table 4-5, the biased OSDS transmitter's output levels are affected by changes in the process. However, the OSDS transmitter outputs are only slightly changed by the

process when compared to the LVDS or PECL transmitter designs. Therefore, the OSDS transmitter in Fig. 4.9 is the second most robust design with respect to process variation.

4.1.6 The GLVDS and OSDS Receiver

The Ericsson Telecom GLVDS receiver is shown in Fig. 4.11 [1]. The receiver is a differential current-mode circuit. The input voltage changes the two input currents which are mirrored into the same signal path in subsequent stages. The difference between the input currents is then amplified and converted to an output voltage in the final stage.

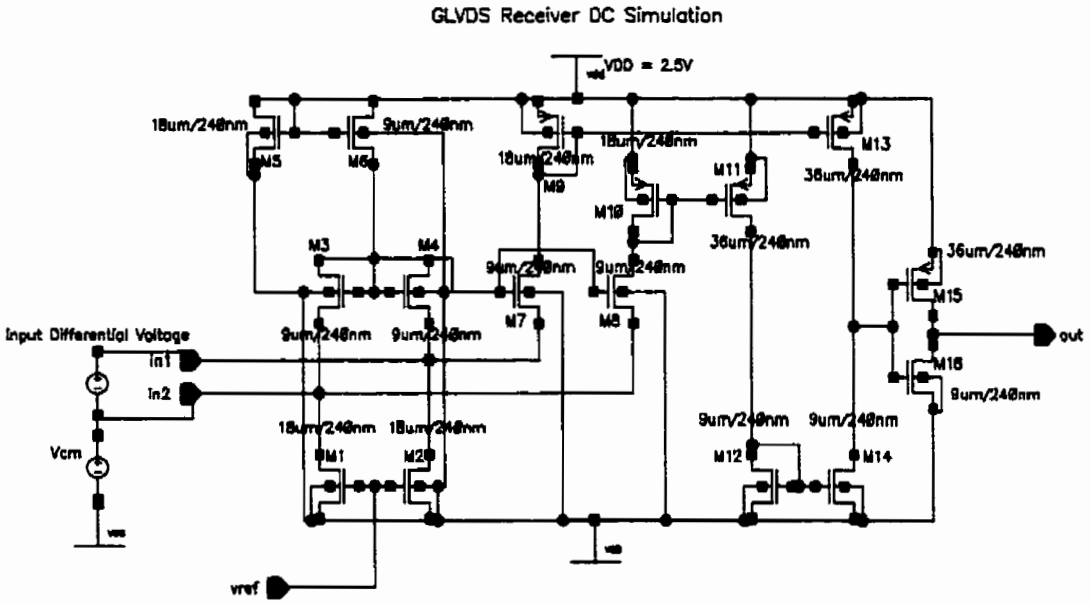

Figure 4.11: GLVDS and OSDS Receiver Circuit and DC Simulation Bench

The Fig. 4.11 circuit has several advantages over voltage-mode receivers: the input common-mode range encompasses all voltage levels between the supplies, and high-impedance inputs minimize the current-noise which the receiver is more susceptible to.

Additionally, the linear-operating transistors M1 and M2 can be biased appropriately to provide in-circuit impedance matching via the *vref* terminal.

The OSDS receiver requires a CMR which extends down to V_{SS}, therefore the GLVDS receiver will be used as the OSDS receiver. Fig. 4.12 is the results of the HSPICE DC simulation of the GLVDS receiver. The simulation determines the CMR of the receiver with a ±200mV differential input signal on a DC swept common-mode voltage. The common-mode voltages at which the receiver output switches in error will determine the CMR of the circuit.

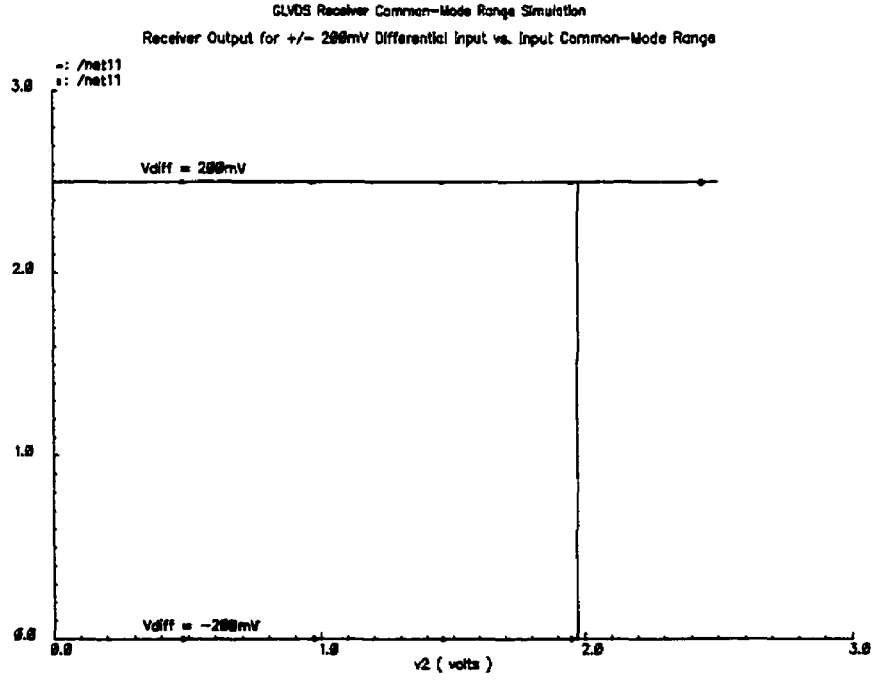

Figure 4.12: HSPICE DC Simulation Results of the GLVDS and OSDS Receiver

Table 4-6: Simulated Common-Mode Range for the GLVDS Receiver

	SS	TT	FF
CMR	< 1.90V	< 1.97V	< 1.98

The CMR values of Table 4-6 show that this particular GLVDS receiver design does not have the V_{SS} to V_{DD} CMR as mentioned in the GLVDS specifications [1]. However, the CMR of the GLVDS receiver is adequate to receive the low output common-mode values of the GLVDS and OSDS transmitters.

4.2 Transient Simulations of the I/O Circuit On-Chip Testbench

When the DC operating specifications of the I/O transmitters and receivers have been satisfied in simulation, the high-frequency transient performance of the circuits must be simulated. In addition to the I/O circuits, the on-chip I/O testbench circuits must also be simulated to operate at the desired I/O test frequencies. This section will present the I/O testbench circuits and their HSPICE transient simulation results. Then the HSPICE simulations of the I/O circuits under test within the testbench will be given. It is these transient simulation results which will be compared to measured results when the circuits are fabricated and measured.

4.2.1 The On-Chip Testbench Without I/O Circuits

The first component of the on-chip I/O testbench is the ring-oscillator circuit which provides the high-frequency CMOS stimulus for the transmitter circuit under test. Fig. 4.13 shows the Cadence schematic of one of the ring oscillators titled 'ringosc2' consisting of 9 inverters.

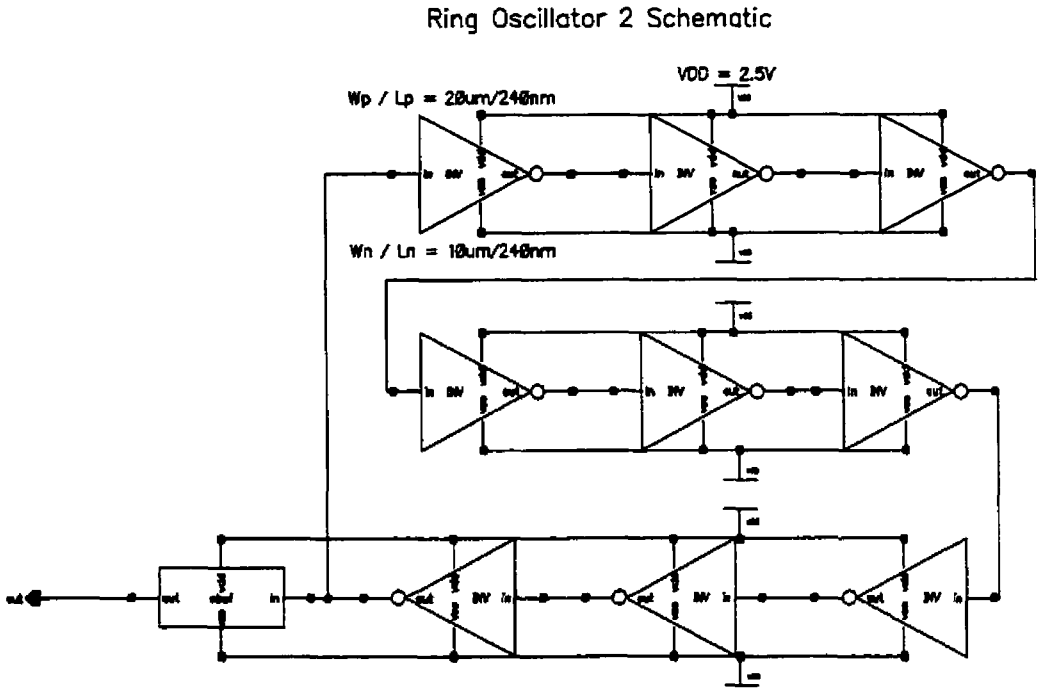

Figure 4.13: Ring Oscillator 2 Circuit Schematic

Two other ring oscillators were designed for the test system, one with 7 inverters (ringosc1) and the other with 11 (ringosc3). During transient HSPICE simulations with typical device models, the three inverters produced CMOS-level outputs at the frequencies described in Table 4-7. Table 4-7 also provides the simulated output frequencies of the ring oscillators for the SS and FF device models.

Table 4-7: Ring Oscillator Output Frequencies Simulated in HSPICE

Oscillator Name	Number of Inverters	Output Frequency (SS)	Output Frequency (TT)	Output Frequency (FF)
ringosc1	7	1.188 GHz	1.528 GHz	1.933 GHz
ringosc2	9	930.0 MHz	1.194 GHz	1.554 GHz
ringosc3	11	762.4 MHz	979.8 MHz	1.275 GHz

The second non-I/O component of the on-chip I/O testbench is the ÷128 prescaler circuit. The prescaler block design shown in Fig. 4.14 was derived from literature [10]. The prescaler is composed of 7 cascaded T flip-flops. The input frequency must toggle the first flip-flop 2^7 (128) times before the output flip-flop toggles once. Therefore, the prescaler will output a CMOS signal at 128th of the input frequency.

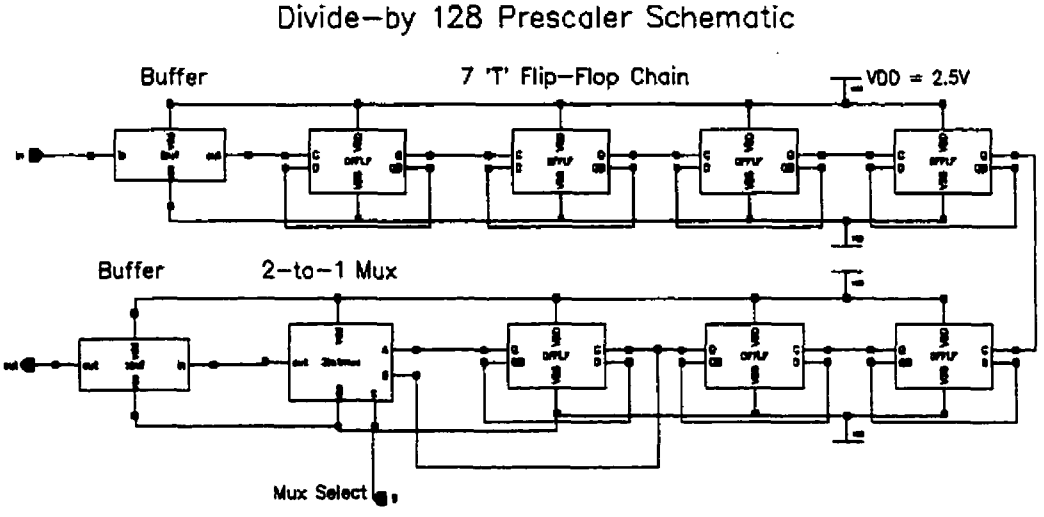

Figure 4.14: ÷128 Prescaler Circuit Schematic

At the output of the prescaler is a 2-to-1 mux which multiplexes the output of the 6th and 7th flip-flop allowing for ÷64 or ÷128 output frequency selection. For the remainder of this thesis, it will be assumed that the prescaler is set for ÷128 operation. The prescaler was transient simulated in HSPICE with each of the three ring oscillator circuits as the input stimulus. Table 4-8 presents the output frequency of the prescaler for each ring oscillator input over the SS, TT, and FF process corners.

Table 4-8: Prescaler Output Frequencies for Ring Oscillator Inputs as Simulated in HSPICE

Input Oscillator	Output Frequency (SS)	Output Frequency (TT)	Output Frequency (FF)
ringosc1	9.301 MHz	11.95 MHz	19.80 MHz
ringosc2	7.273 MHz	9.330 MHz	12.14 MHz
ringosc3	5.960 MHz	7.660 MHz	9.945 MHz

Each of the recorded frequencies in Table 4-8 are 128^{th} of the corresponding oscillator frequencies in Table 4-7. Therefore, the ÷128 prescaler circuit operates in simulation for the ring oscillator frequency inputs.

Several control circuits with the ring oscillators connected directly to the prescaler will be fabricated with the I/O testbench circuits. The outputs of the control circuits will provide a reference for the frequencies which should be output from the I/O testbenches with the same ring oscillator stimulus.

4.2.2 The On-Chip Testbench With I/O Circuits

Once the desired ring oscillator and prescaler operation has been verified in simulation over the typical and extreme process corners, the I/O transmitters and receivers can be simulated in the I/O testbench with some confidence. The methodology for the transient simulations of the I/O transmitter/reciever pairs within the I/O testbench is:

1) Simulate the transmitter/receiver within the I/O testbench.
2) If the output of the I/O testbench matches the output of the appropriate

ring-oscillator/prescaler pair simulation from 4.2.1, then ready for fabrication.

3) Else, the transmitter/receiver circuit is inoperable at the test frequency and may require re-design in DC simulation, and re-simulation in transient mode.

The final testbench designs for each of the I/O standards under test will be presented in this section with their HSPICE transient simulation results.

PECL I/O Testbenches

Fig. 4.15 shows the Cadence symbolic view of an I/O testbench with the PECL transmitter and receiving op-amp under test. This testbench is configured with the ringosc2 oscillator as the test stimulus, and will be referred to as the PECL testbench 2.

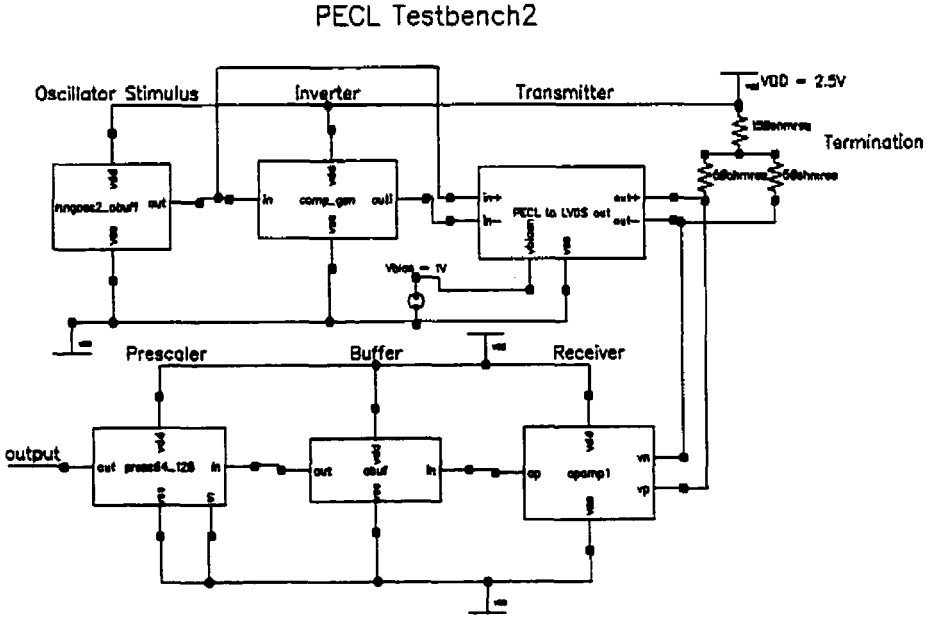

Figure 4.15: Symbolic Schematic of the PECL Testbench 2

All three of the PECL testbenches were setup as in Fig. 4.15 and transient simulated with HSPICE for the TT, SS and FF device models. Table 4-9 gives the simulated system output frequency for each of the testbenches over each of the process corners.

Table 4-9: HSPICE Simulated PECL Testbench Output Frequencies

PECL Testbench Name	Output Frequency (SS)	Output Frequency (TT)	Output Frequency (FF)
Testbench 1	9.300 MHz	11.95 MHz	15.48 MHz
Testbench 2	7.280 MHz	9.340 MHz	12.12 MHz
Testbench 3	5.978 MHz	7.672 MHz	9.941 MHz

The simulated frequencies in Table 4-9 are very close to the simulated output frequencies of the I/O testbench with no I/O circuits under test in Table 4-8. This 'transparency' of the PECL transmitter and receiver in the I/O testbench confirms their simulated operability at the ring oscillator test frequencies.

LVDS I/O Testbenches

Fig. 4.16 displays the Cadence symbolic view of the LVDS testbench 2. The I/O circuits under test are the LVDS transmitter and the LVDS receiving op-amp, terminated with the appropriate 100Ω resistance.

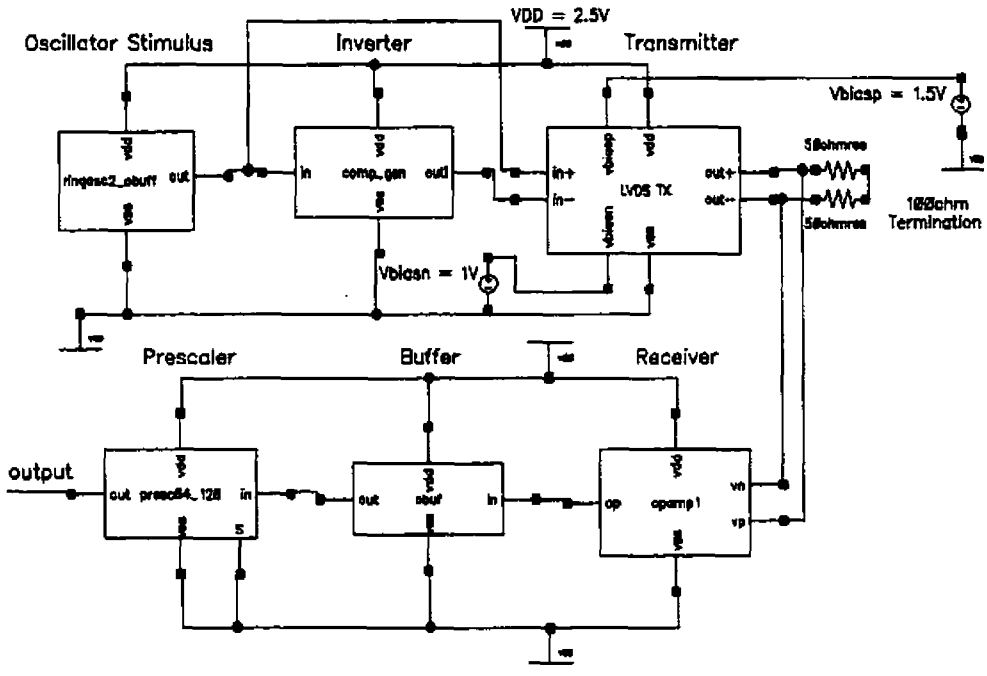

Figure 4.16: Symbolic Schematic of the LVDS Testbench 2

The testbench of Fig. 4.16, and the remaining two LVDS testbenches were transient simulated in HSPICE for the typical, slow and fast process device models. Table 4-10 presents the simulated output frequencies for each of the LVDS testbenches.

Table 4-10: HSPICE Simulated LVDS Testbench Output Frequencies

LVDS Testbench Name	Output Frequency (SS)	Output Frequency (TT)	Output Frequency (FF)
Testbench 1	9.280 MHz	11.96 MHz	15.51 MHz
Testbench 2	7.274 MHz	9.340 MHz	12.15 MHz
Testbench 3	5.982 MHz	7.674 MHz	9.974 MHz

The simulated frequencies from Table 4-10 are similar to those found in Tables 4-8 (no I/O circuits) and 4-9 (PECL testbench). The transparency of the LVDS transmitter and

receiver within the simulated testbenches assures their operability at the ring oscillator test frequencies in simulation.

GLVDS I/O Testbenches

The Cadence symbolic view of the GLVDS testbench 2 is shown in Fig. 4.17. The circuits under test are the GLVDS transmitter and receiver with the receiver's in-circuit termination set to high-impedance (V_{GS}=0V for termination transistors).

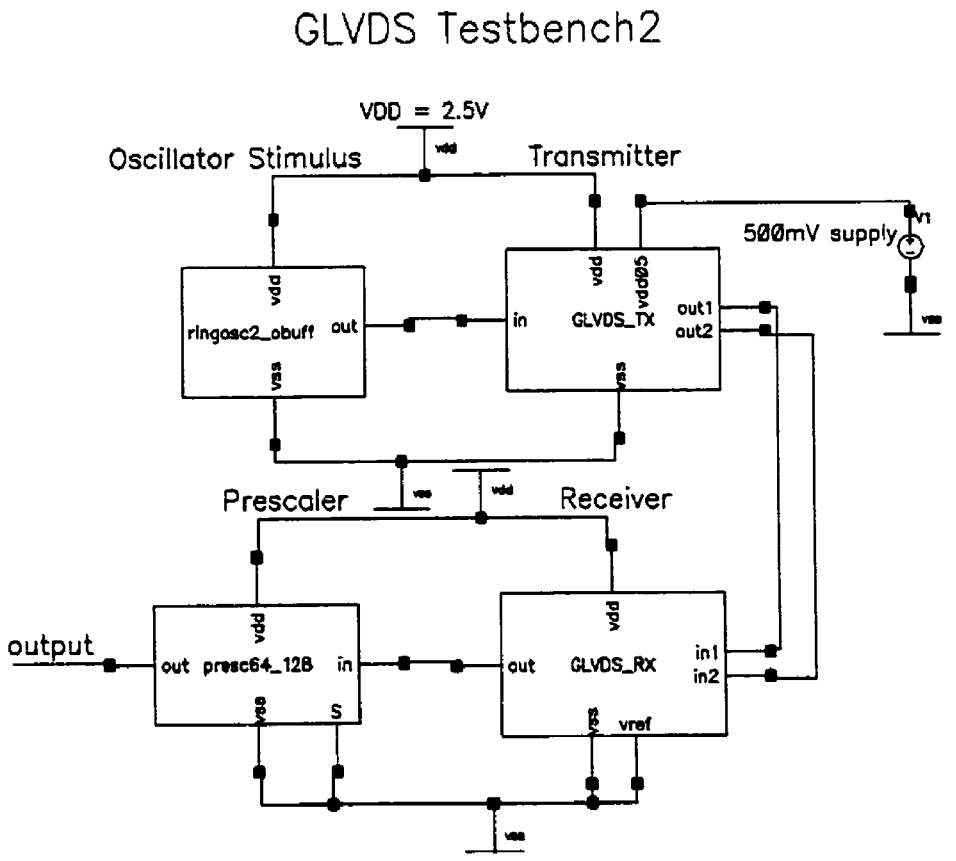

Figure 4.17: Symbolic Schematic of the GLVDS Testbench 2

All three of the GLVDS testbenches were transient simulated in HSPICE for the typical and corner device models. Table 4-11 details the simulated output frequencies from each of the GLVDS testbenches.

Table 4-11: HSPICE Simulated GLVDS Testbench Output Frequencies

GLVDS Testbench Name	Output Frequency (SS)	Output Frequency (TT)	Output Frequency (FF)
Testbench 1	9.297 MHz	11.94 MHz	15.49 MHz
Testbench 2	7.273 MHz	9.342 MHz	12.12 Hz
Testbench 3	5.973 MHz	7.670 MHz	9.951 MHz

The output frequencies of each of the GLVDS testbenches match those of the outputs in previous tables. Therefore, the GLVDS transmitter/receiver pair operate in simulation at the ring oscillator test frequencies.

OSDS Transmitter and Receiver Testbenches

The OSDS testbench 2 is shown in Fig. 4.18 in the Cadence symbolic schematic view. The I/O circuits under test are the OSDS transmitter and the GLVDS receiver. The two 50Ω termination resistors have been included and the GLVDS receiver in-circuit termination set to high-impedance.

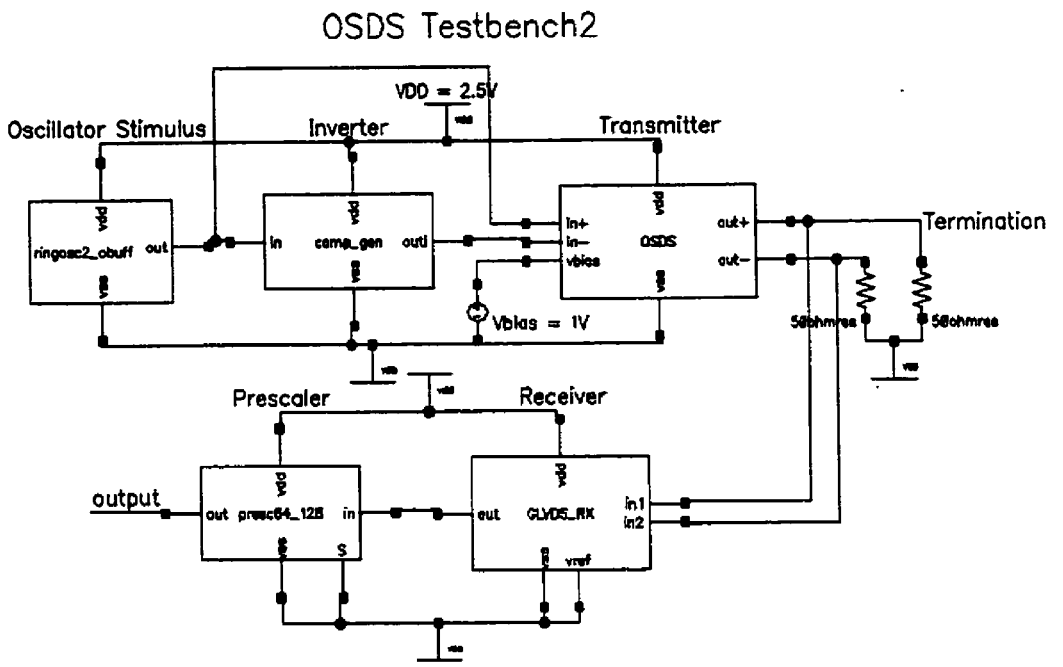

Figure 4.18: Symbolic Schematic of the OSDS Testbench 2

All three of the OSDS testbenches were transient simulated in HSPICE for the TT, SS and FF device models. Table 4-12 presents the simulated output frequencies from each of the OSDS testbenches.

Table 4-12: HSPICE Simulated OSDS Testbench Output Frequencies

OSDS Testbench Name	Output Frequency (SS)	Output Frequency (TT)	Output Frequency (FF)
Testbench 1	9.299 MHz	11.95 MHz	15.65 MHz
Testbench 2	7.275 MHz	9.331 MHz	12.14 MHz
Testbench 3	5.971 MHz	7.673 MHz	9.958 MHz

The OSDS testbench output frequencies of Table 4-12 match those from Tables 4-8 to 4-11. Therefore, the OSDS transmitter and GLVDS receiver circuits are operable in simulation for the ring oscillator input frequencies.

To this point, the I/O circuits and I/O testbenches have been DC and transient simulated in HSPICE to meet the specifications set out in chapters 2 and 3. The I/O circuits and testbench can now be physically designed with some confidence that they too will operate after fabrication as they did in simulation. However, to ensure the desired operation of the fabricated circuits, the physical design must be laid out to match the corresponding simulated design as close as possible.

4.3 Simulation of I/O Circuit Maximum Frequencies of Operation

The I/O circuits studied in this thesis were simulated in HSPICE to determine their maximum simulated frequency of operation. The results offer a relative comparision in simulation-space of which are the faster I/O circuits.

Fig. 4.19 shows the simulation setup for determining the PECL circuit's maximum operating frequency. Two complementary pulse sources provide the stimulus for the transmitter under test. The transmitter and receiver under test are coupled via 50Ω transmission lines and appropriate termination for the I/O standard.

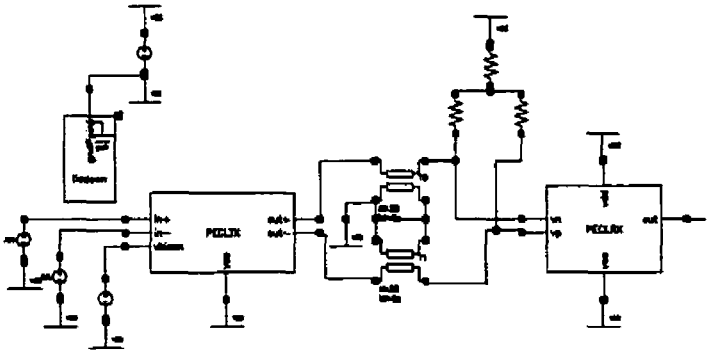

Figure 4.19: Simulation Setup for Maximum Operating Frequency Determination

The I/O circuits under test were simulated at 1GHz input increments starting at 1GHz and ending when the receiver output is no longer correct. The output is considered incorrect when it is no longer a periodic pulse train as are the transmitter inputs. Table 4-13 shows the maximum frequency at which each I/O circuit pair was operable.

Table 4-13: Comparison of Maximum I/O Circuit Frequencies in HSPICE

I/O Circuit Type	Maximum Operating Frequency (GHz)
PECL (LVDS levels)	4GHz
LVDS	4GHz
GLVDS	6GHz
OSDS	10GHz

Both the PECL and the LVDS design were capable up to 4GHz. Each of these designs have the same I/O levels and the same receiver circuit. Therefore, their identical frequency limits may be a reflection of the LVDS I/O standard itself, or just the maximum operating frequency of the PECL/LVDS receiver.

The GLVDS transmitter was capable up to 6GHz in simulation while the OSDS transmitter operated up to 10GHz. As both of these transmitters used the same receiver circuit, their differences in operating frequencies is a direct reflection of the transmitter circuit performance. The GLVDS transmitter may offer the lowest power to bandwidth ratio up to 6GHz, but the OSDS transmitter can continue past 6GHz regardless of power consumption.

5.0 Physical Design of the I/O Circuits and Testbench

Once the I/O testbench and transmitter/receiver circuits have met their design specifications through simulation over the typical, slow and fast process corners, they are ready for layout. The technology which the circuits are being fabricated in is the TSMC 0.25μm CMOS process. Due to the necessity of precise biasing for most of the I/O circuits, consideration must be made to ensure that the physically designed circuits will closely match the circuits from simulation. The layout techniques utilized in ensuring a close match between fabricated and simulated circuits fall in the category of Design for Manufacturability (DFM) [12]. In the layout of the I/O circuits, several common DFM techniques were used. However, other common DFM methods were not implemented due to more important design issues. This section will present the layout designs for each of the major testbench and I/O circuit components. Once the layout is presented, the rationale behind each of the designs will be explained and defended.

5.1 I/O Circuit Layout

To provide as close a match as possible between the physical and simulated designs, several DFM layout techniques have been implemented in the I/O circuit layouts. There are several DFM techniques which are commonly used [12]:

1) Uniform contact coverage in drain and source areas.
2) A common-centroid geometry of transistors to provide close device matching.
3) Use of dummy-transistors to prevent poly over-etch which causes reduced device length.

Points (1) and (3) above were consistently implemented in the I/O circuit designs. Accommodating large current conduction proved to be a DFM constraint particular to the high-current biased differential I/O circuits. The high current drive through the I/O circuits forced the use of wide metal interconnects to prevent aluminum electro-migration. This high-current constraint often made it difficult to efficiently implement point (2) in the I/O circuit designs.

5.1.1 I/O Circuit Current Density Design Constraints

Most of the I/O transmitters have a similar circuit topology: a current source/sink providing current which is steered between outputs by drive transistors. This current-steering design results in the entire bias current passing through all transistors in the design at some point in time. Due to low termination resistance (50Ω), drive currents of 4-10mA are necessary to generate the standard output swing values for the I/O standards in this thesis. Therefore, each transistor must be physically designed to accommodate large bias currents.

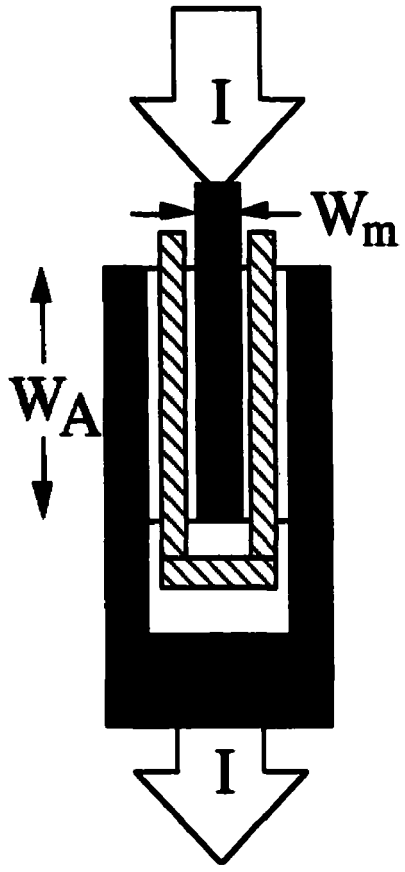

Figure 5.1: Example of a Split-Drain Transistor Layout

Fig. 5.1 illustrates the design process for high-current device layout. The design calls for a bias current I, and the process rules provides the maximum current density value J_{max} for the metallization layers. Therefore, the minimum number of metal 'fingers' per minimized drain area (n_m) which can safely conduct the bias current is determined by eq. 5.1.

$$n_m = \frac{I}{J_{\max} \cdot W_m} \tag{5.1}$$

where W_m is the maximum metal width over a drain/source allowed by the process design rules while maintaining minimum drain/source area.

The result of designing the devices for high-current conduction is that every device must have the same number of metal fingers regardless of the transistor's aspect ratio. Therefore, the number of input metal fingers will be fixed and only the active region width W_A can be varied to fit the device to the desired transistor dimensions.

If a transistor is relatively small in width but must conduct large currents, the active region width W_A must be shrunk to a point where it violates process rule or just makes the circuit very oblong. It then becomes more economical from an IC area point-of-view to layout the device in a single-drain configuration as seen in Fig. 5.2.

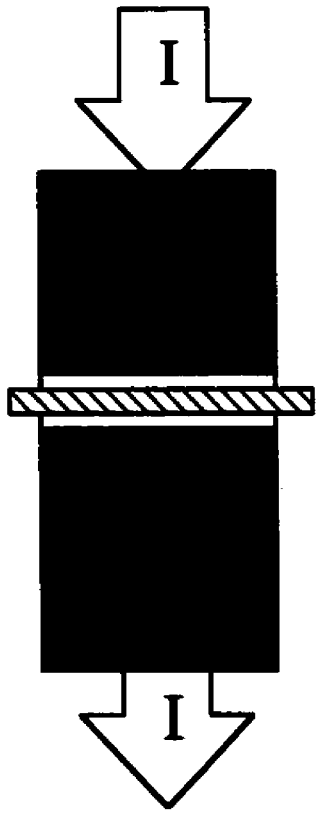

Figure 5.2: Example of a Single-Drain Transistor Layout

The single-drain layout style easily accommodates large currents and can offer a more compact layout than the split-drain style if the transistor W is small and I is large. However, the single-drain layout style does not allow as close transistor-matching as common-centroid geometry layouts which require a split-drain layout style.

It is the I/O transmitter circuits which are required to conduct large output currents, and each transistor in their design must accommodate this current. In all of the I/O transmitter physical designs for this thesis, the transistors were designed in a split-drain fashion where possible. The only exceptions are the LVDS and OSDS designs where there are small drive transistors (W < 50μm). The small drive transistors in the LVDS and OSDS transmitters were laid out in the single-drain style of Fig. 5.2 to accommodate the high output currents while keeping the overall circuit dimensions as compact as possible.

5.1.2 PECL Transmitter Layout

The layout design of the PECL transmitter is shown in Fig. 5.3 with each transistor clearly marked. Each of the transistor layouts are of a split-drain type with dummy poly-gates at the edges to prevent the over-etching of the outermost gate polys. The inverter at the left of the transmitter provides the complementary CMOS level to the transmitter inputs.

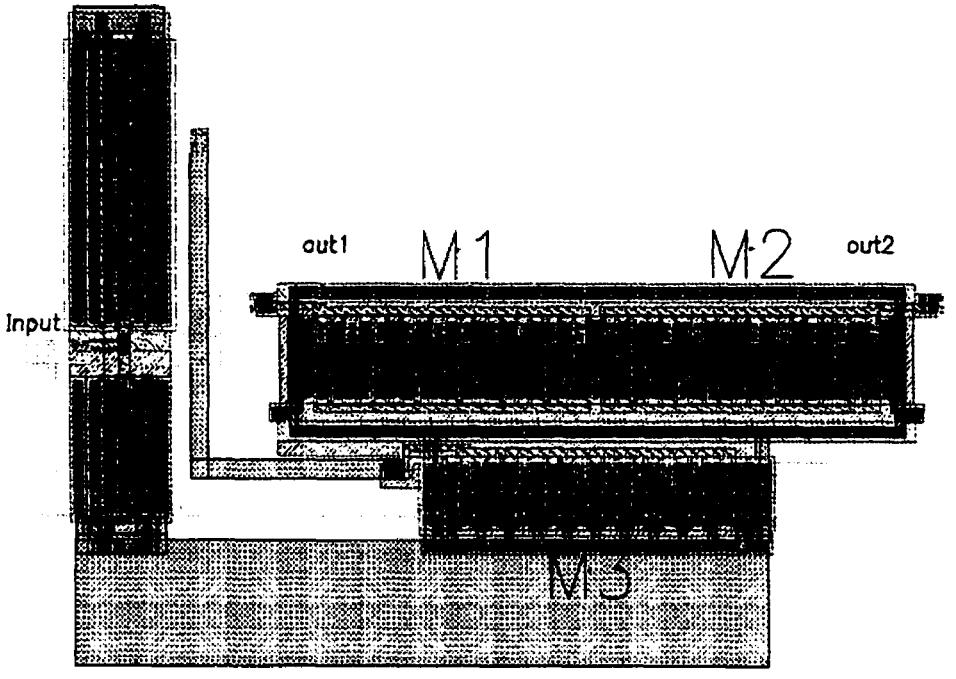

Figure 5.3: PECL Transmitter Layout

The maximum output swing the PECL transmitter was DC simulated at ~450mV (FF simulation) resulting in a necessary bias current of 9mA in a 50Ω terminated environment. Eq. 5.1 was utilized to layout the transistors for a possible 10mA conduction as a safety margin.

The drain and source areas were minimized within process rules to reduce circuit node capacitances. The contacts were placed to maximum density within the drain and source areas to minimize drain and source resistance.

The driving transistors M1 and M2 were not laid out in a common-centroid geometry to increase their matching. The common-centroid geometry would require the interdigitating of the M1 and M2 source/drain areas throughout the active region.

Implementing the common-centroid geometry would require the use of another metal layer and more current density calculations. The transistors M1 and M2 are large current steering transistors with negligible 'on-resistance' and do not require very close matching after fabrication. Therefore, it was decided to keep the M1 and M2 devices separate for ease of the PECL transmitter layout. The common-centroid geometry was not used in other I/O circuit designs for the same current-density reasons.

The few transistors in the PECL transmitter design and their simplicity of connection makes the PECL layout compact and with short interconnections. Therefore, the PECL transmitter circuit topology is very good from the layout and IC real-estate perspective, even within the high-current design constraints.

5.1.3 LVDS Transmitter Layout

Fig. 5.4 shows the layout of the LVDS transmitter circuit with each transistor marked. The bias transistors M5 and M6 are laid out in a split-drain fashion with dummy-gates at the device exterior. The remaining drive transistors M1-M4 were laid out as single-drain devices with dummy-transistors at the active region edges.

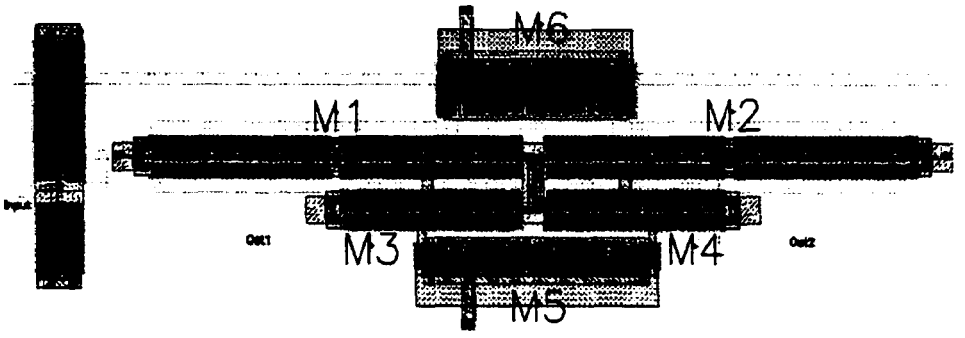

Figure 5.4: LVDS Transmitter Layout

The maximum FF simulated output swing of the LVDS transmitter was 417mV. In the typical LVDS 100Ω terminated output scheme, a 417mV swing corresponds to a 4.17mA output current. To safely accommodate a possible 4.17mA, the transistors in Fig. 5.4 were designed to conduct 5mA in accordance with Eq. 5.1.

The reason for the separated, non-split drain driving transistors is due to metallization current density issues. The aspect ratio of the driving transistors is 25μm/240nm. To layout the driving transistors in a split-drain configuration with enough metal fingers to accommodate 5mA, the resultant active region width, W_A, would be less than 1μm. With a 1μm wide active region, the physical design would behave differently from the simulated design due to the necessity of simulating with different models corresponding to many narrow-channel transistors connected in parallel. All active devices in the LVDS transmitter design were generated with minimized source/drain areas with maximum contact density to reduce RC delays at the circuit nodes.

The number of transistors and their connectivity in the LVDS circuit topography do not make their layout simple. Such large biasing transistors and output current with small

driving transistors forced a layout which is not economical in terms of IC real-estate. A better design from the physical design perspective would incorporate larger driving transistors (comparable to the bias transistor dimensions) which would fit more easily in a split-drain configuration, reducing the overall area of the layout.

5.1.4 PECL/LVDS Receiver Layout

The PECL/LVDS receiving single-stage op-amp is shown in Fig. 5.5. All devices were designed with split-drain layouts and dummy transistors at the active region edges.

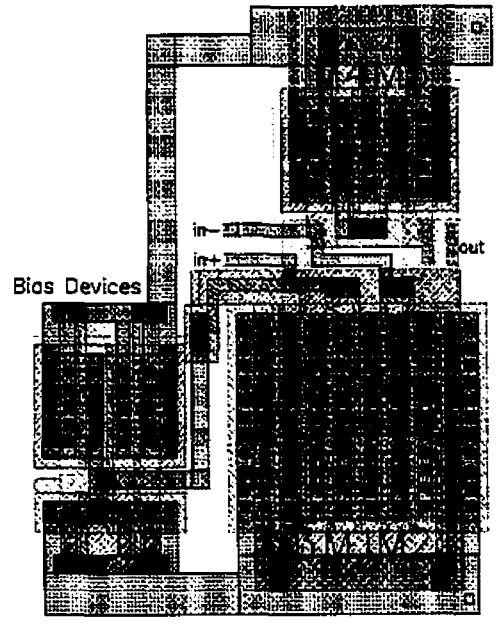

Figure 5.5: PECL/LVDS Receiver Layout

Clearly marked in Fig. 5.5 are the input differential pair M1 and M2, the current sink M3, and the pMOS mirror loads M4 and M5. The two resistor-configured MOS devices at the left of Fig. 5.5 provide voltage biasing for the M3 current sink. The symmetry and small device aspect ratios of the op-amp receiver makes its layout very compact in comparison with the large current-mode GLVDS receiver.

5.1.5 GLVDS Transmitter Layout

The physical design of the GLVDS transmitter in the TSMC 0.25μm CMOS technology is shown in Fig. 5.6. All transistors in this design are of a split-drain layout, with dummy-transistors at the edges of each active region to prevent poly over-etch. The four nMOS driving transistors M1-M4 are clearly marked. The remaining devices in the layout are inverters to generate complementary CMOS input signals for the transmitter.

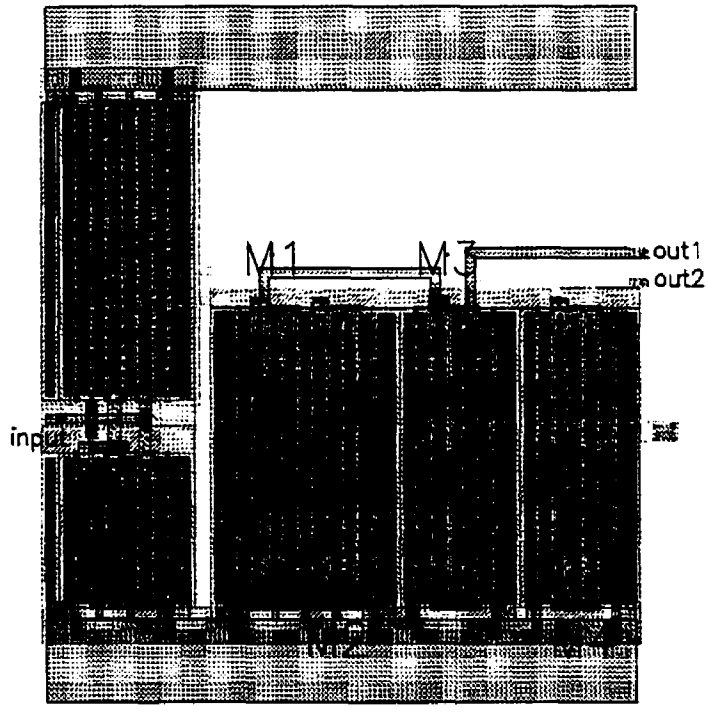

Figure 5.6: GLVDS Transmitter Layout

Through DC simulation, it was found that the highest current through the GLVDS transmitter is <2mA. Eq. 5.1 was used to design the transistors in Fig. 5.6 in a split-drain fashion for 2mA conduction. The drain and source areas were minimized and populated with the maximum number of contacts to reduce nodal RC delays.

The few transistors in the GLVDS transmitter design make it a compact layout. However, the 500mV supply to the nMOS transistors M1-M4 make it difficult to incorporate the input inverters and drive transistors into the same active region and reduce the overall circuit area.

5.1.6 OSDS Transmitter Layout

The 0.25µm CMOS physical design of the OSDS transmitter is shown in Fig. 5.7. The transmitter layout is much the same as the PECL circuit with the split-drain layout of the biasing transistor M3. The driving transistors M1 and M2 were laid out as single-drain transistors due to their very small size (25µm/240nm) and high conduction. As was the case for the LVDS transmitter, a split-drain style of layout for M1 and M2 would result in undesired narrow-width effects in their performance after fabrication. All active regions were laid out with dummy-transistors at their exterior to prevent the over-etch of device gates.

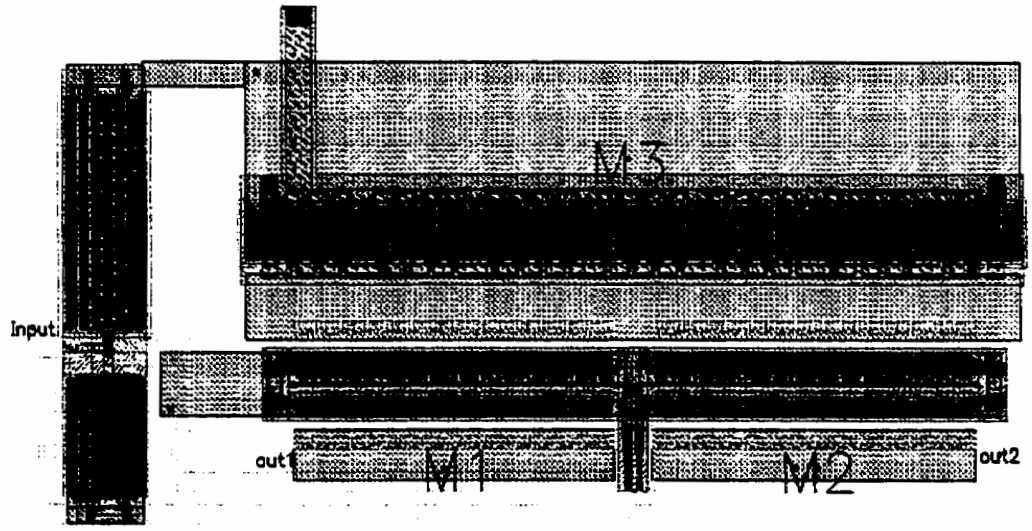

Figure 5.7: OSDS Transmitter Layout

The FF DC simulations of the OSDS transmitter yielded a maximum differential output swing of 562mV. In the typical 50Ω terminated environment, the 562mV corresponds to a transmitter output current of 11.2mA. Eq. 5.1 was used to design the OSDS transmitter transistors for 12mA conduction as a safety margin. As in the previous designs, the drain and source areas were reduced in the design and the contact density maximized to minimize transistor parasitics.

As was the case for the PECL transmitter design, the few devices and simple connectivity of the OSDS transmitter made its layout simple and compact. Of the I/O transmitters researched in this thesis, the PECL and OSDS transmitters consume the least amount of IC area.

5.1.7 GLVDS Receiver Layout

The GLVDS receiver layout design is shown in Fig. 5.8. Due to the number of transistors in the design, circuit devices have not been labeled. All of the devices were laid out in a split-drain fashion with a single active region for both nMOS and pMOS transistors. Dummy gates were added to the edges of each active region, drain areas were minimized, and drain/source contact density maximized.

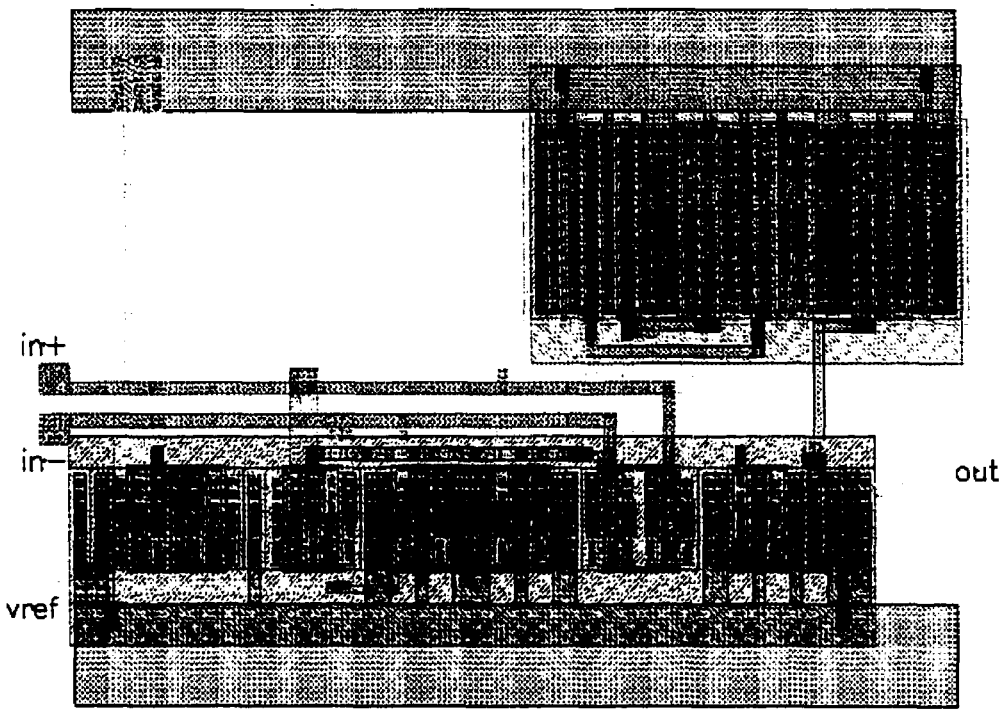

Figure 5.8: GLVDS Receiver Layout

The layout of the GLVDS receiver was not complicated with current density issues. Normally the input termination transistors would be designed to conduct a current determined by the ratio of the GLVDS signal swing and the characteristic impedance of the signaling environment. However, in the on-chip testbench the termination transistors will be set to maximum impedance as transmitter-receiver interconnects need not be modeled as transmission lines for the frequencies under test.

The remainder of the receiver devices conduct low currents for any signaling environment and were easily laid out into a continuous active region. The result is a relatively compact layout when considering the number of transistors within the design.

5.2 I/O Testbench Layout

The remaining circuits for layout in this thesis are the components of the I/O testbench: the ring oscillator and the prescaler. The physical designs of trivial components such as buffers and inverters will not be shown or described. The testbench circuits all drive high-impedance loads and do not require a high-current design methodology as was the case with the I/O transmitter circuits.

5.2.1 Ring Oscillator Layout

The layout of the ring oscillators was not difficult due to the repetitive nature of its design. The ring oscillator 2 layout in Fig. 5.9 was created by first laying out an inverter and then copying it for the remaining inverters in the design.

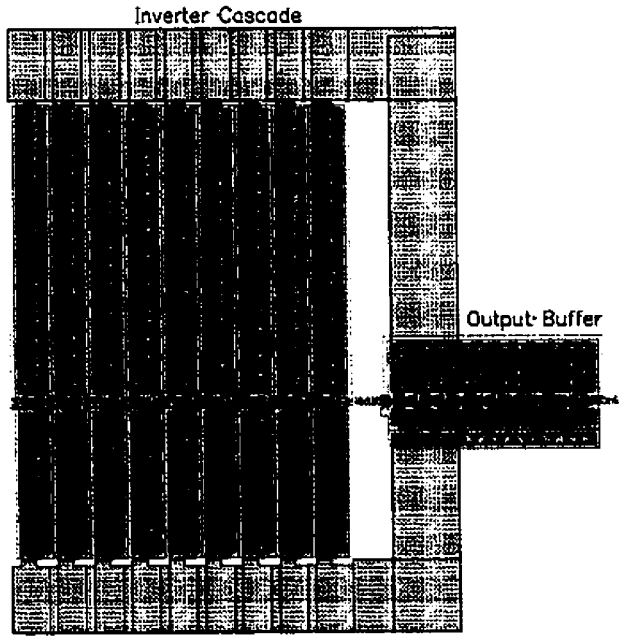

Figure 5.9: Ring Oscillator 2 Layout

The ring oscillator 1 and 3 layouts were created in the same manner as for the ring oscillator 2. As the output frequency of ring oscillator circuits is inherently sensitive to process variation (see Table 4-7), it is very important to implement DFM layout techniques to minimize process sensitivity. In the Fig. 5.9 layout, dummy gates were implemented and contacts were maximized in the active devices.

5.2.2 ÷128 Prescaler Layout

The layout method for the prescaler is similar to the method used to layout the ring oscillators. The prescaler is a cascade of 7 T flip-flops, so an initial T flip-flop was designed, copied, and cascaded to build the layout. The 2-to-1 mux and an output buffer are laid out on the right of the prescaler in Fig. 5.10.

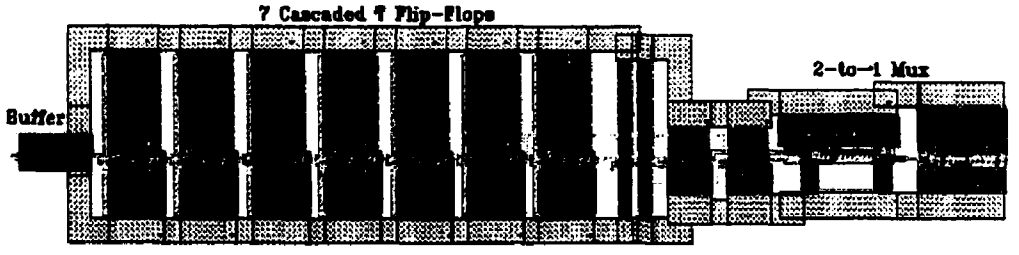

Figure 5.10: ÷128 Prescaler Layout

As was the layout technique for the oscillators, dummy gates and maximum drain/source contact density were used in the prescaler layout.

5.2.3 On-Chip Termination Layout

To test the I/O transmitters and receivers in the testbench, the resistive termination for the standards must be implemented on chip. The common 50Ω signaling environment for the I/O circuits will be assumed in this thesis. In simulations of the PECL, LVDS and OSDS circuits, 50Ω and 150Ω (for PECL) resistors are needed as termination. Therefore a single 50Ω resistors was laid out in an n-doped polysilicon layer shown in Fig. 5.11. The 150Ω resistor for the PECL testbenches was implemented with three resistors from Fig. 5.11 in series.

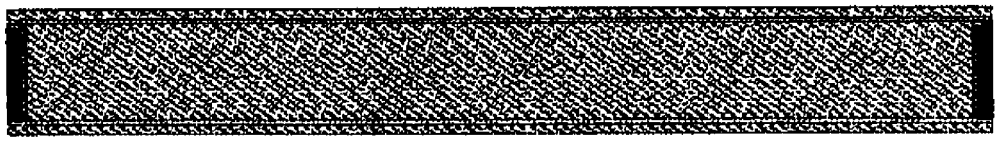

Figure 5.11: 50ohm Resistor Layout

A disadvantage of on-chip resistive termination is the sensitivity of sheet resistances to process variation. The variation of the polysilicon sheet resistance in the TSMC 0.25μm CMOS technology is ±30% and it is the only suitable layer for a small resistance of 50Ω. However, I/O testbench simulations were re-performed for each I/O standard with ±30% variation of the termination resistances. The results of these simulations showed the I/O circuits to still operate although the transmitted voltages were not to standard specifications.

5.2.4 Example I/O Testbench Layout

As an example of a complete I/O testbench layout, the OSDS testbench 2 is shown in Fig. 5.12. Each component of the testbench was laid out at separate times with no standard

cell dimensions. On a typical IC where layout area is precious, each testbench component would be designed to standard cell heights and the supply buses would run as horizontal metal lines. In the test chips through CMC, the ICs are extremely pad-limited. That is, there are so many I/Os in the test circuits that the IC dimensions are determined by the number of necessary I/O pads rather than the total circuit area. Therefore, a 'meandering' V_{DD} bus is an allowable deviation from standard conservative layout practice on the test chips, as available chip area is plentiful.

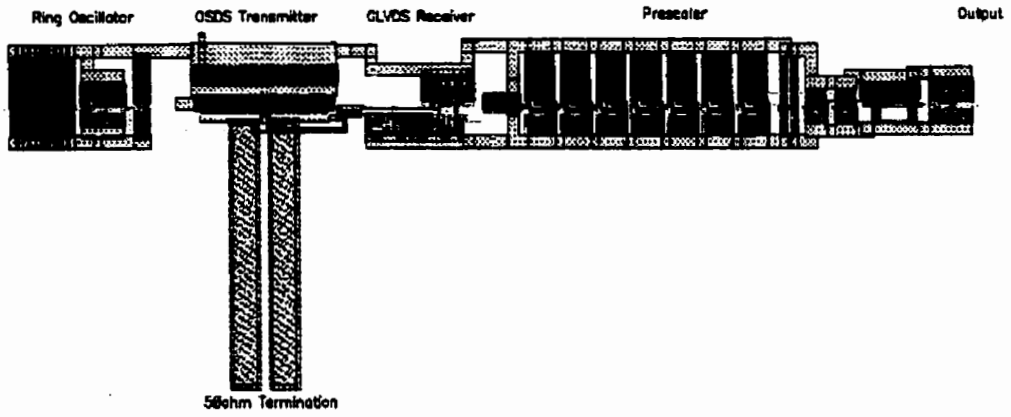

Figure 5.12: OSDS Testbench 2 Layout

5.3 Results of I/O Circuit and Testbench Layout

Two chips were submitted for fabrication in the TSMC 0.25µm CMOS technology through CMC: ICESFMK5 (MK5) and ICESFMK6 (MK6).

The MK5 chip contained:

- I/O testbenches 1, 2 and 3 (no transmitters/receivers).

- The GLVDS testbenches 1, 2 and 3.
- The GLVDS transmitter and receiver for DC testing.

The MK6 chip contained:

- I/O testbenches 1 and 3 (no transmitters/receivers).
- The PECL, LVDS, GLVDS and OSDS testbenches 1 and 3.
- Each of the transmitters and receivers for DC testing.

Each of the circuits were laid out and submitted for fabrication after their DC and transient performances were verified in simulation as described in chapter 4.

A major problem encountered in the LVDS and OSDS transmitter designs was designing relatively small devices (< 50um wide) for large current conduction. To layout these small devices in a split-drain configuration while accommodating high currents would result in devices affected by narrow-width device effects. Therefore, some device layouts did not use all common DFM layout techniques because of current density considerations.

The I/O circuit and testbench layouts were designed to match the simulated designs as close as possible. Compact design, high-current accomodation, dummy-gates, minimized drain areas, and maximum device contact density are all DFM techniques implemented to match the physical and simulated designs. How close the two designs are matched will not be entirely known until the circuits are fabricated and tested.

6.0 Measured Results of the I/O Circuits and the I/O Testbench

The two ICs fabricated in the 0.25µm CMOS technology which contained I/O circuits for testing are named ICESFMK5 (MK5) and ICESFMK6 (MK6). These chips were fabricated through the CMC 9902CE and 9903CE fabrication runs respectively. MK5 contained I/O testbench components, GLVDS testbench circuits and GLVDS I/O circuits. The MK6 IC contained both testbench and I/O designs for the PECL, LVDS, GLVDS and OSDS circuits described in Chapter 4.0.

This chapter describes the DC test methodology and equipment used to determine the switching thresholds and output voltage levels of the I/O circuits. A similar description of the transient test methodology and equipment used in determining the I/O testbench output frequencies is also provided. Chapter 6.0 concludes with a comparison of physical measurements and the simulated measurements conducted in Chapter 4.0. This chapter will also provide a description of problems encountered during circuit testing and attempts to explain the erroneous behaviour.

6.1 IC Testing Methodology

Both DC and transient tests are necessary to evaluate the physical circuit parameters and compare with the corresponding simulated values from Chapter 4.0. The equipment available for testing the fabricated ICs are:

- HP 5155A Semiconductor Parameter Analyzer (SPA).
- Two dual power-supplies.

- Tektronix 500MHz oscilloscope with two 1.5pF active probes.
- 44-CQFP test fixture.

The following two sections will describe how this equipment was used in DC and transient tests.

6.1.1 DC Test Method

DC testing is necessary for testing the input switching levels, output current and output voltage levels for I/O transmitters. I/O receiver circuits are DC tested for input sensitivity and CMR. The DC test method for I/O transmitters using the SPA and 44-CQFP test fixture is shown in Fig. 6.1.

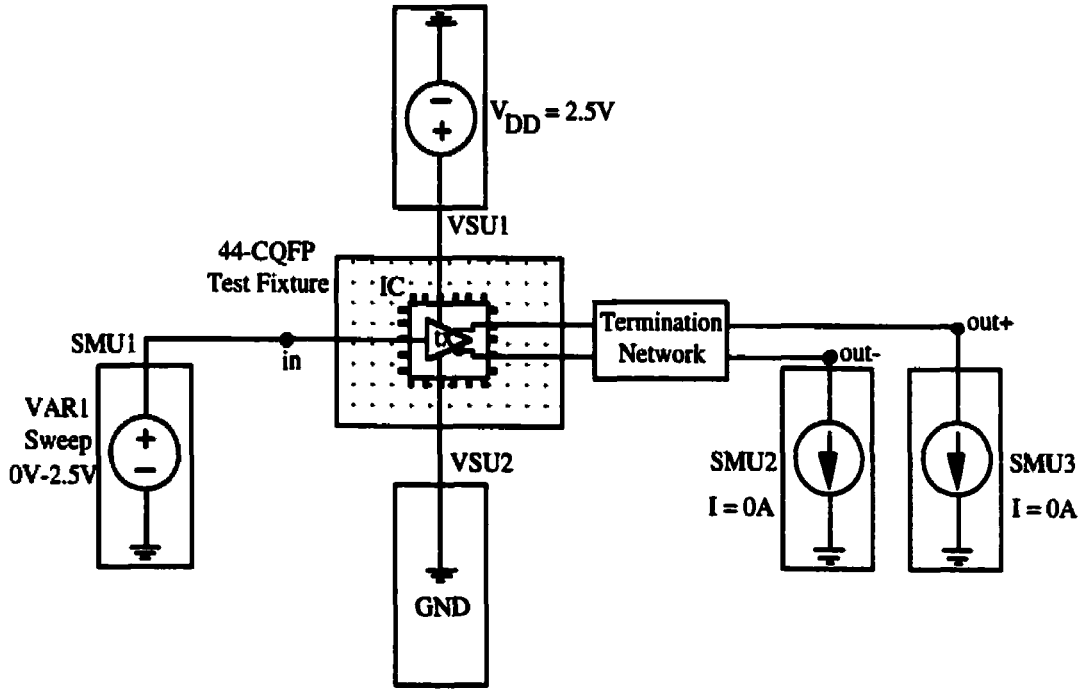

Figure 6.1: I/O Transmitter DC Test Method

Fig. 6.1 shows each SPA SMU channel and graphically represents how each channel is configured. Each SMU monitors both its output current and output voltage as data.

Therefore those SMUs configured as a 0A current source are used only as voltage sampling channels. Only one input SMU is necessary for an I/O transmitter, as each transmitter's input is connected on-chip with an inverter to supply complementary CMOS signals. In the Fig. 6.1 test, SMU1 is swept between V_{SS} and V_{DD}=2.5V while monitoring the output voltages. For the current-biased PECL, LVDS and OSDS designs, appropriate termination was added to the transmitter outputs so that output voltages could be measured.

The DC test method for I/O receivers using the SPA and 44-CQFP test fixture is shown in Fig. 6.2.

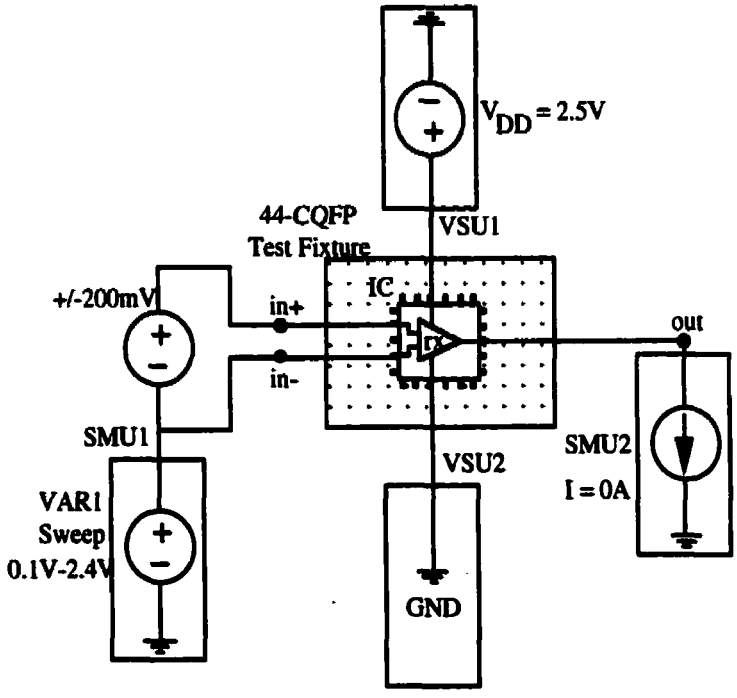

Figure 6.2: I/O Receiver DC Test Method

In the receiver DC tests in+ and in- are kept at a 200mV difference. Multiple tests are performed with input common-mode voltages between 100mV and 2.4V at 100mV

intervals. This DC test is designed to confirm a 200mV input sensitivity of the receiver and each test will provide a point on a CMR graph similar to the simulated CMR graph in Fig. 4.6.

6.1.2 Transient Test Method

Transient testing is necessary for determining whether the I/O testbench components and I/O testbenches output appropriate frequencies as simulated in Chapter 4.0. The transient test method is shown in Fig. 6.3.

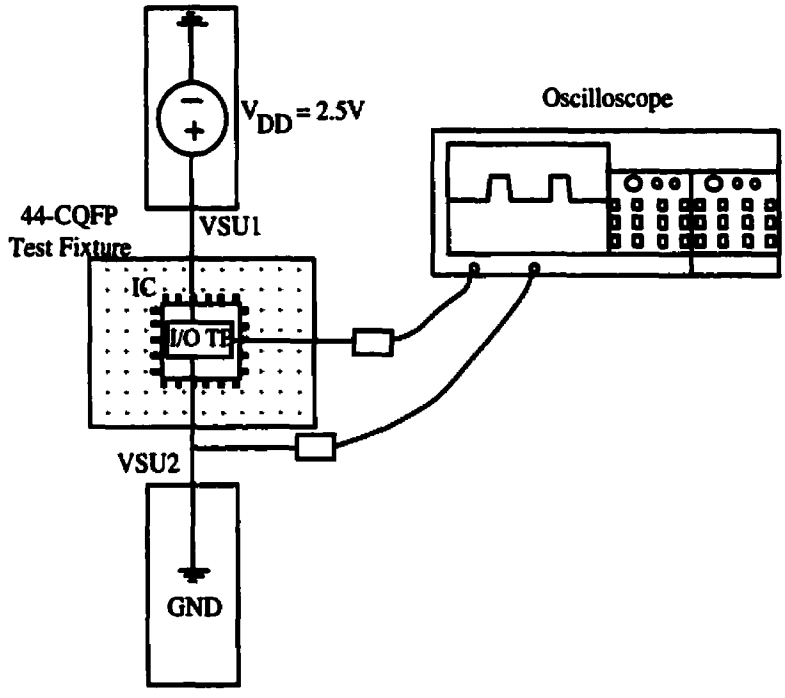

Figure 6.3: I/O Testbench Transient Test Method

The transient test method requires power supplies to provide the V_{SS} and V_{DD}=2.5V voltage supplies as well as biasing voltages. The oscilloscope is attached to the output of the testbench circuit and the frequency is determined by cursor measurements of a saved single-sweep of the oscilloscope's output waveform.

6.2 I/O Circuit Measured Results

Measurement results will be presented differently for each type of test. DC results will display a typical measurement result in figure and will compare all measurements with simulated measurements in Chapter 4.0. Transient results will display a typical output waveform in figure and compare all output frequency measurements with simulated measurements in tabular form.

6.2.1 I/O Circuit DC Measurements

PECL Transmitter

The PECL transmitter circuit for DC testing was fabricated on the MK6 chip. Testing was conducted in accordance with Fig. 6.1 with just one biasing SMU channel for the current-sink transistor set to 1V. External termination is required for testing the DC transmitter circuits. Fig. 6.4 shows a detailed setup for testing the PECL transmitter, including external biasing and termination. The labeled nodes are tested as shown in Fig. 6.1.

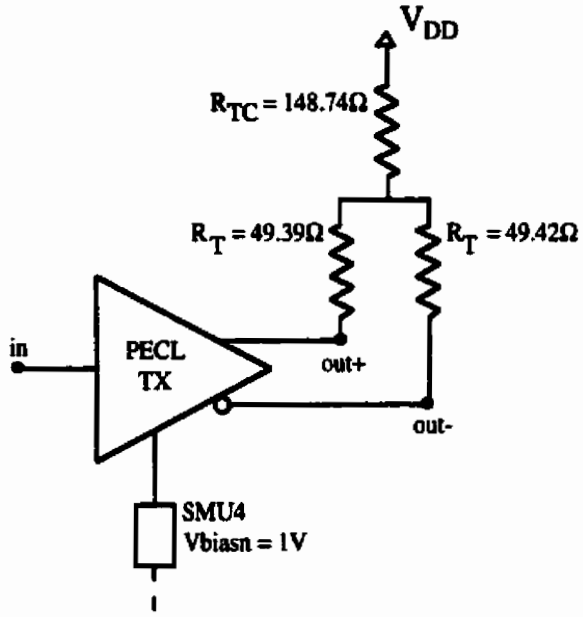

Figure 6.4: DC Test Setup for the PECL Transmitter

Fig. 6.5 shows the output voltage levels versus a V_{SS} to V_{DD} input sweep from a successful DC test of the PECL transmitter. Table 6-1 provides the average measured differential and common-mode output voltages compared with simulated values from Table 4-1.

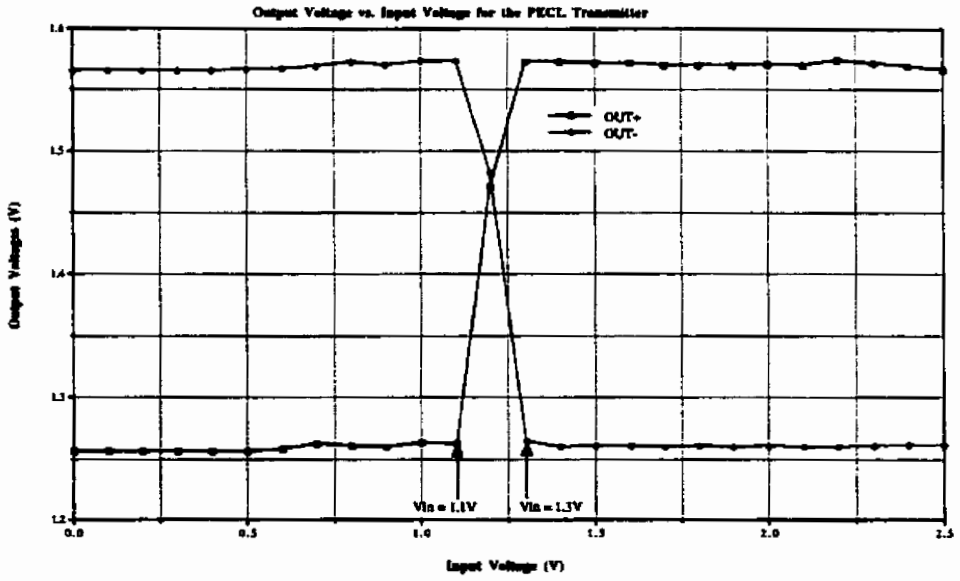

Figure 6.5: PECL Transmitter Output Levels from a DC Test

Table 6-1: Measured DC Output Values from the PECL Transmitter Circuit

PECL Transmitter Output Parameter	Average Measured Value	Simulated Value		
		SS	TT	FF
Output Differential SwingVoltage	310mV	277mV	361mV	446mV
Output Common-Mode Voltage	1.42V	1.53V	1.24V	939mV

The measured DC parameters in Table 6-1 show that the fabricated PECL transmitters operate within their HSPICE simulated range. The overall measured results show the PECL transmitter devices to be most closely modeled with the SS process corner. The measured output differential swing in Table 6-1 is adequate for the LVDS I/O standard, but the common-mode voltage is too high. However, as long as the CMR of the receiving circuit includes the common-mode value of Table 6-1, communication between the PECL transmitter and the receiver is possible.

LVDS Transmitter

The LVDS transmitter DC test circuit from the MK6 IC was tested in the same manner as in Fig. 6.1. Two biasing SMU channels are required for both the in-circuit current source and current sink device. Only one external 100Ω termination resistance is required for testing the LVDS transmitter. Fig. 6.6 describes the specific test setup for the LVDS transmitter circuit, including external biasing and termination. The labeled nodes are tested as shown in the general DC test setup of Fig. 6.1.

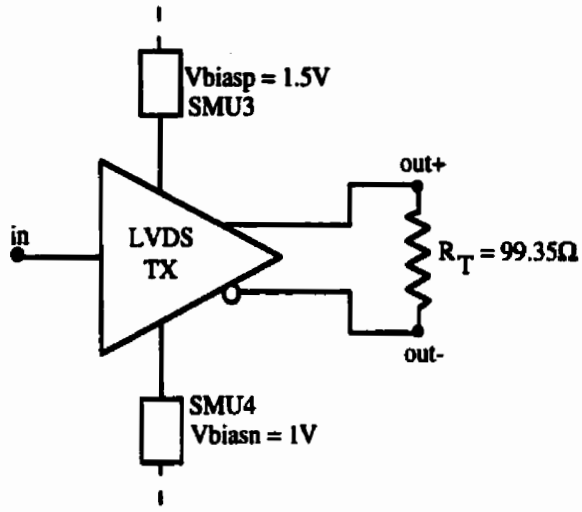

Figure 6.6: DC Test Setup for the LVDS Transmitter

The LVDS transmitter output voltages versus a V_{SS} to V_{DD} input voltage sweep is shown in Fig. 6.7. Table 6-2 contains the average measured differential and common-mode output voltages, and compares them with the simulated values from Table 4-2.

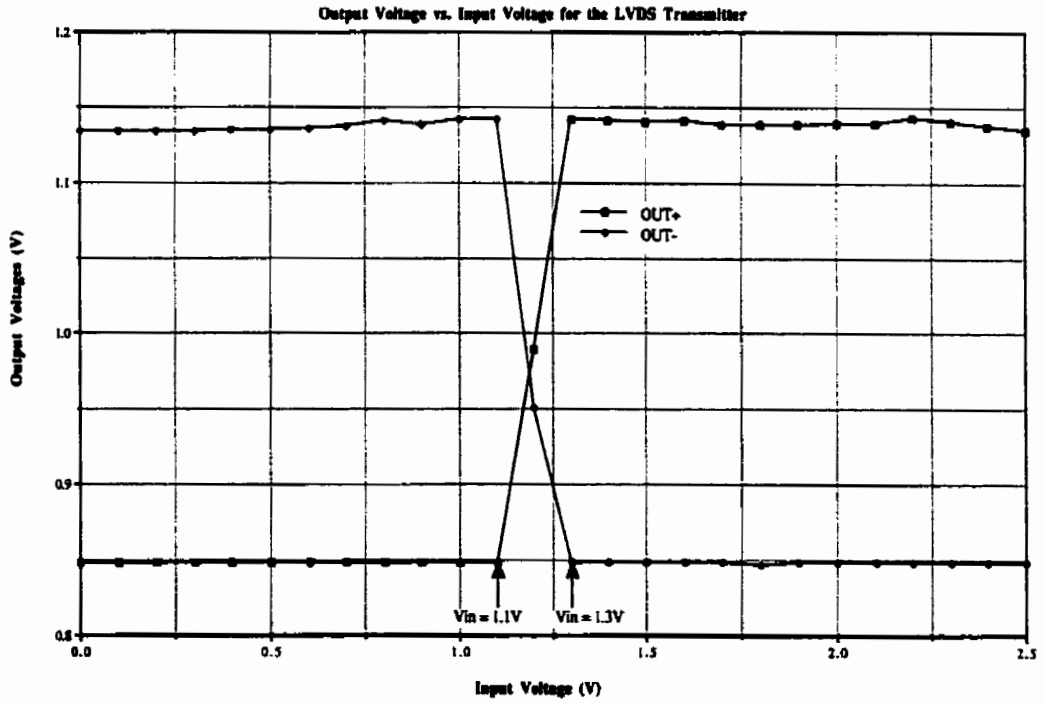

Figure 6.7: LVDS Transmitter Output Levels from a DC Test

Table 6-2: Measured DC Output Values from the LVDS Transmitter Circuit

LVDS Transmitter Output Parameter	Average Measured Value	Simulated Value		
		SS	TT	FF
Output Differential SwingVoltage	280mV	216mV	317mV	412mV
Output Common-Mode Voltage	990mV	584mV	1.12V	1.18V

The measured LVDS transmitter DC parameters in Table 6-2 are within the HSPICE simulated range of values from Chapter 4. The overall measurements show the LVDS devices to be slightly on the slow side of the typical process corner. The average measured differential output voltage of the LVDS transmitter is within the LVDS I/O specification, but the common-mode voltage is too low. As is the case with the PECL transmitter, the LVDS transmitter can still interface with a receiver provided the receiver's CMR includes the measured common-mode output voltage in Table 6-2.

PECL and LVDS Receiver

The PECL and LVDS receiving op-amp circuit from the MK6 IC was tested in the same fashion as described in section 6.1.1. SPA testing of the receiver required only one 1V biasing SMU for the receiver's current sink device. Fig. 6.8 shows an output voltage versus input common-mode plot for one op-amp receiver DC test. The two waveforms in Fig. 6.8 correspond to +200mV and –200mV input differential signal tests while the input common-mode voltage is varied.

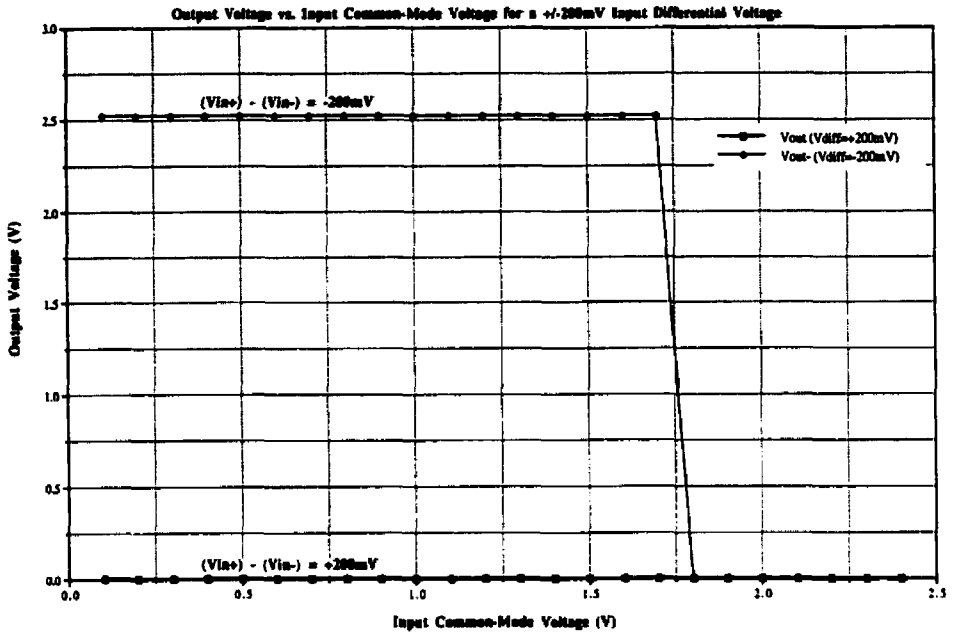

Figure 6.8: Output Voltage Vs. Input Common-Mode Voltage Plot for the PECL and LVDS Differential Amplifier Receiver

Table 6-3 provides the average CMR value for each receiver successfully tested and compares them with previously simulated values from Table 4-3.

Table 6-3: Measured CMR of the PECL/LVDS Receiver

PECL/LVDS Receiver Parameter	Average Measured Value	Simulated Value		
		SS	TT	FF
CMR	< 1.8V	<1.92V	<1.89V	<1.85V

The measured CMR of the PECL/LVDS receiver is slightly lower than the CMR range simulated by HSPICE in Chapter 4. However, as the common-mode output values measured for the PECL and LVDS transmitters are well below 1.8V, the measured PECL/LVDS receiver circuit will be capable of rectifying their transmitted signals.

GLVDS Transmitter

The GLVDS transmitter for DC testing was fabricated on both the MK5 and MK6 ICs. Testing of the GLVDS transmitter was performed in the same fashion described in section 6.1.1. As the GLVDS transmitter is voltage biased, no external termination was necessary for DC testing. However, an extra 500mV supply SMU is necessary for the GLVDS transmitter.

Fig. 6.9 presents the output waveforms versus a V_{SS} to V_{DD} input voltage sweep of the GLVDS transmitter. Table 6-4 contains measured data of the average differential and common-mode output voltages, and compares it with the HSPICE simulated values from Table 4-4.

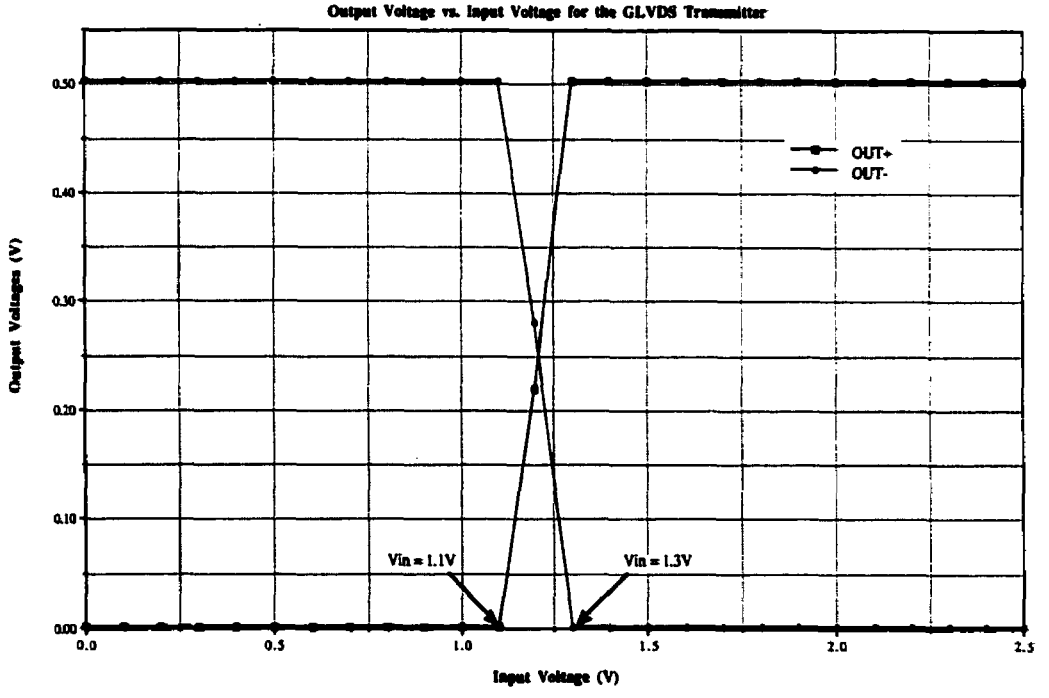

Figure 6.9: GLVDS Transmitter Output Levels from a DC Test

Table 6-4: Measured DC Output Values from the GLVDS Transmitter Circuit

GLVDS Transmitter Output Parameter	Average Measured Value	Simulated Value		
		SS	TT	FF
Output Differential SwingVoltage	500mV	500mV	500mV	500mV
Output Common-Mode Voltage	250mV	250mV	250mV	250mV

The measured GLVDS transmitter output values in Table 6-4 exactly match the DC simulated output values from Chapter 4. This is to be expected as the output values of the GLVDS transmitter depend only on the biasing voltage and not a biasing current with termination resistors.

OSDS Transmitter

The OSDS transmitter circuits fabricated on the MK6 IC were tested in accordance with Fig. 6.1. The OSDS transmitter requires only one biasing SMU for the in-circuit current source device. Two external 50Ω terminating resistors were employed in testing the OSDS transmitter's output voltages. Fig. 6.10 shows the specific DC test setup for the OSDS transmitter. The labeled nodes are tested as shown in the general DC test method in Fig. 6.1.

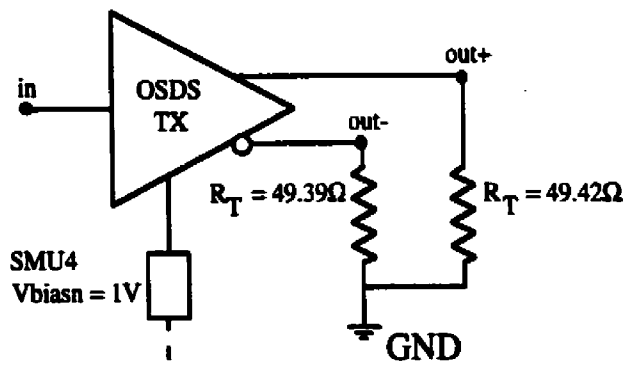

Figure 6.10: DC Test Setup for the OSDS Transmitter

Fig. 6.11 displays the OSDS transmitter output voltage waveforms versus an input voltage sweep of V_{SS} to V_{DD}. Data on the average measured differential and common-mode voltage, and their corresponding HSPICE simulated values are given in Table 6-5.

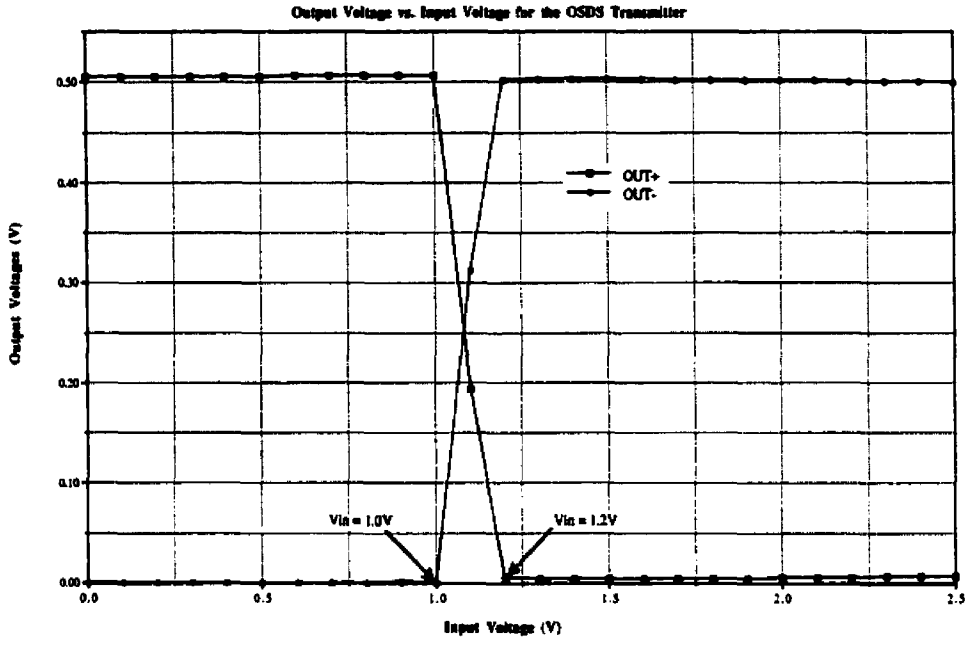

Figure 6.11: OSDS Transmitter Output Levels from a DC Test

Table 6-5: Measured DC Output Values from the OSDS Transmitter Circuit

OSDS Transmitter Output Parameter	Average Measured Value	Simulated Value		
		SS	TT	FF
Output Differential SwingVoltage	506mV	455mV	504mV	562mV
Output Common-Mode Voltage	253mV	228mV	252mV	281mV

The measured OSDS transmitter DC paramters in Table 6-5 are very close to the typical-process simulated values from Table 4-5. Provided the GLVDS/OSDS receiving circuit's CMR includes 253mV, the OSDS transmitter and its receiver will be capable of I/O communication.

GLVDS and OSDS Receiver

The GLVDS and OSDS receiver circuit was fabricated on both the MK5 and MK6 ICs. The DC testing of the receiver was performed as described in section 6.1.1. The only biasing for the GLVDS/OSDS receiver is connecting V_{SS} to the gates of the in-circuit nMOS termination transistors via the pin Vref. Fig. 6.12 shows the output voltage versus input common-mode voltage for ±200mV differential input signals.

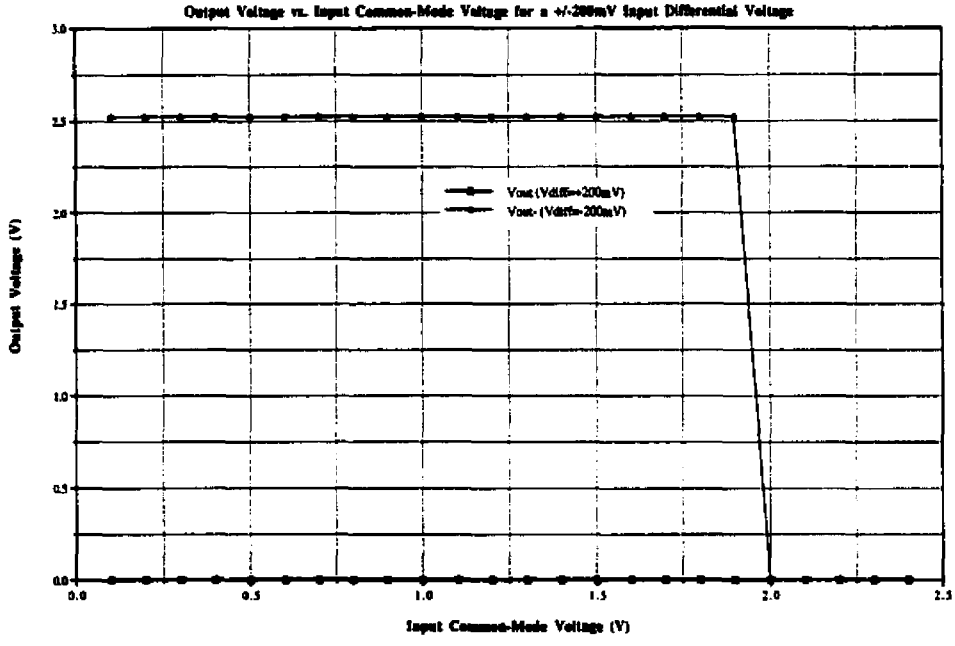

Figure 6.12: Output Voltage Vs. Input Common-Mode Voltage Plot for the GLVDS and OSDS Receiver

Table 6-6 contains the average measured CMR value for each GLVDS/OSDS receiver and compares it with the HSPICE simulated CMR range.

Table 6-6: Measured CMR of the GLVDS/OSDS Receiver

GLVDS/OSDS Receiver Parameter	Average Measured Value	Simulated Value		
		SS	TT	FF
CMR	< 2.0V	<1.90V	<1.97V	<1.98V

The measured CMR in Table 6-6 is slightly greater than the CMR range simulated in HSPICE. When testing the GLVDS/OSDS receiver, the common-mode input voltage was changed in 100mV increments only. Therefore, the true CMR value of the receiver could be anywhere between 1.9V and 2.0V which agrees with simulation. The CMR of this receiver is adequate to rectify the GLVDS and OSDS differential signals with their ~250mV common-mode voltage.

6.2.2 I/O Circuit Transient Measurements

The On-Chip Testbench Without I/O Circuits

The I/O testbench components were tested as shown in Fig. 6.3. The three circuits of interest are each ring-oscillator coupled with the ÷128 prescaler. These circuits were only present on the MK5 IC as bonding pads on the MK6 were very limited. Fig. 6.13 gives a typical measured output waveform from a ringosc1 oscillator after passing through the prescaler.

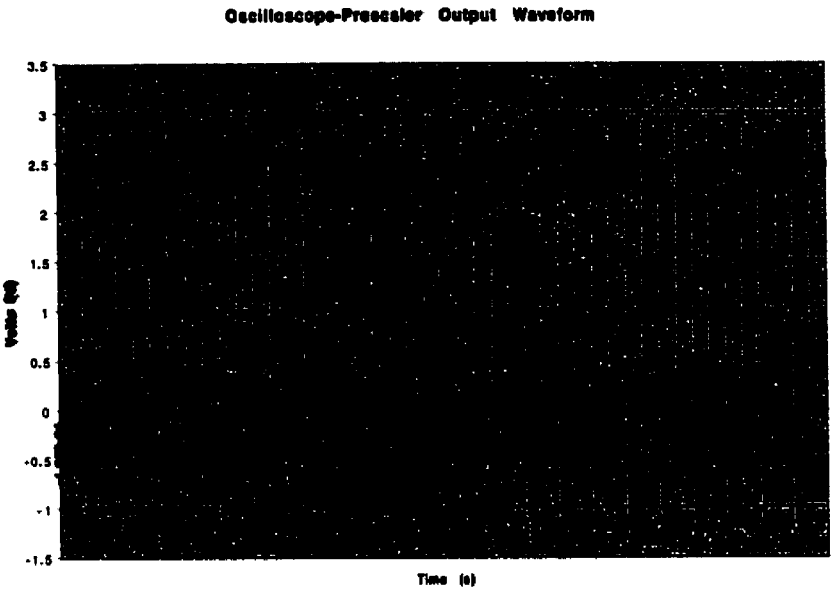

Figure 6.13: Output Waveform of the Prescaler with Ring-Oscillator 1 Input

Table 6-7 presents the average measured prescaler output frequencies for each of the three ring-oscillator inputs. Also given in Table 6-8 is the calculated prescaler input frequency (prescaler output f x128) and the range of simulated ring-oscillator output frequencies from Table 4-7.

Table 6-7: Comparison of Measured and Simulated Testbench Component Output Frequencies

Prescaler Input Oscillator	Average Measured Prescaler Output f (MHz)	Calculated Oscillator Output f (GHz)	Simulated Oscillator Output f (GHz)		
			SS	TT	FF
ringosc1	11.28	1.44	1.19	1.53	1.93
ringosc2	8.88	1.14	0.930	1.19	1.55
ringosc3	7.32	0.937	0.762	0.980	1.28

According to Table 6-7 the fabricated ring-oscillators and prescalers operate within the range simulated in HSPICE process-corner analysis. The measured output frequencies of these testbench components provide a reference for measurements of I/O testbenches with corresponding ring-oscillator stimulus.

The PECL I/O Testbenches

The PECL I/O testbenches 1, 2 and 3 were all setup and measured in accordance with Fig. 6.3. Table 6-8 presents the average measured frequencies for each of the testbenches, the measured sample size, and the number of failed measurements. All of the measured PECL testbenches were fabricated on the MK6 IC.

Table 6-8: Measured Output Frequencies from the PECL I/O Testbenches

PECL Testbench Name	Average Measured Output *f* (MHz)	Number of Measurements	Number of Failed Measurements
Testbench 1	11.48	10	2
Testbench 3	7.53	10	7

Table 6-9 compares the measured PECL testbench output frequencies and compares them with range of simulated output frequencies in Chapter 4.0.

Table 6-9: Comparison of PECL Testbench Measured and Simulated Output Frequencies

PECL Testbench Name	Average Measured Output *f* (MHz)	Simulated Output *f* (MHz)		
		SS	TT	FF
Testbench 1	11.48	9.30	11.95	15.48
Testbench 3	7.53	5.98	7.67	9.94

As seen in Table 6-9, the tested PECL I/O testbenches 1 and 2 output a CMOS signal at an average frequency very close to that which was simulated in HSPICE. The measured frequencies are also very close to the operating frequencies of the oscillator-prescaler pair in Table 6-7. Based on Table 6-10 the PECL transmitter and PECL/LVDS receiver are capable of operating on-chip between 964MHz and 1.47GHz.

The LVDS I/O Testbenches

The LVDS I/O testbenches were connected and measured as shown in Fig. 6.3. Table 6-10 contains the average measured frequencies for each testbench along with the measured sample size and the number of failed measurements. All of the measured LVDS testbench circuits were fabricated on the MK6 chip.

Table 6-10: Measured Output Frequencies from the LVDS I/O Testbenches

LVDS Testbench Name	Average Measured Output *f* (MHz)	Number of Measurements	Number of Failed Measurements
Testbench 1	11.92	10	4
Testbench 3	7.62	10	5

The measured output frequencies of Table 6-10 are compared with the simulated fequencies of Chapter 4.0 in Table 6-11.

Table 6-11: Comparison of LVDS Testbench Measured and Simulated Output Frequencies

LVDS Testbench Name	Average Measured Output f (MHz)	Simulated Output f (MHz)		
		SS	TT	FF
Testbench 1	11.92	9.28	11.96	15.51
Testbench 3	7.62	5.98	7.67	9.97

The measured results in Table 6-11 are very close to both the HSPICE simulated results and the oscillator-prescaler circuit output frequencies of Table 6-7. It can be concluded from the Table 6-11 data that the LVDS transmitter and PECL/LVDS receiver make a usable I/O interface in the 975MHz-1.53GHz operating frequency range.

The GLVDS I/O Testbenches

The GLVDS testbenches were fabricated on both the MK5 and MK6 IC. The MK5 chip contained all three testbench designs while MK6 held only the GLVDS testbench 1 and 3 designs due to bond-pad density limitations. All measured GLVDS testbench circuits were tested in accordance with Fig. 6.3. Table 6-12 holds the averaged measured frequencies, the measured sample size and the number of failed measurements per the MK5 and MK6 IC.

Table 6-12: Measured Output Frequencies from the GLVDS I/O Testbenches

GLVDS Testbench Name	Average Measured Output f (MHz)	Number of Measurements	Number of Failed Measurements
MK5 Testbench 1	10.23	20	2
MK5 Testbench 2	8.47	10	1
MK5 Testbench 3	7.02	10	0
MK6 Testbench 1	11.53	10	4
MK6 Testbench 3	7.40	10	6

Table 6-13 provides a comparison of the measured and simulated output frequencies of the GLVDS I/O testbenches.

Table 6-13: Comparison of GLVDS Testbench Measured and Simulated Output Frequencies

GLVDS Testbench Name	Average Measured Output *f* (MHz)	Simulated Output *f* (MHz)		
		SS	TT	FF
Testbench 1	MK5: 10.23 MK6: 11.53	9.30	11.94	15.49
Testbench 2	MK5: 8.47	7.27	9.34	12.12
Testbench 3	MK5: 7.02 MK6: 7.40	5.97	7.67	9.95

As can be seen in Table 6-13, the MK5 devices tend to operate towards the SS process corner while the MK6 devices are closer to the TT process parameters. Both the MK5 and MK6 GLVDS testbenches operate within the range of HSPICE simulated frequencies and are similar to the oscillator-prescaler operation described in Table 6-7. Therefore the GLVDS transmitter and receiver are a capable I/O interface on-chip in the 899MHz to 1.48GHz operating frequency range.

The OSDS I/O Testbenches

The OSDS testbench 1 and 3 circuits were fabricated on the MK6 chip. The testing of the OSDS testbench circuits was performed as shown in Fig. 6.3. Table 6-14 presents the average measured output frequency, the measured sample size, and the number of failed measurements for each OSDS I/O testbench.

Table 6-14: Measured Output Frequencies from the OSDS I/O Testbenches

OSDS Testbench Name	Average Measured Output *f* (MHz)	Number of Measurements	Number of Failed Measurements
Testbench 1	11.38	10	4
Testbench 3	7.42	10	5

A comparison of the Table 6-14 measured values and the simulated frequencies of Chapter 4.0 is given in Table 6-15.

Table 6-15: Comparison of OSDS Testbench Measured and Simulated Output Frequencies

OSDS Testbench Name	Average Measured Output *f* (MHz)	Simulated Output *f* (MHz)		
		SS	TT	FF
Testbench 1	11.38	9.30	11.95	15.65
Testbench 3	7.42	5.97	7.67	9.96

Table 6-15 clearly shows that the average measured output frequencies of the OSDS testbench 1 and testbench 3 are within the range of frequencies simulated in HSPICE. It can be concluded from Table 6-15 that the OSDS transmitter and GLVDS/OSDS receiver are capable of communicating on-chip within the 950MHz-1.46GHz frequency range.

6.3 Problems Encountered During Measurements

During both DC and transient measurements, strange operating performance was noticed in many of the circuits on the MK6 chip. In DC tests, appropriate output levels were often recorded but without any switching of the output differential voltage over a V_{SS} to V_{DD} differential input sweep. In the I/O testbenches, many circuits failed to output any frequency and instead displayed stuck-at 0 or 1 faults.

During further DC testing with the SPA, it was noticed that circuit inputs connected to internal bias gates were drawing >100uA of current. As the input resistance of MOS gates is in the order of 10MΩ-10GΩ, the presence of >100uA gate-currents (I_G) indicates a relatively low-resistance connection between the gate and one of the internal power buses. This discovery of excessive gate current sparked further testing of all gate inputs for each MK6 chip tested. With the SPA, each gate's input voltage was swept between V_{SS} and V_{DD} while the on chip supplies were powered appropriately. Table 6-16 provides a summary of the gates tested, the input gate-current, and the number of on-chip circuits which failed in DC and transient measurements.

Table 6-16: Summary of Input Gate Currents on the MK6 Integrated Circuit

Category	# Tested
Gates With I_G > 500uA	105
Gates with 1uA < I_G < 500uA	30
Gates with I_G < 1uA	65
Total Gates Tested	200
Total Failed Circuit Measurements	91
Total Circuits Tested	130

It is believed that this excessive gate leakage is what caused many of the testbenches to fail during transient testing. Two different power supplies were used in transient measurements: one supply provided V_{DD} and V_{SS}, the other supply provided gate voltages for biasing devices in the I/O transmitter and receiver circuits. In many failed tests of the testbenches, it was noticed that the biasing-supply display would change when the V_{DD} and V_{SS} supply was turned on and would then return to its proper value when

V_{DD} and V_{SS} was turned off. One hypothesis is that the V_{DD} and V_{SS} supply was coupling onto the bias device's gate via the same path which was causing excessive input gate currents. It is very difficult to determine the reliability of any measurements made from the MK6 chip. The GLVDS testbenches which are present on MK6 were directly copied from designs initially fabricated on the MK5 chip. The GLVDS testbenches on MK5 were measured with output frequencies close to those simulated in Chapter 4.0 with almost 100% yield. However, the identical designs fabricated on MK6 provided an output (erroneous or not) with less than 40% yield. Therefore, the evidence points towards a process or post-process event which may have compromised device-gate isolation.

A possible process event may be poor yield on the gate-oxide growth process which results in many gate-to-channel shorts. The pads on MK6 are not ESD protected and therefore handling the ICs without heeding standard anti-ESD practise may also breakdown the gate-oxide and short the gate to the channel. The MK5 and MK6 chips were both handled in accordance with standard anti-ESD practise (static mats, handler is grounded, anti-static packaging, etc.), therefore any ESD damage of MK6 would have occurred before the chips were received.

Another possible reason for gate-channel shorts in the MK6 devices is due to in-process antenna effects. During the etching of large pad metal areas a charge is developed on the metal. If this pad is connected to a small poly-gate area, charge-sharing develops a voltage on the poly-gate sufficient to breakdown the gate-oxide isolation. It was

discovered after fabrication that the CMC service which checks for antenna rule violations was unstable. However, these antenna problems did not appear on the MK5 IC, making the source of the gate leakage still unclear.

6.4 Summary of Measurement Results

The fact that gate current levels on MK6 are very high, and identical GLVDS testbench circuits were successfully tested on MK5 but not on MK6, points towards a low yield from the manufacturer. Whether the low yield originated at the manufacturer or at the IC packager is still not known. However, the successful measurements which were recorded are enough to verify the functionality of the fabricated circuits.

The DC measurements of the I/O transmitters and receivers showed all to be working within the range of operation simulated by HSPICE in Chapter 4. Measurements of the I/O transmitters yielded adequate differential and common-mode output voltage levels. The I/O receivers were tested to prove they are capable of rectifying a 200mV differential input signal and to determine their input CMR. The overall DC measurement results showed that each transmitter's DC output levels were compatible with its respective receiver's DC input parameters. The DC measurement results were confirmed by the successful operation of the I/O testbench circuits.

Initial testbench measurements were performed on the oscillator-prescaler paired circuits fabricated on MK5. The measured output frequencies of the oscillator-prescaler circuits yielded corresponding prescaler input frequencies which were within the HSPICE

simulated ranges for each ring-oscillator circuit. The PECL, LVDS, GLVDS and OSDS testbench 1 and 2 circuits were tested from the MK6 IC. The GLVDS testbenches 1, 2 and 3 were also fabricated on the MK5 chip and tested. All the fabricated I/O testbenches were measured with output frequencies within the HSPICE corner-analysis simulation range determined in Chapter 4. Both the MK5 and MK6 measurements showed the process to be close to its typical parameters with the MK5 IC belonging to a slower process run (according to the small sample size).

Through the successful measurements of each I/O circuit and testbench we found that the measurement sample size was sufficient to confirm their functionality. However, the sample size is still too small to provide as comprehensive a comparison of the I/O circuits as initially desired. Additionally, each of the I/O circuits tested within the on-chip I/O testbench circuit framework were successful in operation, leaving no recognizable superior I/O circuit in the context of output bandwidth. Therefore, the conclusions in this thesis will have to depend more heavily on the I/O circuit simulated performance than initially anticipated. Relying more on the simulated performance of the I/O circuits does not make the fabrication and measurement of the circuits for naught. In fact, the strong correlation between circuit measurements in this chapter and their simulation in Chapter 4 lends credibility to conclusions based on the simulated I/O circuit performance.

7.0 Thesis Summary and Conclusions

The goal of the thesis was to compare each I/O standard through the I/O circuits based on:

- Circuit performance – power consumption, output bandwidth.
- Process robustness – sensitivity of designs to process variation, scalability to lower supply voltages.
- Physical design – layout area, on or off-chip termination requirements, necessity for extra supply or bias pins.

In this section, the data presented in this thesis will be summarized, and conclusions will be made based on each of the points set out in the thesis goal.

The most discerning points for each I/O standard and its circuit implementation can be derived from analyzing the transmitter I/O standard specifications and the transmitter circuit architecture. Each receiver discussed in this thesis simply amplifies the sensed low-voltage differential output levels which have been generated by the transmitter circuit and rectifies it to a single-ended CMOS signal. The low-power nature and scalability of the receiver/amplifier circuits contribute little to the comparison of the I/O standards implemented in this thesis except in regards to physical layout issues. Therefore, discussions of power consumption, output frequency, and circuit scalability will be based primarily on the analysis of the transmitter circuits.

Circuit Performance

In a general comparison of the I/O standards and their transmitter circuit designs, it is the current-biased designs of the LVDS, PECL, and OSDS standards which are the least efficient relative to the voltage-biased design of the GLVDS standard. In the current-biased designs, current is sourced/sunk from/to a potential different than the generated output voltage. The result is the output bias current passing through the transmitter over a potential difference which increases the on-chip DC power dissipation in the transmitter. Even when the transmitter maintains static output levels, the current-biased transmitters dissipate this on-chip power. In the voltage-biased GLVDS transmitters, the output levels are equal to the transmitter supply potentials. Power is only dissipated in the GLVDS transmitter when output levels are switching and output capacitances must be charged or discharged to their new output level. When maintaining static output voltages, the GLVDS transmitter only provides enough power to generate the output levels across the termination while the on-chip dissipated power is negligible.

Each I/O transmitter/receiver pair was found to be capable of operating between 950MHz and 1.5GHz via measurements of the on-chip I/O testbenches. These measured results were in strong agreement with the simulated testbench performances from Chapter 4. Further simulations were performed on the I/O circuit pairs to estimate their maximum frequency of operation. The PECL and LVDS I/O circuits were unable to operate reliably above 4GHz while the GLVDS circuit operated up to 6GHz before failing. The maximum simulated frequency of operation was 10GHz from the OSDS I/O circuit pair simulations. Although the simulated maximum operation frequency of the I/O circuit

pairs may not be exact in reality, they provide a relative comparison between the potential I/O circuit performances. The high-frequency performance of the OSDS circuit pair is why a ratio of operating power to maximum operating bandwidth is a better I/O performance benchmark than power or bandwidth alone. Although the OSDS circuits consume more power than the GLVDS circuits, the GLVDS circuits can not compete with the OSDS circuits above 5GHz in simulation despite their low-power operation.

Process Robustness

The GLVDS transmitter design is the least sensitive to process variation and voltage supply change when compared with the current-biased transmitter designs. As each transistor in the GLVDS transmitter acts simply as a switch for the supply potentials, process variation does not change the output levels. Voltage supply changes also do not significantly affect the GLVDS transmitter design. The GLVDS transmitter is powered with 250mV-500mV supplies which are not at all close to projected CMOS technology supplies over the next decade.

The current-biased transmitter designs for the PECL, LVDS, and OSDS standards can be quite sensitive to process variation as seen in their simulated and measured performances. Their reliance on current bias transistors to generate a constant output current make the output current sensitive to the processing of the bias device. In this respect, the LVDS is the most sensitive to process variation as it depends on both a current source and sink device to establish its output voltages. The PECL and OSDS transmitter designs contain only one current biasing transistor and are thus less sensitive to process variation as

supported by their simulation results in Chapter 4. However, the OSDS transmitter uses V_{SS} as one of its output levels, making its output swing less sensitive to process variation than the PECL design.

The current-biased transmitter designs are also quite sensitive to changes in supply voltages due to constant electric-field scaling in new CMOS technologies. As voltage supplies are reduced, the biasing transistors in the transmitters may need to be changed beyond simple aspect-ratio scaling to 'tune' the circuit for appropriate output current.

Several of the I/O standard specifications themselves are very sensitive to reduction in power supplies. The PECL transmitter is based on an open-drain PECL transmitter architecture but was configured to transmit LVDS output levels. The 2.5V supply for the 0.25μm CMOS process is already too low to easily design the PECL transmitter for PECL output levels. Additionally, the 750mV output swing of the PECL standard requires such a large output current that it is not efficient to implement when other differential I/O standards such as LVDS, GLVDS or OSDS are available. The LVDS standard will probably be the next I/O standard to become obsolete as it specifies an output common-mode voltage of ~1.2V. As IC supplies get closer to the output common-mode voltage of an I/O standard, the circuits to implement the I/O standard become increasingly difficult to design until they finally become impossible. For this reason, the GLVDS and OSDS standards have a greater "time-to-obsolescence" than PECL or LVDS as their output common-mode voltage is 250mV at maximum.

Physical Design

The ease of physical design and the physical circuit area are also important considerations when comparing the various I/O circuits. Of all the transmitter circuits, the PECL design is the most compact as it is composed of three nMOS transistors which can be laid out in the same active region. The next most compact transmitter designs are the OSDS and GLVDS circuits. The OSDS circuit is composed of three transistors but requires two active regions to accommodate both nMOS and pMOS devices. The GLVDS transmitter is also quite compact as it contains four nMOS transistors which may be designed in the same active region. The LVDS transmitter contains six transistors and is the least area-efficient of the transmitter physical designs.

The receiver design for the PECL and LVDS transmitter circuits requires the least amount of IC area. The PECL/LVDS receiver is a single-stage amplifier composed of five small transistors. The GLVDS/OSDS receiver contains >10 transistors in complex connections. Therefore the GLVDS/OSDS receiver requires the most IC area and is not as easy to implement in layout as the PECL/LVDS receiver.

In summary, the GLVDS I/O standard seems to be the most power efficient and flexible relative to advancing CMOS technology. The GLVDS transmitter offers high-frequency operation, low on-chip power dissipation, a compact physical design, and has a lot of 'headroom' beneath the lowering process voltage supply ceiling. Although the GLVDS/OSDS receiver is greater than the PECL/LVDS receiver in physical area and design complexity, its disadvantages are mitigated by its large CMR and voltage noise

immunity. Similarly, the OSDS I/O transmitter offers a compact physical design and headroom beneath current process supply voltages. The OSDS does dissipate more on-chip power than the GLVDS transmitter, but a reduction in output voltage swing proportionally reduces this power consumption. Additionally, the OSDS transmitter has nearly twice the operating bandwidth than the GLVDS transmitter in simulation. The OSDS transmitter may require more operating power than the GLVDS transmitter, but the extra power may buy > 5GHz operation in a single transmitter/receiver pair.

The PECL and LVDS I/O circuits do not provide as large a simulated operating bandwidth as the GLVDS and OSDS circuits in simulation. The PECL transmitter design which outputs LVDS standard levels has a compact physical design and a lower power consumption than OSDS, but is still greater than GLVDS. Between the PECL and LVDS transmitter which both output LVDS levels, the LVDS transmitter suffers from greater process sensitivity. However, the LVDS transmitter architecture allows lower on-chip power dissipation, as a 100Ω termination resistance is used to generate output voltages rather than a 50Ω which cuts output current in half for the same output voltage.

In conclusion, based on the I/O standard specification, the implemented I/O circuit architectures, the I/O circuit physical designs, and their simulated and measured behaviour, the I/O standards can be ranked as follows:

1) GLVDS and OSDS
2) LVDS

3) PECL

These rankings are based on current and projected future needs for faster I/O circuits running in lower voltage environments. The LVDS and PECL I/O standards are still usable for where they meet design specifications. However, the GLVDS and OSDS capabilities exceed that of PECL and LVDS for use in cutting-edge IC designs.

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